IEEE SOLID-STATE CIRCUITS SOCIETY

ADVANCE PROGRAM

2016 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

JANUARY 31 — FEBRUARY 1, 2, 3, 4

CONFERENCE THEME:

SILICON SYSTEMS FOR THE INTERNET OF EVERYTHING

SAN FRANCISCO
MARRIOTT MARQUIS HOTEL

5-DAY PROGRAM

SUNDAY ALL-DAY
2 FORUMS: SECURE SYSTEMS; DATA CONVERTER ADAPTIVE CALIBRATION
10 TUTORIALS: VCO PHASE NOISE; MEMORY-TIER IMPLICATIONS; HIGH-VOLTAGE DESIGN; POWER-MANAGEMENT SYSTEMS; SAR ADCs; OPTICAL INTERCONNECTS; LOW-POWER ASYNCHRONOUS CIRCUITS; NOISE IN MIXED-SIGNAL SoCs; LOW-POWER WIRELESS CIRCUITS; CIRCUIT FOR IMPLANTABLES
2 EVENING EVENTS ON GRADUATE STUDENT RESEARCH IN PROGRESS, POWER-EFFICIENT COMPUTER ARCHITECTURES

THURSDAY ALL-DAY
4 FORUMS: CIRCUITS & ARCHITECTURES FOR 5G; SHORT-REACH INTERCONNECTS FOR IoE; ICs FOR LOW-NOISE SENSING; WEARABLE/IMPLANTABLE SYSTEMS
SHORT-COURSE: CIRCUITS FOR IoE

ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at thecutting edge of IC design and application to maintain technical currency, and to network with leading experts.

CONFERENCE TECHNICAL HIGHLIGHTS

On Sunday, January 31st, the day before the official opening of the Conference, ISSCC 2016 offers:

- A choice of up to 4 of a total of 10 Tutorials
- A choice of 1 of 2 all-day Advanced-Circuit-Design Forums

The 90-minute tutorials offer background information and a review of the basics in specific circuit-design topics. In the all-day Advanced-Circuit-Design Forums, leading experts present state-of-the-art design strategies in a workshop-like format. The Forums are targeted at designers experienced in the technical field.

On Sunday evening, there are two events: A Special-Topic Session entitled, "Computing Architectures Paving the Path to Power Efficiency" will be offered starting at 8:00pm. In addition, the Student Research Preview, featuring short presentations followed by a poster session from selected graduate-student researchers from around the world will begin at 7:30 pm. Introductory remarks at the Preview will be provided by a distinguished member of the solid-state circuit community, Professor Rinaldo Castello of the University of Pavia, Italy.

On Monday, February 1st, ISSCC 2016 offers four plenary papers on the theme: "Silicon Systems for the Internet of Everything (IoE)". On Monday at 12:15 pm, there will be a Women's Networking Event, a luncheon. On Monday afternoon, there will be five parallel technical sessions, followed by a Social Hour open to all ISSCC attendees. The Social Hour, held in conjunction with the Book Display and Author Interviews, will also include a Demonstration Session, featuring posters and live demonstrations for selected papers from industry and academia. Monday evening will include 2 panel sessions on "**Class of 2025 — Where Will Be the Best Jobs?**" and "**Do We Need to Downscale Our Radios Below 20nm?**".

On Tuesday, February 2nd, there are five parallel technical sessions, both morning and afternoon. A Social Hour open to all ISSCC attendees will follow. The Social Hour, held in conjunction with the Book Display and Author Interviews, will also include a second Demonstration Session. Tuesday evening sessions includes two panels on "**Survey Says!**" and "**Eureka! The Best Moments of Solid-State Circuit Design in the 2000's**".

On Wednesday, February 3rd, there will be five parallel technical sessions, both morning and afternoon, followed by Author Interviews.

On Thursday, February 4th, ISSCC offers a choice of five all-day events:

- A Short Course on "**Circuits for Internet of Everything (IoE)**"
- Four Advanced-Circuit-Design Forums on
  - "**Radio Architectures & Circuits Towards 5G**";
  - "**Emerging Short-Reach & High-Density Interconnect Solutions for IoE**";
  - "**Advanced IC Design for Ultra Low-Noise Sensing**";
  - "**Circuit, Systems and Data Processing for Next Generation Wearable/Implantable Medical Devices**"

Registration for educational events on Sunday and Thursday will be filled on a first-come first-served basis. Use of the ISSCC Web-Registration Site (http://www.isscc.org) is strongly encouraged. Registrants will be provided with immediate confirmation on registration for the Conference, Tutorials, Advanced-Circuit-Design Forums, and the Short Course.

Need Additional Information? Go to: www.isscc.org

TABLE OF CONTENTS

T1: Understanding Phase Noise in LC VCOs

Over the last 20 years, the analysis of phase noise in LC oscillators has been one of the most discussed topics in the area of RF IC design. Phase noise is difficult to analyze and represents one of the main bottlenecks in the design of a transceiver. This tutorial will focus on the basics of phase noise in LC oscillators, emphasizing physical intuition over mathematics. The tutorial will begin with the basics of LC oscillators, followed by an explanation of the characteristics of phase noise and its impact on transceiver performance. Emphasis will be on the evaluation of phase noise in the most important LC oscillator topologies, and the analysis of the up-conversion mechanism for flicker noise. This will highlight fundamental limits of phase noise and the trade-off with power dissipation. The last part of the tutorial will present advanced LC oscillator topologies.

Instructor: Carlo Samori

Carlo Samori received the Ph.D. in electrical engineering in 1995, at the Politecnico di Milano, Italy, where he is now a Professor. His research interests are in the area of RF circuits, in particular of design and analysis of VCOs and high-performance frequency synthesizers. He has collaborated with several semiconductor companies. He is a co-author of more than 100 papers and of the book Integrated Frequency Synthesizers for Wireless Systems (Cambridge University Press, 2007). Prof. Samori is a member of the International Technical Program Committees of the IEEE International Solid-State Circuits Conference and the European Solid-State Circuits Conference. He was Guest Editor for the December 2014 issue of the IEEE Journal of Solid-State Circuits.

T2: Basics of Memory Tiers in Compute Systems

As Moore's Law challenges have slowed CPU lithography-based performance scaling, potential changes in the memory subsystem stand out as one area where continued system-level performance improvements can be realized. As part of this tutorial, a server Total Cost of Ownership (TCO) model will be presented that can apply from stand-alone servers to datacenters. This model will be used to evaluate the wider impact of performance and behavioral characteristics of various tiers of the memory hierarchy - from SRAM cache to new tiers of emerging memory. Typical datacenter workloads and how the memory tiers are utilized will also be presented.

Instructor: Rob Sprinkle

Rob Sprinkle is a Technical Lead in Google's Data Center Infrastructure Advanced Technology Team. He is responsible for working with established and emerging memory technology companies to track and influence strategic technical directions, and internally to determine best uses of emerging memory technologies in the infrastructure. Previously he was the technical lead for the concept and hardware design of Google's first custom NAND Flash storage tier. Prior to 2006, he was a SiGe bipolar circuit, PCB, and ASIC/FPGA designer at Teradyne. He received a BSEE from the Virginia Military Institute and has been issued numerous patents with others pending.

T3: High-Voltage Power Devices, Converter Topologies and Applications

Power electronics can be found in everything from electric vehicles and industrial motors, to laptop power adaptors that hook up to the wall outlets. While silicon still dominates the power-semiconductor landscape, the recent onset of wide-bandgap semiconductor (WBG) devices promises low loss, higher-frequency operation of converters leading to smaller, lighter power supplies. This tutorial will introduce the properties of high-voltage (200 to 1200V) Si superjunction and WBG devices and discuss their relative merits. Common power-converter topologies employed in power systems will be explored with a detailed analysis of the main loss mechanisms inside a converter and the impact of topology and device choice on efficiency and power density. The latter part of the tutorial will discuss gate drive and associated protection circuits that are required to safely operate the power FETs with examples provided from commercial gate driver designs.

Instructor: Yogesh Ramadass

Yogesh Ramadass received his B. Tech. degree from the Indian Institute of Technology, Kharagpur in 2004 and the S. M. and Ph.D. degrees in Electrical Engineering from MIT in 2006 and 2009. He is currently working at Texas Instruments where he is the Director of Power Management R&D in Kilby Labs, Santa Clara. Dr. Ramadass was awarded the President of India Gold Medal in 2004 and the EETimes 'Innovator of the Year' award in 2013. He was a co-recipient of the Jack Kilby best student paper award at ISSCC 2009 and the Beatrice Winner award for editorial excellence at ISSCC 2007. He serves on the Technical Program Committee for ISSCC and ISLPED.

T4: System-Level Power-Management Techniques

The Internet of Everything covers a wide spectrum of systems from sensors to servers, implemented in a wide range of semiconductor technologies. The underlying challenges of managing active and standby power and energy depend on the process technology and power sources and are covered as fundamentals in this tutorial. The requirement for a systems-level approach to power management and control in order to exploit dynamic and standby power and energy savings will then be explained. Practical examples will be covered for both high-end processing systems for cloud and hub applications, where power and thermal profile are most significant, as well as low-end processing in Wireless Sensor Nodes where energy saving is paramount.

Instructor: David Flynn

David Flynn received his B.Sc.(Hons) in Computer Science from Hatfield Polytechnic, UK and his Dr.Eng. in Electronic Engineering from the Loughborough University UK in 2007. He is a Senior Member of the IEEE. Since October 1991 he has worked for ARM Ltd, specializing in low-power design and IP deployment. Dr. Flynn was recognized as an ARM Fellow in 2000. Since 2008 he has also served part-time as a Visiting Professor with the University of Southampton and is co-director of the ARM-ECS Research Centre. He currently serves on technical program committees for DAC, ISSCC, SNUG-Silicon Valley and ARM TechCon.

T5: Basics of SAR ADCs: Circuits & Architectures

This tutorial will cover the fundamentals of Successive-Approximation-Register (SAR) Analog-to-Digital Converters (ADCs), as well as the latest architectural innovations that have led to unprecedented performance metrics. While SAR ADCs have been around for a very long time, a lot of attention has been given to them in recent years in the context of process scaling. Performance gains in submicron processes were expected, but the extent to which improvements in power-efficiency and conversion speed were demonstrated has been somewhat surprising. The tutorial is intended to bring audience members up to speed on this topic at architectural, circuit and algorithm levels.

Instructor: Pieter Harpe

Pieter Harpe received the M.Sc. and Ph.D. degrees from the Eindhoven University of Technology, The Netherlands. In 2008, he joined Holst Centre / IMEC where he worked on ultra-low-power wireless transceivers, with a main focus on ADC research and design. In April 2011, he joined Eindhoven University of Technology as Assistant Professor on low-power mixed-signal circuits. His main interests include power-efficient and reconfigurable data converters, signal acquisition systems and low-power analog design. He is co-organizer of the yearly workshop on Advances in Analog Circuit Design and a member of the TPC for ISSCC and ESSCIRC.

T6: Optical Interconnects: Design and Analysis

This tutorial presents design and analysis of high-performance receivers and transmitters for optical interconnects. After a description of an overall electrical-optical-electrical (EOE) link as a framework, an introduction to optical devices and their modeling for circuit designers will be presented, followed by an introduction to circuit topologies for modulator drivers, VCSEL drivers and front-end receivers. Silicon photonic devices such as micro-ring modulators, Mach Zehnder modulators (MZM), electroabsorption modulators (EAM), and waveguide photo-detectors will then be discussed. Additional topics will include the co-design of electronics and photonics, analysis, simulation and performance trade-offs, as well as equalization, bandwidth enhancement and thermal control for modulators and VCSELs.

Instructor: Azita Emami

Azita Emami received her M.S. and Ph.D. degrees in Electrical Engineering from Stanford University in 1999 and 2004 respectively. She received her B.S. degree from Sharif University of Technology in 1996. In 2004, she joined IBM T. J. Watson Research Center, Communication Technologies Department. In 2007, she joined Caltech, where she is now a Professor of Electrical Engineering and Medical Engineering. Her current research interests include mixed-signal integrated circuits and systems, high-speed on-chip and chip-to-chip electrical and optical interconnects, clocking techniques, wearable and implantable devices for health, biomedical sensors, drug delivery systems, and compressive sensing.

T7: Asynchronous Circuit Design and Methodology for Low-Power IoE

Asynchronous circuits have characteristics that differ significantly from those of synchronous circuits in terms of their power and robustness to variations. This tutorial will show how it is possible to exploit these characteristics to design ultra-low-power and robust circuits in the scope of the Internet-of-Everything (IoE) and also Globally Asynchronous and Locally Synchronous architectures. More specifically, the aims of the tutorial are to give fundamentals of asynchronous circuits design and to detail design methodologies with practical low-power asynchronous circuits examples. At the end of the tutorial, attendees will be able to differentiate the usefulness of an asynchronous circuit compared to a synchronous one according to their application needs.

Instructor: Edith Beigne

Edith Beigne joined CEA-LETI, Grenoble, France, in 1998. She first focused her research on asynchronous mixed-signal circuits and systems for wireless applications. In 2002, she developed an asynchronous NoC dedicated to Globally Asynchronous and Locally Synchronous complex digital circuits. Since 2009, she is a senior scientist in the digital and mixed-signal design lab where she conducts research on low-power and adaptive circuit techniques. She led complex test-chip designs dedicated to low power and variability management, exploiting asynchronous design and advanced technology nodes like FDSOI 28nm and 14nm for many different applications from high-performance MPSoC to ultra-low-power IoT devices.

T8: Noise Simulation in Mixed-Signal SoCs

This tutorial presents an overview of integrated power and substrate noise simulation techniques to verify noise coupling in mixed analog-digital system-on-chip integration. The simulation captures: (1) background mechanisms, (2) power noise generation in digital portions of a chip, (3) substrate noise propagation in a whole die, and (4) noise interference with analog circuitry on the same chip. The models for chip-package-board interaction in power delivery networks and noise coupling in a silicon substrate will also be covered. A silicon example of an LTE-class receiver chain uses hardware-in-the-loop simulation (HILS) for quantifying the in-band spurs due to noise coupling and measuring their impact on system-level communication performance such as error vector magnitude (EVM) and data throughput.

Instructor: Makoto Nagata

Makoto Nagata received the B.S. and M.S. degrees in physics from Gakushuin University, Tokyo, Japan, in 1991 and 1993, respectively, and the Ph.D. in electronics engineering from Hiroshima University in 2001. He is currently a Professor of the Graduate School of System Informatics, Kobe University. His research interests include design techniques for high-performance mixed analog, RF, and digital VLSI systems, with particular emphasis on power/signal/substrate integrity and electromagnetic compatibility, testing and diagnosis, 3D system integration, as well as connectivity and security applications. He is currently a member of the ISSCC-ITPC and was a Program Chair (2010-2011) and a Symposium Chair (2012-2013) for the Symposium on VLSI Circuits.

T9: Circuit Design for Low-Power Wireless Applications

The continued rapid expansion in low-power, short-range wireless communications requires a different approach to RFIC design. Maintaining functionality while cutting power below 1mW requires a revision of everything from system-level decisions down to basic circuit-design choices. System choices like modulation type and duty-cycling should be co-designed with critical circuits. Since power is limited by blocks such as RF oscillators, amplifiers, modulators and demodulators, optimization is required to reduce power in these circuits, and even to eliminate them when possible. This tutorial will provide an overview of some popular system and architecture approaches and the circuit techniques that enable them.

Instructor: Alyosha Molnar

Alyosha Molnar received his BS from Swarthmore College in 1997, and worked for Conexant Systems from 1998-2001 as an RFIC design engineer, where he jointly developed their first-generation direct-conversion receiver for the GSM cellular standard. Starting graduate school at U.C. Berkeley in 2001, Molnar worked on early, ultra-low-power radio transceivers for wireless sensor networks, and then joined a retinal neurophysiology group, where he worked on dissecting the structure and function of neural circuits in the mammalian retina. He joined the Faculty at Cornell University in 2007, and presently works on software-defined radios, neural interface circuits, and integrated imaging techniques.

T10: Circuit Design Considerations for Implantable Devices

Implantable devices are a unique area for circuit designers. A comprehensive understanding of design trade-offs at the system level is important to ensure device success. The goal of this tutorial is to provide knowledge to CMOS circuit designers with limited biomedical background to understand design challenges and trade-offs for implantable devices. Besides system-level design, examples of topics in this tutorial include RF powering/recharging circuits with hermetic and non-hermetic packaging, communication schemes for data telemetry, tissue interface modeling and circuit techniques to deal with electrode artifacts, signal acquisition circuits including low-power low-noise amplifiers and ADCs, and signal conditioning including both analog and digital approaches.

Instructor: Peng Cong

Peng Cong received the Ph.D. degree from the Department of Electrical Engineering and Computer Science at Case Western Reserve University, Cleveland, OH, in 2008. He then joined Medtronic Neuromodulation Core Technology, where he worked on next-generation implantable devices with concurrent sensing and therapeutic capabilities. In September 2014, he joined Google Life Sciences to explore innovations for healthcare systems. Dr. Cong's research interests are in sensor interfaces, analog integrated circuit design, sensors, microsystems, as well as system integration for wearable and implantable medical devices. He currently serves on the program committees for ISSCC and ESSCIRC.

F1: Designing Secure Systems: Manufacturing, Circuits and Architectures

Organizer: **Vivek De,** *Intel, Hillsboro, OR*
Committee: **Kerry Bernstein,** *DARPA, Arlington, VA*
Takefumi Yoshikawa, *National Institute of Technology, Nagano College, Nagano, Japan*
Yusuf Leblebici, *Swiss Federal Institute of Technology, Lausanne, Switzerland*
Marian Verhelst, *KU Leuven, Heverlee, Belgium*
Mahesh Mehendale, *Texas Instruments, Bangalore, India*
Makoto Nagata, *Kobe University, Kobe, Japan*

Hardware security in server, client, mobile and embedded systems is becoming increasingly critical, especially with the rapid growth of the Internet-of-Everything (IoE). Security threats and vulnerabilities for all hardware components must be addressed. This forum brings together chip designers and system architects to discuss: (1) design, hardware and logistics attack challenges, as well as advanced mitigation and prevention techniques across the entire chip design, validation, manufacturing and test pipeline including EDA for the foundry and fabless design ecosystem, and (2) data and operational security challenges and efficient cryptographic countermeasures for systems ranging from large cloud datacenters to compact lightweight embedded IoE devices. The first speaker provides an overview of hardware security challenges. The second speaker summarizes security attack challenges and solutions in the foundry and fabless manufacturing and design ecosystem. Two speakers then discuss key security circuit building blocks and cryptographic hardware accelerators. An overview of protections against IC counterfeiting and cloning, as well as hardware Trojans, is provided by the fifth speaker. Circuit techniques for detection, mitigation and preemptive countermeasures against passive and active side-channel attacks are discussed by the sixth speaker. The last two speakers present security hardware architectures for IoE platforms and cloud data centers.

Forum Agenda

Time:	Topic:
8:00 AM	Breakfast
8:20 AM	Introduction by Chair
8:30 AM	**A Matter of Trust: Overview of Hardware Security Challenges** ***Kerry Bernstein,*** *DARPA, Arlington, VA*
9:20 AM	**Ecosystem of Design for Security** ***Hsien-Hsin Sean Lee,*** *TSMC, Hsinchu, Taiwan*
10:10 AM	Break
10:35 AM	**Circuit Building Blocks for Security Technologies** ***Sanu Mathew,*** *Intel, Hillsboro, OR*
11:25 AM	**Cryptographic Hardware Accelerators** ***Ingrid Verbauwhede,*** *KU Leuven, Heverlee, Belgium*
12:15 PM	Lunch
1:20 PM	**Overview of Protections Against IC Counterfeiting and Hardware Trojan Horses** ***Jean-Luc Danger,*** *Télécom Paristech, Paris, France*
2:10 PM	**Side-Channel-Aware Circuit Design: Detection and Prevention of Side-Channel Attacks** ***Naofumi Homma,*** *Tohoku University, Sendai, Japan*
3:00 PM	Break
3:20 PM	**You Can't Trust Big Data Unless You Can Trust Little Data: Ultra-Lightweight Security for IoT** ***Rob Aitken,*** *ARM, San Jose, CA*
4:10 PM	**Hardware Architectures for End-to-End Security in Cloud Data Centers** ***Dimitrios Pendarakis,*** *IBM T.J. Watson Research Group, Yorktown Heights, NY*
5:00 PM	Closing remarks by Chair

F2: Data-Converter Calibration and Dynamic-Matching Techniques

Organizer: **Kostas Doris ,** *NXP, Eindhoven, The Netherlands*

Committee: **Alyosha Molnar,** *Cornell University, Ithaca, NY*
Xicheng Jiang, *Broadcom, Irvine, CA*
Seung-Tak Ryu, *KAIST, Daejeon, Korea*

This forum covers the greatest calibration and dynamic matching techniques for data converters, showing the way these have changed modern transceivers and applications.

Experts in the field will give an overview of the most widely used and best mixed-signal/digital calibration techniques and dynamic-element-matching methods in Nyquist and oversampled AD/DA converters, such as offset calibration, gain matching, linearity enhancement, I/Q matching improvement, and use of redundancy.

What are the tradeoffs between analog vs. digital corrections, what role does technology play, and what are the differences between standalone vs. application-specific calibrations? What should we expect to see in the future? The forum makes a link between what is calibrated, the associated architecture elements of the Data Converter and receiver or transmitter, and the requirements of the application that connects them.

Forum Agenda

Time:	Topic:
8:00 AM	Breakfast
8:30 AM	**Calibration and Dynamic Matching in Data Converters** ***Kenneth Dyer, John Keane,*** *Keysight Technologies, Santa Clara, CA,* *and* ***Stephen Lewis,*** *University of California, Davis, CA*
9:20 AM	**System Calibrations in Wireless Tranceivers** ***Theodoros Georgantas,*** *Broadcom, Athens, Greece*
10:10 AM	Break
10:35 AM	**Advanced Calibration Techniques for High-Speed and High-Resolution ADCs** ***Ahmed Ali,*** *Analog Devices, Greensboro, NC*
11:25 AM	**Calibration and Dynamic Element Matching for Delta-Sigma Modulators in Wireless Receivers** ***Lucien Breems,*** *NXP, Eindhoven, The Netherlands*
12:15 PM	Lunch
1:20 PM	**Digitally Assisted Analog in Radar and Electronic Warfare Applications** ***Simran Singh,*** *Airbus Defence and Space, Ulm, Germany*
2:10 PM	**Calibrations and Dynamic-Matching Techniques in High-Speed High-Resolution Digital-to-Analog Converters** ***Joost Briaire,*** *Aquantia, Eindhoven, The Netherlands*
3:00 PM	Break
3:20 PM	**Self-Calibration Techniques for Precision Sensing Applications** ***Fabio Sebastiano,*** *Delft University, The Netherlands*
4:10 PM	**Panel Discussion** **All speakers**
5:00 PM	Closing remarks

ES1: STUDENT RESEARCH PREVIEW (SRP)

The Student Research Preview (SRP) will highlight selected student research projects in progress. The SRP consists of 25 one-minute presentations followed by a Poster Session, by graduate students from around the world, which have been selected on the basis of a short submission concerning their on-going research. Selection is based on the technical quality and innovation of the work. This year, the SRP will be presented in three theme sections: Analog and Mixed-Signal Circuits, Biomedical Systems and Processors, RF & Wireless Techniques.

The Student Research Preview will begin with a brief talk by a distinguished member of the solid-state circuit community, Professor Rinaldo Castello of the University of Pavia, Italy.

His remarks are scheduled for Sunday, January 31st, starting at 7:30 pm. SRP is open to all ISSCC registrants.

Chair:	Jan Van der Spiegel	University of Pennsylvania
Co-Chair:	SeongHwan Cho	KAIST
Secretary:	Denis Daly	Maxim Integrated
Advisor:	Kenneth Smith	University of Toronto
Media/Publications:	Laura Fujino	University of Toronto
A/V:	Trudy Stetzler	

Committee Members

Bryan Ackland	Stevens Inst. of Technology
Andrea Baschirotto	University of Milan-Bicocca
William Bowhill	Intel, USA
SeongHwan Cho	KAIST
Denis Daly	Maxim Integrated
Andreas Demosthenous	University College London, UK
Vincent Gaudet	University of Waterloo
Manish Goel	Samsung Research America, USA
Chun-Huat Heng	National University Of Singapore
Makoto Ikeda	University of Tokyo
Jaeha Kim	Seoul National University
Joyce Kwong	TI
Qiang Li	University Electr. Sc. & Tech., China
Tsung-Hsien Lin	National Taiwan University
Shahriar Mirabbasi	University of British Columbia
Tinoosh Mohsenin	University of Maryland
Cormac O'Connell	TSMC, Canada
Mondira Pant	Intel, USA
Nils Pohl	Ruhr-University, Bochum, Germany
Patrick Reynaert	University of Leuven, Belgium
Bing Sheu	National Chiao Tung University, Taiwan
Jan Van der Spiegel	University of Pennsylvania
GuoXing Wang	Shanghai Jiao Tong University
Jeffrey Weldon	CMU
Peter Wu	National Chiao Tung University
Jerald Yoo	Masdar Inst. Sc. & Tech.

ES2: Computing Architectures Paving the Path to Power Efficiency

Organizers **Dejan Markovic,** *University of California, Los Angeles, CA*
Antoine Dupret, *CEA, Gif-sur-Yvette, France*
Atsuki Inoue, *Fujitsu, Kawasaki, Japan*

Chair: **Dejan Markovic,** *University of California, Los Angeles, CA*

As the benefits of CMOS feature size scaling (Moore and Dennard) are coming to an end, there is an emerging need to re-architect computing systems from the ground up. Will quantum and neuro-inspired computers outperform conventional architectures? Will heterogeneous system architectures become mainstream? What will future memories look like? In this evening session, a group of experts will share their views on architectural innovations that will shape the future of computing.

Time	Topic
8:00 PM	**A Tour of a Modern SoC, its Engines, Architecture and Challenges** **Joe Macri,** *AMD, Austin, TX*
8:24 PM	**The Rebirth of Neuromorphic Accelerators: A Step Towards a New Generation of More Intelligent Machines?** **Marc Duranton,** *CEA-Leti, Gif-sur-Yvette, France*
8:48 PM	**Heterogeneous Computing in Datacenter with FPGAs** **Sailesh Kottapalli,** *Intel, Santa Clara, CA*
9:12 PM	**Rethinking Memory Architecture** **Dean Klein,** *Micron Technology, Boise, ID*
9:36 PM	**CMOS Ising Chip for Combinatorial Optimization Problem** **Masanao Yamaoka,** *Hitachi, Tokyo, Japan*

Plenary Session — Invited Papers

Chair: ***Anantha Chandrakasan,*** *Massachusetts Institute of Technology, Cambridge, MA*
ISSCC Conference Chair

Associate Chair: ***Kevin Zhang,*** *Intel, Hillsboro, OR*
ISSCC International Technical-Program Chair

FORMAL OPENING OF THE CONFERENCE **8:30 AM**

1.1 Moore's Law: A Path Forward **8:45 AM**
William M. Holt, *Executive Vice-President and General Manager, Technology and Manufacturing Group, Intel Corporation, Hillsboro, Oregon*

Moore's Law has served as the guiding principle for the semiconductor industry for 50 years. But now there are growing concerns and doubts over the vitality of Moore's Law going forward, given the scaling challenges we face. This talk will directly address those concerns and explore future opportunities for the industry. We will present the scaling benefits for power, performance, and cost using specific product and design examples based on state-of-the-art 14nm CMOS technology, for applications ranging from high-performance computing down to ultra-low-power mobile applications. In additional to the scaling path of CMOS technology beyond 14nm, this talk will also discuss some leading technology options on the horizon beyond CMOS and their potential design benefits in advancing Moore's Law well into the future. Novel 3D heterogeneous integration schemes and new memory technologies will be discussed for their potential in optimizing the memory hierarchy and addressing bandwidth challenges in processor performance and power.

1.2 Three Pillars Enabling the Internet of Everything: Smart Everyday Objects, Information-Centric Networks, and Automated Real-Time Insights **9:20 AM**
Sophie V. Vandebroek, *Chief Technology Officer, Xerox Corporation, Norwalk, CT*

When smart everyday objects, information-centric networks, and automated real-time insights work in concert a "perfect storm" of functionality emerges, one which will disrupt entire industries: Gartner predicts that the global economic value of the Internet of Everything (IoE) will be $1.7T in 2020. But, even more important will be the inevitable improvements to human society that IoE enables: personalized healthcare and education, agile urban mobility, efficient energy usage, and much more.

This talk will provide examples of how each of the three pillars of IoE relies on electronics: (1) printed hybrid logic and sensor circuits using organic inks and inks embedding microchips to create smart 2D labels and to manufacture 3D personalized Internet-connected objects; (2) information-centric network protocols and hardware (for example, CCNx®) to increase the Internet's versatility, reduce its traffic congestion, improve security, and simplify application development; and (3) machine-intelligence software and deep-learning chips to create real-time insights and automate processes at the "edge" of the IoE network.

The three pillars of IoE will be illustrated through examples from healthcare and transportation. A number of unique challenges and opportunities for general-purpose and custom chip designs will be highlighted.

ISSCC, SSCS, IEEE AWARD PRESENTATIONS **9:55 AM**

BREAK **10:20 AM**

1.3 The Evolution of 5G Mobile Technology Toward 2020 and Beyond **10:45 AM**
Seizo Onoe, *Executive Vice President and CTO, NTT DOCOMO, Tokyo, Japan*

Recently, LTE has become the mainstream of mobile technologies; correspondingly, global expectations for 5G are rapidly growing toward 2020 and beyond. Up to the generation of 4G, a representative technology for each generation emerged immediately after the commercial launch of the previous one; However, today, while everyone talks about 5G, there is no single technology representing it. Although researchers see some saturation in the evolution of radio, combinations of existing technologies will continue to create new possibilities and solutions. Thus, through such combinations, developments that are considered impossible today will be achieved in the 5G era. For example, cellular systems will provide cost-effective solutions with wide coverage at even higher frequencies with broader bandwidth. In this talk, the history of mobile-system evolution up to 5G will be reviewed. Then discussion will turn to 5G definition, its requirements, its technologies, and their coverage for variable use cases and spectrum bands. Finally, DOCOMO's recent R&D activities targeting a 5G commercial launch in 2020 will be described.

1.4 The Road Ahead for Securely Connected Cars **11:15 AM**
Lars Reger, *CTO Automotive, NXP Semiconductors, Hamburg, Germany* **DS1**

The car is evolving: It is transforming from simply a mode of transport to a mobile personalized-information hub! Cars are enabling consumers to seamlessly integrate their mobile and wearable devices, and soon they will be able to operate autonomously.

The technologies that make autonomous driving a reality are clearly on the rise; they include secure vehicle-to-everything (V2X) communications, affordable compact radar detection, and Ethernet for high-bandwidth in-car data transfer.

As well, self-driving cars will integrate a variety of wireless interfaces for exchanging data with other vehicles and the surrounding intelligent traffic infrastructure – all aimed at understanding the world around to optimize the traffic flow, reduce CO2 emissions, and avoid accidents. While providing an essential element of autonomous driving, this connectivity also exposes cars to vulnerabilities such as hackers and viruses.

Powerful reliable wireless technologies combined with the highest-level privacy and system security are critical. This talk will discuss what it takes to realize the secure connected car of the future.

PRESENTATION TO PLENARY SPEAKERS **11:50 AM**

CONCLUSION **11:55 AM**

RF Frequency Synthesis Techniques

Session Chair: ***Ahmad Mirzaei,*** *Broadcom, Irvine, CA*
Associate Chair: ***Hyunchol Shin,*** *Kwangwoon University, Seoul, Korea*

1:30 PM

2.1 DS1 An Integrated 0.56THz Frequency Synthesizer with 21GHz Locking Range and -74dBc/Hz Phase Noise at 1MHz Offset in 65nm CMOS
Y. Zhao[1], Z-Z. Chen[1], G. Virbila[1], Y. Xu[1], R. Al Hadi[1], Y. Kim[1,2], A. Tang[1,2], T. Reck[2], H-N. Chen[3], C. Jou[3], F-L. Hsueh[3], M-C. F. Chang[1,4]
[1]University of California, Los Angeles, CA; [2]Jet Propulsion Laboratory, Pasadena, CA
[3]TSMC, Hsinchu, Taiwan; [4]National Chiao Tung University, Hsinchu, Taiwan

2:00 PM

2.2 A Scalable 28GHz Coupled-PLL in 65nm CMOS with Single-Wire Synchronization for Large-Scale 5G mm-Wave Arrays
A. Agrawal, A. Natarajan, Oregon State University, Corvallis, OR

2:30 PM

2.3 A 4.2µs-Settling-Time 3rd-Order 2.1GHz Phase-Noise-Rejection PLL Using a Cascaded Time-Amplified Clock-Skew Sub-Sampling DLL
Z. Huang[1], B. Jiang[1], L. Li[2], H. C. Luong[1]
[1]Hong Kong University of Science and Technology, Hong Kong, China
[2]Southeast University, Nanjing, China

Break 3:00 PM

3:15 PM

2.4 A 2-to-16GHz BiCMOS ΔΣ Fractional-N PLL Synthesizer with Integrated VCOs and Frequency Doubler for Wireless Backhaul Applications
T. Copani, C. Asero, M. Colombo, P. Aliberti, G. Martino, F. Clerici
STMicroelectronics, Catania, Italy

3:45 PM

2.5 A Complementary VCO for IoE that Achieves a 195dBc/Hz FOM and Flicker Noise Corner of 200kHz
D. Murphy, H. Darabi, Broadcom, Irvine, CA

4:00 PM

2.6 A 190.5GHz Mode-Switching VCO with 20.7% Continuous Tuning Range and Maximum Power of -2.1dBm in 0.13µm BiCMOS
R. Kananizadeh, O. Momeni, University of California, Davis, CA

4:15 PM

2.7 A 0.003mm² 1.7-to-3.5GHz Dual-Mode Time-Interleaved Ring-VCO Achieving 90-to-150kHz 1/f³ Phase-Noise Corner
J. Yin[1], P-I. Mak[1], F. Maloberti[2], R. P. Martins[1,3]
[1]University of Macau, Macau, China; [2]University of Pavia, Pavia, Italy
[3]Instituto Superior Tecnico, Lisbon, Portugal

4:30 PM

2.8 A Mixed-Mode Injection Frequency-Locked Loop for Self-Calibration of Injection Locking Range and Phase Noise in 0.13µm CMOS
D. Shin, S. Raman, K-J. Koh; Virginia Tech, Blacksburg, VA

4:45 PM

2.9 A 2GHz 244fs-Resolution 1.2ps-Peak-INL Edge-Interpolator-Based Digital-to-Time Converter in 28nm CMOS
S. Sievert[1], O. Degani[2], A. Ben-Bassat[2], R. Banin[2], A. Ravi[3], B-U. Klepser[1], Z. Boos[1], D. Schmitt-Landsiedel[4]
[1]Intel, Neubiberg, Germany; [2]Intel, Haifa, Israel; [3]Intel, Hillsboro, OR
[4]Technische Universität München, Munich, Germany

Conclusion 5:15 PM

Ultra-High-Speed Transceivers

Session Chair: ***Hyeon-Min Bae,*** *KAIST, Daejeon, Korea*

Associate Chair: ***Ajith Amerasekera,*** *Texas Instruments, Dallas, TX*

1:30 PM

3.1 A 25Gb/s ADC-Based Serial Line Receiver in 32nm CMOS SOI

S. Rylov[1], T. Beukema[1], Z. Toprak-Deniz[1], T. Toifl[2], Y. Liu[3], A. Agrawal[1], P. Buchmann[2], A. Rylyakov[4], M. Beakes[1], B. Parker[1], M. Meghelli[1]

[1]IBM T. J. Watson Reseach Center, Yorktown Heights, NY
[2]IBM Zurich Research Laboratory, Rüschlikon, Switzerland
[3]now with Shanghai Jiao Tong University, Shanghai, China
[4]now with Coriant Advanced Technology Group, New York, NY

2:00 PM

3.2 A 320mW 32Gb/s 8b ADC-Based PAM-4 Analog Front-End with Programmable Gain Control and Analog Peaking in 28nm CMOS

D. Cui[1], H. Zhang[1], N. Huang[1,2], A. Nazemi[1], B. Catli[1], H. G. Rhew[1], B. Zhang[1], A. Momtaz[1], J. Cao[1]

[1]Broadcom, Irvine, CA; [2]now with Apple, Cupertino, CA

2:30 PM

3.3 A 25Gb/s Multistandard Serial Link Transceiver for 50dB-Loss Copper Cable in 28nm CMOS DS1

T. Norimatsu[1], T. Kawamoto[1], K. Kogo[1], N. Kohmu[1], F. Yuki[1], N. Nakajima[2], T. Muto[2], J. Nasu[2], T. Komori[2], H. Koba[2], T. Usugi[2], T. Hokari[2], T. Kawamata[2], Y. Ito[2], S. Umai[2], M. Tsuge[2], T. Yamashita[2], M. Hasegawa[2], K. Higeta[2]

[1]Hitachi, Tokyo, Japan; [2]Hitachi, Kanagawa, Japan

Break 3:00 PM

3:15 PM

3.4 A 40/50/100Gb/s PAM-4 Ethernet Transceiver in 28nm CMOS

K. Gopalakrishnan[1], A. Ren[1], A. Tan[1], A. Farhood[1], A. Tiruvur[1], B. Helal[1], C-F. Loi[2], C. Jiang[1], H. Cirit[1], I. Quek[2], J. Riani[1], J. Gorecki[1], J. Wu[1], J. Pernillo[1], L. Tse[1], M. Le[3], M. Ranjbar[1], P-S. Wong[1], P. Khandelwal[1], R. Narayanan[1], R. Mohanavelu[1], S. Herlekar[1], S. Bhoja[1], V. Shvydun[1]

[1]Inphi, Santa Clara, CA; [2]Inphi, Singapore, Singapore; [3]Inphi, Irvine, CA

3:45 PM

3.5 A 56Gb/s NRZ Electrical 247mW/lane Serial Link Transceiver in 28nm CMOS DS1

T. Shibasaki[1], T. Danjo[1], Y. Ogata[1], Y. Sakai[1], H. Miyaoka[2], F. Terasawa[2], M. Kudo[2], H. Kano[2], A. Matsuda[2], S. Kawai[2], T. Arai[2], H. Higashi[2], N. Naka[2], H. Yamaguchi[1], T. Mori[1], Y. Koyanagi[1], H. Tamura[1]

[1]Fujitsu Laboratories, Kawasaki, Japan; [2]Socionext, Yokohama, Japan

4:15 PM

3.6 A 45Gb/s PAM-4 Transmitter Delivering 1.3V_{ppd} Output Swing with 1V Supply in 28nm CMOS FDSOI

M. Bassi[1], F. Radice[2], M. Bruccoleri[2], S. Erba[3], A. Mazzanti[1]

[1]University of Pavia, Pavia, Italy; [2]STMicroelectronics, Cornaredo, Italy
[3]STMicroelectronics, Pavia, Italy

4:45 PM

3.7 A 40-to-64Gb/s NRZ Transmitter with Supply-Regulated Front-End in 16nm FinFET DS1

Y. Frans, S. McLeod, H. Hedayati, M. Elzeftawi, J. Namkoong, W. Lin, J. Im, P. Upadhyaya, K. Chang

Xilinx, San Jose, CA

Conclusion 5:15 PM

Digital Processors

Session Chair: ***Mahesh Mehendale,*** *Texas Instruments, Bangalore, India*
Associate Chair: ***Luke Jinuk Shin,*** *Oracle, San Jose, CA*

1:30 PM

4.1 14nm 6th-Generation Core Processor SoC with Low Power Consumption and Improved Performance
E. Fayneh, M. Yuffe, E. Knoll, M. Zelikson, M. Abozaed, Y. Talker, Z. Shmuely, S. Abu Rahme, Intel, Haifa, Israel

2:00 PM

4.2 Increasing the Performance of a 28nm x86-64 Microprocessor Through System Power Management
A. Grenat[1], S. Sundaram[1], S. Kosonocky[2], R. Rachala[1], S. Sambamurthy[1], S. Liepe[2], M. Rodriguez[2], T. Burd[3], A. Clark[4], M. Austin[1], S. Naffziger[2]
[1]AMD, Austin, TX; [2]AMD, Fort Collins, CO;
[3]AMD, Sunnyvale, CA; [4]AMD, Markham, Canada

2:30 PM

4.3 A 20nm 2.5GHz Ultra-Low-Power Tri-Cluster CPU Subsystem with Adaptive Power Allocation for Optimal Mobile SoC Performance
H. T. Mair[1], G. Gammie[1], A. Wang[2], R. Lagerquist[1], C. Chung[1], S. Gururajarao[1], P. Kao[2], A. Rajagopalan[1], A. Saha[3], A. Jain[4], E. Wang[2], S. Ouyang[5], H. Wen[1], A. Thippana[1], H. Chen[1], S. Rahman[1], M. Chau[1], A. Varma[1], B. Flachs[1], M. Peng[2], A. Tsai[2], V. Lin[2], U. Fu[2], W. Kuo[2], L-K. Yong[2], C. Peng[2], L. Shieh[2], J. Wu[2], U. Ko[2]
[1]MediaTek, Austin, TX; [2]MediaTek, Hsinchu, Taiwan; [3]MediaTek, Singapore
[4]MediaTek, Bangalore, India; [5]MediaTek, San Jose, CA

Break 3:00 PM

3:15 PM

4.4 DS1 A 197mW 70ms-Latency Full-HD 12-Channel Video-Processing SoC for Car Information Systems
S. Mochizuki[1], K. Matsubara[1], K. Matsumoto[1], C. L. P. Nguyen[2], T. Shibayama[1], K. Iwata[1], K. Mizumoto[1], T. Irita[3], H. Hara[3], T. Hattori[1]
[1]Renesas System Design, Tokyo, Japan
[2]Renesas Design Vietnam, Ho Chi Minh City, Vietnam
[3]Renesas Electronics, Tokyo, Japan

3:45 PM

4.5 A 16nm FinFET Heterogeneous Nona-Core SoC Complying with ISO26262 ASIL-B: Achieving 10^{-7} Random Hardware Failures per Hour Reliability
C. Takahashi[1], S. Shibahara[1], K. Fukuoka[1], J. Matsushima[1], Y. Kitaji[1], Y. Shimazaki[2], H. Hara[2], T. Irita[2]
[1]Renesas System Design, Tokyo, Japan; [2]Renesas Electronics, Tokyo, Japan

4:15 PM

4.6 A 65nm CMOS 6.4-to-29.2pJ/FLOP@0.8V Shared Logarithmic Floating Point Unit for Acceleration of Nonlinear Function Kernels in a Tightly Coupled Processor Cluster
M. Gautschi[1], M. Schaffner[1], F. K. Gürkaynak[1], L. Benini[1,2]
[1]ETH Zurich, Zurich, Switzerland; [2]University of Bologna, Bologna, Italy

4:45 PM

4.7 A 65nm ReRAM-Enabled Nonvolatile Processor with 6× Reduction in Restore Time and 4× Higher Clock Frequency Using Adaptive Data Retention and Self-Write-Termination Nonvolatile Logic
Y. Liu[1], Z. Wang[1], A. Lee[2,3], F. Su[1], C-P. Lo[2], Z. Yuan[1], C-C. Lin[2], Q. Wei[1], Y. Wang[1], Y-C. King[2], C-J. Lin[2], P. Khalili[3], K-L. Wang[3], M-F. Chang[2], H. Yang[1]
[1]Tsinghua University, Beijing, China; [2]National Tsing Hua University, Hsinchu,Taiwan
[3]University of California, Los Angeles, CA

Conclusion 5:15 PM

Analog Techniques

Session Chair: ***Marco Berkhout,*** *NXP Semiconductors, Nijmegen, The Netherlands*
Associate Chair: ***Tim Piessens,*** *ICsense, Leuven, Belgium*

1:30 PM

5.1 A 10MHz-Bandwidth 4µs-Large-Signal-Settling 6.5nV/√Hz-Noise 2µV-Offset Chopper Operational Amplifier
V. Ivanov, M. Shaik, Texas Instruments, Tucson, AZ

2:00 PM

5.2 A 118dB-PSRR 0.00067%(-103.5dB) THD+N and 3.1W Fully Differential Class-D Audio Amplifier with PWM Common-Mode Control
W-C. Wang, Y-H. Lin, MediaTek, Hsinchu, Taiwan

2:30 PM

5.3 A 2×70W Monolithic Five-Level Class-D Audio Power Amplifier
DS1
M. Høyerby[1], J. K. Jakobsen[1], J. Midtgaard[1], T. H. Hansen[1], A. N. Nielsen[1,2], H. Hasselby-Andersen[1]
[1]Merus Audio, Herlev, Denmark; [2]now at Knowles Corporation, Roskilde, Denmark

Break 3:00 PM

3:15 PM

5.4 A Sub-µW 36nV/√Hz Chopper Amplifier for Sensors Using a Noise-Efficient Inverter-Based 0.2V-Supply Input Stage
DS1
F. M. Yaul, A. P. Chandrakasan
Massachusetts Institute of Technology, Cambridge, MA

3:30 PM

5.5 A 2µW 40mV$_{pp}$ Linear-Input-Range Chopper-Stabilized Bio-Signal Amplifier with Boosted Input Impedance of 300MΩ and Electrode-Offset Filtering
H. Chandrakumar, D. Marković, University of California, Los Angeles, CA

3:45 PM

5.6 A 420µW 100GHz-GBW CMOS Programmable-Gain Amplifier Leveraging the Cross-Coupled Pair Regeneration
M. Sautto[1], F. Quaglia[2], G. Ricotti[2], A. Mazzanti[1]
[1]University of Pavia, Pavia, Italy; [2]STMicroelectronics, Cornaredo, Italy

4:00 PM

5.7 A 39.25MHz 278dB-FOM 19µW LDO-Free Stacked-Amplifier Crystal Oscillator (SAXO) Operating at I/O Voltage
S. Iguchi, T. Sakurai, M. Takamiya, University of Tokyo, Tokyo, Japan

4:15 PM

5.8 A 4.7nW 13.8ppm/°C Self-Biased Wakeup Timer Using a Switched-Resistor Scheme
T. Jang, M. Choi, S. Jeong, S. Bang, D. Sylvester, D. Blaauw
University of Michigan, Ann Arbor, MI

4:45 PM

5.9 A 24MHz Crystal Oscillator with Robust Fast Start-Up Using Dithered Injection
D. Griffith[1], J. Murdock[1], P. T. Røine[2], [1]Texas Instruments, Dallas, TX
[2]Texas Instruments, Oslo, Norway

5:00 PM

5.10 A 1.4V 10.5MHz Swing-Boosted Differential Relaxation Oscillator with 162.1dBc/Hz FOM and 9.86ps$_{rms}$ Period Jitter in 0.18µm CMOS
J. Lee[1], A. George[1,2,3], M. Je[2]
[1]Institute of Microelectronics, Singapore
[2]Daegu Gyeongbuk Institute of Science and Technology, Daegu, Korea
[3]Nanyang Technological University, Singapore

Conclusion 5:15 PM

Image Sensors

Session Chair: ***Jun Deguchi,*** *Toshiba, Kawasaki, Japan*
Associate Chair: ***David Stoppa,*** *Fondazione Bruno Kessler, Trento, Italy*

1:30 PM

6.1 DS1 **An Over 120dB Simultaneous-Capture Wide-Dynamic-Range 1.6e⁻ Ultra-Low-Reset-Noise Organic-Photoconductive-Film CMOS Image Sensor**
K. Nishimura, Y. Sato, J. Hirase, R. Sakaida, M. Yanagida, T. Tamaki, M. Takase, H. Kanehara, M. Murakami, Y. Inoue, Panasonic, Moriguchi, Japan

2:00 PM

6.2 DS1 **210ke⁻ Saturation Signal 3µm-Pixel Variable-Sensitivity Global-Shutter Organic Photoconductive Image Sensor for Motion Capture**
S. Shishido, Y. Miyake, Y. Sato, T. Tamaki, N. Shimasaki, Y. Sato, M. Murakami, Y. Inoue, Panasonic, Moriguchi, Japan

2:15 PM

6.3 **105×65mm² 391Mpixel CMOS Image Sensor with >78dB Dynamic Range for Airborne Mapping Applications**
J. Bogaerts, R. Lafaille, M. Borremans, J. Guo, B. Ceulemans, G. Meynants, N. Sarhangnejad, G. Arsinte, V. Statescu, S. van der Groen, CMOSIS NV, Antwerp, Belgium

2:30 PM

6.4 **An APS-H-Size 250Mpixel CMOS Image Sensor Using Column Single-Slope ADCs with Dual-Gain Amplifiers**
H. Totsuka, T. Tsuboi, T. Muto, D. Yoshida, Y. Matsuno, M. Ohmura, H. Takahashi, K. Sakurai, T. Ichikawa, H. Yuzurihara, S. Inoue, Canon, Kawasaki, Japan

Break 3:00 PM

3:15 PM

6.5 DS1 **A 64×64-Pixel Digital Silicon Photomultiplier Direct ToF Sensor with 100MPhotons/s/pixel Background Rejection and Imaging/Altimeter Mode with 0.14% Precision up to 6km for Spacecraft Navigation and Landing**
M. Perenzoni, D. Perenzoni, D. Stoppa, Fondazione Bruno Kessler, Trento, Italy

3:45 PM

6.6 **A 1280×720 Single-Photon-Detecting Image Sensor with 100dB Dynamic Range Using a Sensitivity-Boosting Technique**
M. Mori, Y. Sakata, M. Usuda, S. Yamahira, S. Kasuga, Y. Hirose, Y. Kato, T. Tanaka
Panasonic, Nagaokakyo, Japan

4:00 PM

6.7 DS1 **A 1.2e⁻ Temporal Noise 3D-Stacked CMOS Image Sensor with Comparator-Based Multiple-Sampling PGA**
K. Shiraishi, Y. Shinozuka, T. Yamashita, K. Sugiura, N. Watanabe, R. Okamoto, T. Ashitani, M. Furuta, T. Itakura, Toshiba, Kawasaki, Japan

4:15 PM

6.8 **A 1.5V 33Mpixel 3D-Stacked CMOS Image Sensor with Negative Substrate Bias**
C. C-M. Liu, M. M. Mhala, C-H. Chang, H. Tu, P-S. Chou, C. Chao, F-L. Hsueh
TSMC, Hsinchu, Taiwan

4:45 PM

6.9 DS1 **A 1.1µm 33Mpixel 240fps 3D-Stacked CMOS Image Sensor with 3-Stage Cyclic-Based Analog-to-Digital Converters**
T. Arai[1], T. Yasue[1], K. Kitamura[1], H. Shimamoto[1], T. Kosugi[2], S. Jun[2], S. Aoyama[2], M-C. Hsu[3], Y. Yamashita[3], H. Sumi[3], S. Kawahito[2,4]
[1]NHK Science & Technology Research Laboratories, Tokyo, Japan
[2]Brookman Technology, Hamamatsu, Japan
[3]TSMC, Hsinchu, Taiwan; [4]Shizuoka University, Hamamatsu, Japan

Conclusion 5:15 PM

Demonstration Session 1, Monday February 1st, 5:00-7:00 PM

This year, the Demonstration Session extending in selected regular papers, both Academic and Industrial, will take place on Monday February 1st, and Tuesday February 2nd, from 5 pm until 7 pm in the Golden Gate Hall. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2016, as noted by the symbol **DS1**

Monday, February 1st

11:15 AM

1.4 The Road Ahead for Securely Connected Cars

1:30 PM

2.1 An Integrated 0.56THz Frequency Synthesizer with 21GHz Locking Range and -74dBc/Hz Phase Noise at 1MHz Offset in 65nm CMOS

2:30 PM

3.3 A 25Gb/s Multistandard Serial Link Transceiver for 50dB-Loss Copper Cable in 28nm CMOS

3:45 PM

3.5 A 56Gb/s NRZ Electrical 247mW/lane Serial Link Transceiver in 28nm CMOS

4:45 PM

3.7 A 40-to-64Gb/s NRZ Transmitter with Supply-Regulated Front-End in 16nm FinFET

3:15 PM

4.4 A 197mW 70ms-Latency Full-HD 12-Channel Video-Processing SoC for Car Information Systems

2:30 PM

5.3 A 2×70W Monolithic Five-Level Class-D Audio Power Amplifier

3:15 PM

5.4 A Sub-μW 36nV/√Hz Chopper Amplifier for Sensors Using a Noise-Efficient Inverter-Based 0.2V-Supply Input Stage

1:30 PM

6.1 An Over 120dB Simultaneous-Capture Wide-Dynamic-Range 1.6e$^-$ Ultra-Low-Reset-Noise Organic-Photoconductive-Film CMOS Image Sensor

2:00 PM

6.2 210ke$^-$ Saturation Signal 3μm-Pixel Variable-Sensitivity Global-Shutter Organic Photoconductive Image Sensor for Motion Capture

3:15 PM

6.5 A 64×64-Pixel Digital Silicon Photomultiplier Direct ToF Sensor with 100MPhotons/s/pixel Background Rejection and Imaging/Altimeter Mode with 0.14% Precision up to 6km for Spacecraft Navigation and Landing

4:00 PM

6.7 A 1.2e$^-$ Temporal Noise 3D-Stacked CMOS Image Sensor with Comparator-Based Multiple-Sampling PGA

4:45 PM

6.9 A 1.1μm 33Mpixel 240fps 3D-Stacked CMOS Image Sensor with 3-Stage Cyclic-Based Analog-to-Digital Converters

Tuesday, February 2nd

9:00 AM

7.2 4Mb STT-MRAM-Based Cache with Memory-Access-Aware Power Optimization and Write-Verify-Write / Read-Modify-Write Scheme

8:30 AM

8.1 A 4×4×2 Homogeneous Scalable 3D Network-on-Chip Circuit with 326MFlit/s 0.66pJ/b Robust and Fault-Tolerant Asynchronous 3D Links

10:15 AM

8.4 Post-Silicon Voltage-Guard-Band Reduction in a 22nm Graphics Execution Core Using Adaptive Voltage Scaling and Dynamic Power Gating

11:30 AM

8.7 Physically Unclonable Function for Secure Key Generation with a Key Error Rate of 2E-38 in 45nm Smart-Card Chips

8:30 AM

9.1 A 45nm CMOS RF-to-Bits LTE/WCDMA FDD/TDD 2×2 MIMO Base-Station Transceiver SoC with 200MHz RF Bandwidth

9:00 AM

9.2 A Scalable 0.1-to-1.7GHz Spatio-Spectral-Filtering 4-Element MIMO Receiver Array with Spatial Notch Suppression Enabling Digital Beamforming

9:30 AM

9.3 A Very-Low-Noise Frequency-Translational Quadrature-Hybrid Receiver for Carrier Aggregation

8:30 AM

10.1 A Pin-Efficient 20.83Gb/s/wire 0.94pJ/bit Forwarded Clock CNRZ-5-Coded SerDes up to 12mm for MCM Packages in 28nm CMOS

9:00 AM

10.2 A 38mW 40Gb/s 4-Lane Tri-Band PAM-4 / 16-QAM Transceiver in 28nm CMOS for High-Speed Memory Interface

EE1: Class of 2025 – Where Will Be the Best Jobs?

Organizers: **Xicheng Jiang,** *Broadcom, Irvine, CA*
Axel Thomsen, *Cirrus Logic, Austin, TX*
Piero Malcovati, *University of Pavia, Pavia, Italy*

Moderator: **M.C. Frank Chang**, *National Chiao Tung University, Hsinchu, Taiwan*

Digital circuits have been driving the development of IC technologies for decades and they cover by far the widest share of the IC market. Analog and RF circuits, on the other hand, are essential for implementing crucial functions in electronic systems and require highly qualified and skilled designers. As a result, a widespread opinion is that there will always be request for competent analog and RF engineers, however, others argue that digital electronics is taking over and there will be little need for other disciplines. Indeed, for the past several decades, the camps of analog and digital engineers have been debating the year in which their opponents' discipline will become obsolete. On top of this there is the common misconception that analog, RF, and power electronic circuits, compared to digital and memory designs, seem to be more of a whimsical art than a systematic science. In this context, which is the best choice for students? Is it worth pursuing the whimsical art of analog electronics, or is it better to focus entirely on digital systems and software? This panel will try to answer these basic questions, exploiting the know-how of top educators and industry experts active in either the analog or the digital field.

Panelists:

Willy Sansen, *KU Leuven, Leuven, Belgium*
Jan M. Rabaey, *UC Berkeley, CA*
Lawrence Loh, *MediaTek, Taiwan*
Alessandro Piovaccari, *Silicon Labs, Austin, TX*
David Flynn, *ARM, Cambridge, United Kingdom*
Tzi-Dar Chiueh, *National Taiwan University, Taipei, Taiwan*

EE2: Do We Need to Downscale Our Radios Below 20nm?

Organizers: **Harish Krishnaswamy,** *Columbia University, New York, NY*
Jan Craninckx, *imec, Leuven, Belgium*
Tae Wook Kim, *Yonsei University, Seoul, South Korea*

Moderator: **Harish Krishnaswamy,** *Columbia University, New York, NY*

It is well known that CMOS technology scaling benefits digital circuits and systems, but creates numerous challenges for analog/RF circuit designers. Analog and RF operating frequencies have ceased to noticeably improve as wiring dominates over raw transistor performance. The shrinking supply voltage limits dynamic range while gate-leakage mismatch dominates over conventional mismatch mechanisms. As this analog-digital divide widens below the 20nm technology node, it becomes important to ask: Should we continue to downscale our radios? Do analog and RF designers need to "get with the program" and figure out how to design in radically scaled technologies? Will analog and RF circuits look increasingly "digital"? Or, will economic forces rule all, and the high cost of scaled technologies eventually dictate a two-chip "best node for the operating mode" solution?

Panelists:

Aaron Thean, *imec, Leuven, Belgium*
George Chien, *Mediatek, San Jose, CA*
Peter Kinget, *Columbia University, New York, NY*
Pietro Andreani, *Lund University, Lund, Sweden*
Thomas Byunghak Cho, *Samsung Electronics, South Korea*
Tony Montalvo, *Analog Devices, Raleigh, NC*

Nonvolatile Memory Solutions

Session Chair: ***Sungdae Choi,*** *SK hynix, Icheon, Korea*

Associate Chair: ***Jin-Man Han,*** *Samsung Electronics, Hwaseong, Korea*

8:30 AM

7.1 256Gb 3b/Cell V-NAND Flash Memory with 48 Stacked WL Layers

D. Kang, W. Jeong, C. Kim, D-H. Kim, Y. S. Cho, K-T. Kang, J. Ryu, K-M. Kang, S. Lee, W. Kim, H. Lee, J. Yu, N. Choi, D-S. Jang, J-D. Ihm, D. Kim, Y-S. Min, M-S. Kim, A-S. Park, J-I. Son, I-M. Kim, P. Kwak, B-K. Jung, D-S. Lee, H. Kim, H-J. Yang, D-S. Byeon, K-T. Park, K-H. Kyung, J-H. Choi, Samsung Electronics, Hwaseong, Korea

9:00 AM

7.2 DS1 4Mb STT-MRAM-Based Cache with Memory-Access-Aware Power Optimization and Write-Verify-Write / Read-Modify-Write Scheme

H. Noguchi[1], K. Ikegami[1], S. Takaya[1], E. Arima[2], K. Kushida[1], A. Kawasumi[1], H. Hara[1], K. Abe[1], N. Shimomura[1], J. Ito[1], S. Fujita[1], T. Nakada[2], H. Nakamura[2]

[1]Toshiba, Kawasaki, Japan; [2]University of Tokyo, Tokyo, Japan

9:30 AM

7.3 A Resistance-Drift Compensation Scheme to Reduce MLC PCM Raw BER by Over 100× for Storage-Class Memory Applications

W-S. Khwa[1,2], M-F. Chang[2], J-Y. Wu[1], M-H. Lee[1], T-H. Su[1,3], K-H. Yang[3], T-F. Chen[3], T-Y. Wang[1], H-P Li[1], M. BrightSky[4], S. Kim[4], H-L. Lung[1], C. Lam[4]

[1]Macronix International, Hsinchu, Taiwan; [2]National Tsing Hua University, Hsinchu, Taiwan

[3]National Chiao Tung University, Hsinchu, Taiwan

[4]IBM T. J. Watson Reseach Center, Yorktown Heights, NY

Break 10:00 AM

10:15 AM

7.4 A 256b-Wordlength ReRAM-based TCAM with 1ns Search-Time and 14× Improvement in WordLength-EnergyEfficiency-Density Product using 2.5T1R cell

C-C. Lin[1,2], J-Y. Hung[1], W-Z. Lin[1], C-P. Lo[1], Y-N. Chiang[1], H-J. Tsai[3], G-H. Yang[3], Y-C. King[1], C. J. Lin[1], T-F. Chen[3], M-F. Chang[1]

[1]National Tsing Hua University, Hsinchu, Taiwan; [2]TSMC, Hsinchu, Taiwan

[3]National Chiao Tung University, Hsinchu, Taiwan

10:45 AM

7.5 A 128Gb 2b/cell NAND Flash Memory in 14nm Technology with t_{PROG}=640µs and 800MB/s I/O Rate

S. Lee, J-Y. Lee, I-H. Park, J. Park, S-W. Yun, M-S. Kim, J-H. Lee, M. Kim, K. Lee, T. Kim, B. Cho, D. Cho, S. Yun, J-N. Im, H. Yim, K-H. Kang, S. Jeon, S. Jo, Y-L. Ahn, S-M. Joe, S. Kim, D-K. Woo, J. Park, H-W. Park, Y. Kim, J. Park, Y. Choi, M. Hirano, J-D. Ihm, B. Jeong, S-K. Lee, M. Kim, H. Lee, S. Seo, H. Jeon, C-H. Kim, H. Kim, J. Kim, Y. Yim, H. Kim, D-S. Byeon, H-J. Yang, K-T. Park, K-H. Kyung, J-H. Choi

Samsung Electronics, Hwaseong, Korea

11:15 AM

7.6 A 90nm Embedded 1T-MONOS Flash Macro for Automotive Applications with 0.07mJ/8kB Rewrite Energy and Endurance Over 100M Cycles Under T_j of 175°C

H. Mitani[1], K. Matsubara[1], H. Yoshida[1], T. Hashimoto[2], H. Yamakoshi[2], S. Abe[2], T. Kono[1], Y. Taito[1], T. Ito[1], T. Krafuji[1], K. Noguchi[1], H. Hidaka[1], T. Yamauchi[1]

[1]Renesas Electronics, Kodaira, Japan; [2]Renesas Electronics, Hitachinaka, Japan

11:45 AM

7.7 A 768Gb 3b/cell 3D-Floating-Gate NAND Flash Memory

T. Tanaka[1], M. Helm[2], T. Vali[3], R. Ghodsi[2], K. Kawai[1], J-K. Park[2], S. Yamada[1], F. Pan[2], Y. Einaga[1], A. Ghalam[2], T. Tanzawa[1], J. Guo[2], T. Ichikawa[1], E. Yu[2], S. Tamada[1], T. Manabe[1], J. Kishimoto[1], Y. Oikawa[1], Y. Takashima[1], H. Kuge[1], M. Morooka[1], A. Mohammadzadeh[2], J. Kang[2], J. Tsai[2], E. Sirizotti[3], E. Lee[2], L. Vu[2], Y. Liu[2], H. Choi[2], K. Cheon[2], D. Song[2], D. Shin[2], J. H. Yun[2], M. Piccardi[2], K-F. Chan[2], Y. Luthra[2], D. Srinivasan[2], S. Deshmukh[2], K. Kavalipurapu[2], D. Nguyen[2], G. Gallo[3], S. Ramprasad[2], M. Luo[2], Q. Tang[2], M. Incarnati[3], A. Macerola[3], L. Pilolli[3], L. De Santis[3], M. Rossini[3], V. Moschiano[3], G. Santin[3], B. Tronca[3], H. Lee[2], V. Patel[2], T. Pekny[2], A. Yip[2], N. Prabhu[4], P. Sule[4], T. Bemalkhedkar[4], K. Upadhyayula[4], C. Jaramillo[4]

[1]Micron, Tokyo, Japan; [2]Micron, Milpitas, CA; [3]Micron, Avezzano, Italy; [4]Intel, Folsom, CA

Conclusion 12:15 PM

Low-Power Digital Circuits

Session Chair: ***Eric Fluhr,*** *IBM, Austin, TX*

Associate Chair: ***Bing Sheu,*** *National Chiao Tung University, Hsinchu, Taiwan*

8:30 AM

8.1 A 4×4×2 Homogeneous Scalable 3D Network-on-Chip Circuit with 326MFlit/s 0.66pJ/b Robust and Fault-Tolerant Asynchronous 3D Links DS1

P. Vivet[1], Y. Thonnart[1], R. Lemaire[1], E. Beigne[1], C. Bernard[1], F. Darve[1], D. Lattard[1], I. Miro-Panades[1], C. Santos[1], F. Clermidy[1], S. Cheramy[1], F. Petrot[2], E. Flamand[3], J. Michailos[4]

[1]CEA-LETI-MINATEC, Grenoble, France; [2]Tima Laboratory, Grenoble, France
[3]STMicroelectronics, Grenoble, France; [4]STMicroelectronics, Crolles, France

9:00 AM

8.2 Fully Integrated Low-Drop-Out Regulator Based on Event-Driven PI Control

D. Kim, M. Seok, Columbia University, New York, NY

9:30 AM

8.3 A 200mA Digital Low-Drop-Out Regulator with Coarse-Fine Dual Loop in Mobile Application Processors

Y-J. Lee[1,2], M-Y. Jung[1], S. Singh[2], T-H. Kong[2], D-Y. Kim[2], K-H. Kim[2], S-H. Kim[2], J-J. Park[2], H-J. Park[2], G-H. Cho[1]

[1]KAIST, Daejeon, Korea; [2]Samsung Electronics, Hwaseong, Korea

Break 10:00 AM

10:15 AM

8.4 Post-Silicon Voltage-Guard-Band Reduction in a 22nm Graphics Execution Core Using Adaptive Voltage Scaling and Dynamic Power Gating DS1

M. Cho, S. Kim, C. Tokunaga, C. Augustine, J. Kulkarni, K. Ravichandran, J. Tschanz, M. Khellah, V. De, Intel, Hillsboro, OR

10:45 AM

8.5 A 60%-Efficiency 20nW-500μW Tri-Output Fully Integrated Power Management Unit with Environmental Adaptation and Load-Proportional Biasing for IoT Systems

W. Jung[1], J. Gu[1], P. D. Myers[1], M. Shim[2], S. Jeong[1], K. Yang[1], M. Choi[1], Z. Foo[1], S. Bang[1], S. Oh[1], D. Sylvester[1], D. Blaauw[1]

[1]University of Michigan, Ann Arbor, MI; [2]Korea University, Seoul, Korea

11:15 AM

8.6 A 6.5-to-23.3fJ/b/mm Balanced Charge-Recycling Bus in 16nm FinFET CMOS at 1.7-to-2.6Gb/s/wire with Clock Forwarding and Low-Crosstalk Contraflow Wiring

J. M. Wilson[1], M. R. Fojtik[1], J. W. Poulton[1], X. Chen[2], S. G. Tell[1], T. H. Greer III[1], C. T. Gray[1], W. J. Dally[2]

[1]Nvidia, Durham, NC; [2]Nvidia, Santa Clara, CA

11:30 AM

8.7 Physically Unclonable Function for Secure Key Generation with a Key Error Rate of 2E-38 in 45nm Smart-Card Chips DS1

B. Karpinskyy, Y. Lee, Y. Choi, Y. Kim, M. Noh, S. Lee
Samsung Electronics, Hwaseong, Korea

11:45 AM

8.8 iRazor: 3-Transistor Current-Based Error Detection and Correction in an ARM Cortex-R4 Processor

Y. Zhang[1], M. Khayatzadeh[1], K. Yang[1], M. Saligane[1], N. Pinckney[1], M. Alioto [2], D. Blaauw[1], D. Sylvester[1]

[1]University of Michigan, Ann Arbor, MI; [2]National University of Singapore, Singapore

Conclusion 12:15 PM

High-Performance Wireless

Session Chair: ***Ali Afsahi,*** *Broadcom, San Diego, CA*
Associate Chair: ***Guang-Kaai Dehng,*** *MediaTek, Hsinchu, Taiwan*

8:30 AM

9.1 DS1 A 45nm CMOS RF-to-Bits LTE/WCDMA FDD/TDD 2×2 MIMO Base-Station Transceiver SoC with 200MHz RF Bandwidth

N. Klemmer[1], S. Akhtar[1], V. Srinivasan[1], P. Litmanen[1], H. Arora[1], S. Uppathil[1], S. Kaylor[1], A. Akour[1], V. Wang[1], M. Fares[1], F. Dulger[1], A. Frank[1], D. Ghosh[1], S. Madhavapeddi[1], H. Safiri[1], J. Mehta[1], A. Jain[1], H. Choo[1], E. Zhang[1], C. Sestok[1], C. Fernando[1], R. K.A.[2], S. Ramakrishnan[2], V. Sinari[2], V. Baireddy[2]

[1]Texas Instruments, Dallas, TX; [2]Texas Instruments, Bangalore, India

9:00 AM

9.2 DS1 A Scalable 0.1-to-1.7GHz Spatio-Spectral-Filtering 4-Element MIMO Receiver Array with Spatial Notch Suppression Enabling Digital Beamforming

L. Zhang[1], A. Natarajan[2], H. Krishnaswamy[1]

[1]Columbia University, New York, NY; [2]Oregon State University, Corvallis, OR

9:30 AM

9.3 DS1 A Very-Low-Noise Frequency-Translational Quadrature-Hybrid Receiver for Carrier Aggregation

J. Zhu, P. R. Kinget, Columbia University, New York, NY

Break 10:00 AM

10:15 AM

9.4 A 2×2 WLAN and Bluetooth Combo SoC in 28nm CMOS with On-Chip WLAN Digital Power Amplifier, Integrated 2G/BT SP3T Switch and BT Pulling Cancelation

R. Winoto[1], A. Olyaei[1], M. Hajirostam[1], W. Lau[1], X. Gao[1], A. Mitra[1], O. Carnu[1], P. Godoy[1], L. Tee[1], H. Li[1], E. Erdogan[1], A. Wong[1], Q. Zhu[1], T. Loo[1], F. Zhang[1], L. Sheng[1], D. Cui[1], A. Jha[1], X. Li[1], W. Wu[1], K-S. Lee[1], D. Cheung[1], K. W. Pang[1], H. Wang[2], J. Liu[1], X. Zhao[1], D. Gangopadhyay[1], D. Cousinard[2], A. Anumula Paramanandam[1], X. Li[1], N. Liu[1], W. Xu[1], Y. Fang[1], X. Wang[1], R. Tsang[1], L. Lin[1]

[1]Marvell, Santa Clara, CA; [2]Marvell, Etoy, Switzerland

10:30 AM

9.5 A Dual-Band Digital-WiFi 802.11a/b/g/n Transmitter SoC with Digital I/Q Combining and Diamond Profile Mapping for Compact Die Area and Improved Efficiency in 40nm CMOS

Z. Deng[1], E. Lu[1], E. Rostami[1], D. Sieh[1], D. Papadopoulos[1], B. Huang[1], R. Chen[1], H. Wang[1], W. Hsu[2], C. Wu[2], O. Shanaa[1]

[1]MediaTek, San Jose, CA; [2]MediaTek, Hsinchu, Taiwan

10:45 AM

9.6 A 2.7-to-4.3GHz, 0.16ps$_{rms}$-Jitter, -246.8dB-FOM, Digital Fractional-N Sampling PLL in 28nm CMOS

X. Gao[1], O. Burg[2], H. Wang[2], W. Wu[1], C-T. Tu[2], K. Manetakis[2], F. Zhang[1], L. Tee[1], M. Yayla[1], S. Xiang[1], R. Tsang[1], L. Lin[1]

[1]Marvell, Santa Clara, CA; [2]Marvell, Etoy, Switzerland

11:15 AM

9.7 A Self-Calibrated 10Mb/s Phase Modulator with -37.4dB EVM Based on a 10.1-to-12.4GHz, -246.6dB-FOM, Fractional-N Subsampling PLL

N. Markulic[1,2], K. Raczkowski[1], E. Martens[1], P. E. Paro Filho[1,2], B. Hershberg[1], P. Wambacq[1,2], J. Craninckx[1]

[1]imec, Leuven, Belgium; [2]Vrije Universiteit Brussel, Brussels, Belgium

11:45 AM

9.8 Receiver with Integrated Magnetic-Free N-Path-Filter-Based Non-Reciprocal Circulator and Baseband Self-Interference Cancellation for Full-Duplex Wireless

J. Zhou, N. Reiskarimian , H. Krishnaswamy, Columbia University, New York, NY

Conclusion 12:15 PM

Advanced Wireline Transceivers and PLLs

Session Chair: ***Jaeha Kim,*** *Seoul National University, Seoul, Korea*
Associate Chair: ***Roberto Nonis,*** *Infineon Technologies, Villach, Austria*

8:30 AM

10.1 A Pin-Efficient 20.83Gb/s/wire 0.94pJ/bit Forwarded Clock CNRZ-5-Coded SerDes up to 12mm for MCM Packages in 28nm CMOS DS1

A. Shokrollahi[1], D. Carnelli[1], J. Fox[2], K. Hofstra[1], B. Holden[1], A. Hormati[1], P. Hunt[2], M. Johnston[1], J. Keay[2], S. Pesenti[1], R. Simpson[2], D. Stauffer[1], A. Stewart[2], G. Surace[2], A. Tajalli[1], O. Talebi Amiri[1], A. Tschank[2], R. Ulrich[1], C. Walter[1], F. Licciardello[1], Y. Mogentale[1], A. Singh[1]
[1]Kandou Bus, Lausanne, Switzerland; [2]Kandou Bus, Northampton, United Kingdom

9:00 AM

10.2 A 38mW 40Gb/s 4-Lane Tri-Band PAM-4 / 16-QAM Transceiver in 28nm CMOS for High-Speed Memory Interface DS1

W-H. Cho[1], Y. Li[1], Y. Du[1], C-H. Wong[1], J. Du[1], P-T. Huang[1,2], S. J. Lee[1], H-N. Chen[3], C-P. Jou[3], F-L. Hsueh[3], M-C. F. Chang[1,2]
[1]University of California, Los Angeles, CA
[2]National Chiao Tung University, Hsinchu, Taiwan; [3]TSMC, Hsinchu, Taiwan

9:30 AM

10.3 An Analog Front-End for 100BASE-T1 Automotive Ethernet in 28nm CMOS DS2

H. Pan[1], J. Tan[1], E. Wang[1], J. Wang[1], K. Swaminathan[2], R. Pandarinathan[2], R. Pasagadugula[2], V. Yakkala[2], M. Hammad[1], K. Abdelhalim[1], K. Li[1], S. Cui[1], J. Wang[1], A. Chini[1], M. Tazebay[1], S. Venkatesan[2], D. Tam[1], I. Fujimori[1], K. Vakilian[1]
[1]Broadcom, Irvine, CA; [2]Broadcom, Bangalore, India

Break 10:00 AM

10:15 AM

10.4 A 12Gb/s 0.9mW/Gb/s Wide-Bandwidth Injection-Type CDR in 28nm CMOS with Reference-Free Frequency Capture

T. Masuda[1], R. Shinoda[1], J. Chatwin[2], J. Wysocki[2], K. Uchino[1], Y. Miyajima[3], Y. Ueno[1], K. Maruko[1], Z. Zhou[1], H. Matsumoto[1], H. Suzuki[1], N. Shoji[1]
[1]Sony, Tokyo, Japan; [2]Mixed Signal Systems, Scotts Valley, CA
[3]Sony LSI Design, Kanagawa, Japan

10:45 AM

10.5 A Digital PLL with Feedforward Multi-Tone Spur Cancelation Loop Achieving <-73dBc Fractional Spur and <-110dBc Reference Spur in 65nm CMOS

C-R. Ho, M-W. Chen, University of Southern California, Los Angeles, CA

11:15 AM

10.6 A 6.75-to-8.25GHz, 250fs$_{rms}$-Integrated-Jitter 3.25mW Rapid On/Off PVT-Insensitive Fractional-N Injection-Locked Clock Multiplier in 65nm CMOS

A. Elkholy[1], A. Elmallah[1], M. Elzeftawi[2], K. Chang[2], P. K. Hanumolu[1]
[1]University of Illinois, Urbana-Champaign, IL; [2]Xilinx, San Jose, CA

11:45 AM

10.7 A 185fs$_{rms}$-Integrated-Jitter and -245dB FOM PVT-Robust Ring-VCO-Based Injection-Locked Clock Multiplier with a Continuous Frequency-Tracking Loop Using a Replica-Delay Cell and a Dual-Edge Phase Detector

S. Choi, S. Yoo, J. Choi, Ulsan National Institute of Science and Technology, Ulsan, Korea

12:00 PM

10.8 A 12-to-26GHz Fractional-N PLL with Dual Continuous Tuning LC-D/VCOs

M. Ferriss, B. Sadhu, A. Rylyakov, H. Ainspan, D. Friedman
IBM Research, Yorktown Heights, NY

Conclusion 12:15 PM

Sensors and Displays

Session Chair: ***Yong Ping Xu,*** *National University of Singapore, Singapore*
Associate Chair: ***Joseph Shor,*** *Bar Ilan University, Ramat Gan, Israel*

8:30 AM

11.1 Dual-MEMS-Resonator Temperature-to-Digital Converter with 40µK Resolution and FOM of 0.12pJK²

M. Heidarpour Roshan[1,2], S. Zaliasl[1], K. Joo[1], K. Souri[1], R. Palwai[1], W. Chen[1], S. Pamarti[3], J. C. Doll[1], N. Miller[1], C. Arft[1], S. Tabatabaei[1], C. Sechen[2], A. Partridge[1], V. Menon[1]

[1]SiTime, Sunnyvale, CA; [2]University of Texas, Dallas, TX
[3]University of California, Los Angeles, CA

9:00 AM

11.2 3D Ultrasonic Fingerprint Sensor-on-a-Chip DS2

H-Y. Tang[1], Y. Lu[2], F. Assaderagh[3], M. Daneman[3], X. Jiang[1], M. Lim[3], X. Li[1], E. Ng[3], U. Singhal[1], J. M. Tsai [3], D. A. Horsley[2], B. E. Boser[1]

[1]University of California, Berkeley, CA; [2]University of California, Davis, CA
[3]Invensense, San Jose, CA

9:30 AM

11.3 A Hybrid Multipath CMOS Magnetic Sensor with 210µT_{rms} Resolution and 3MHz Bandwidth for Contactless Current Sensing

J. Jiang, K. Makinwa, Delft University of Technology, Delft, The Netherlands

Break 10:00 AM

10:15 AM

11.4 1650µm² Thermal-Diffusivity Sensors with Inaccuracies Down to ±0.75°C in 40nm CMOS DS2

U. Sönmez, F. Sebastiano, K. A. Makinwa
Delft University of Technology, Delft, The Netherlands

10:30 AM

11.5 A 3.2×1.5×0.8mm³ 240nA 1.25-to-5.5V 32kHz-DTCXO RTC Module with an Overall Accuracy of ±1ppm and an All-Digital 0.1ppm Compensation-Resolution Scheme at 1Hz

D. Ruffieux[1], F. Pengg[1], N. Scolari[1], F. Giroud[1], D. Severac[1], T. Le[1], S. Dalla Piazza[2], O. Aubry[2]

[1]CSEM, Neuchâtel, Switzerland; [2]Micro Crystal, Grenchen, Switzerland

10:45 AM

11.6 A 100-TRX-Channel Configurable 85-to-385Hz-Frame-Rate Analog Front-End for Touch Controller with Highly Enhanced Noise Immunity of 20V_{pp}

J-E. Park, J. Park, Y-H. Hwang, J. Oh, D-K. Jeong
Seoul National University, Seoul, Korea

11:15 AM

11.7 A Load-Aware Pre-Emphasis Column Driver with 27% Settling-Time Reduction in ±18% Panel-Load RC Delay Variation for 240Hz UHD Flat-Panel Displays

J-S. Bang[1], H-S. Kim[2], K-S. Yoon[1], S-H. Lee[1], S-H. Park[1], O. Kwon[3], C. Shin[3], S. Kim[3], G-H. Cho[1]

[1]KAIST, Daejeon, Korea; [2]Dankook University, Cheonan, Korea
[3]Samsung Display, Yongin, Korea

11:45 AM

11.8 Chip-Scale Electro-Optical 3D FMCW Lidar with 8µm Ranging Precision

B. Behroozpour[1], P. A. M. Sandborn[1], N. Quack[1,2], T. J. Seok[1], Y. Matsui[3], M. C. Wu[1], B. E. Boser[1]

[1]University of California, Berkeley, CA; [2]EPFL, Lausanne, Switzerland
[3]Finisar, Fremont, CA

Conclusion 12:15 PM

Efficient Power Conversion

Session Chair: ***Vadim Ivanov,*** *Texas Instruments, Tucson, AZ*
Associate Chair: ***Jaejin Park,*** *Samsung Electronics, Hwaseong, Korea*

1:30 PM

12.1 A Rational-Conversion-Ratio Switched-Capacitor DC-DC Converter Using Negative-Output Feedback
W. Jung, D. Sylvester, D. Blaauw, University of Michigan, Ann Arbor, MI

2:00 PM

12.2 A 94.6%-Efficiency Fully Integrated Switched-Capacitor DC-DC Converter in Baseline 40nm CMOS Using Scalable Parasitic Charge Redistribution
N. Butzen, M. Steyaert, KU Leuven, Leuven, Belgium

2:30 PM

12.3 A 2-Output Step-Up/Step-Down Switched-Capacitor DC-DC Converter with 95.8% Peak Efficiency and 0.85-to-3.6V Input Voltage Range
C. K. Teh, A. Suzuki, Toshiba, Kawasaki, Japan

2:45 PM

12.4 A 10mW Fully Integrated 2-to-13V-Input Buck-Boost SC Converter with 81.5% Peak Efficiency
D. Lutz, P. Renz, B. Wicht, Reutlingen University, Reutlingen, Germany

Break 3:00 PM

3:15 PM

12.5 A 2MHz 12-to-100V 90%-Efficiency Self-Balancing ZVS Three-Level DC-DC Regulator with Constant-Frequency AOT V^2 Control and 5ns ZVS Turn-On Delay
J. Xue, H. Lee, University of Texas, Dallas, TX

3:45 PM

12.6 Capacitor-Current-Sensor Calibration Technique and Application in a 4-Phase Buck Converter with Load-Transient Optimization
S-Y. Huang, K-Y. Fang, Y-W. Huang, S-H. Chien, T-H. Kuo
National Cheng Kung University, Tainan, Taiwan

4:15 PM

12.7 A 96%-Efficiency and 0.5%-Current-Cross-Regulation Single-Inductor Multiple Floating-Output LED Driver with 24b Color Resolution
H-A. Yang[1], W-H. Yang[1], K-H. Chen[1], C-L. Wey[1], Y-H. Lin[2], C-C. Lee[2], J-R. Lin[2], T-Y. Tsai[2], S-C. Lai[3]
[1]National Chiao Tung University, Hsinchu, Taiwan
[2]Realtek Semiconductor, Hsinchu, Taiwan
[3]Nan Hua University, Hsinchu, Taiwan

4:45 PM

12.8 DS2 Synchronized Floating Current Mirror for Maximum LED Utilization in Multiple-String Linear LED Drivers
J. Kim, S. Park, Dankook University, Yongin, Korea

5:00 PM

12.9 A Flying-Domain DC-DC Converter Powering a Cortex-M0 Processor with 90.8% Efficiency
L. G. Salem, J. G. Louie, P. P. Mercier, University of California, San Diego, CA

Conclusion 5:15 PM

Wireless Systems

Session Chair: ***Yuu Watanabe,*** *DENSO, Tokyo, Japan*
Associate Chair: ***Pierre Busson,*** *STMicroelectronics, Crolles, France*

1:30 PM

13.1 A 940MHz-Bandwidth 28.8µs-Period 8.9GHz Chirp Frequency Synthesizer PLL in 65nm CMOS for X-Band FMCW Radar Applications
H. Yeo[1,2], S. Ryu[1], Y. Lee[1], S. Son[1], J. Kim[1]
[1]Seoul National University, Seoul, Korea
[2]Samsung Semiconductor, Hwaseong, Korea

2:00 PM

13.2 A Ku-Band 260mW FMCW Synthetic Aperture Radar TRX with 1.48GHz BW in 65nm CMOS for Micro-UAVs
Y. Wang, K. Tang, Y. Zhang, L. Lou, B. Chen, S. Liu, L. Qiu, Y. Zheng
Nanyang Technological University, Singapore

2:30 PM

13.3 A 56Gb/s W-Band CMOS Wireless Transceiver
K. K. Tokgoz[1], S. Maki[1], S. Kawai[1], N. Nagashima[1], J. Emmei[1], M. Dome[1], H. Kato[1], J. Pang[1], Y. Kawano[2], T. Suzuki[2], T. Iwai[2], Y. Seo[1], K. Lim[1], S. Sato[1], L. Ning[1], K. Nakata[1], K. Okada[1], A. Matsuzawa[1]
[1]Tokyo Institute of Technology, Tokyo, Japan
[2]Fujitsu Laboratories, Atsugi, Japan

Break 3:00 PM

3:15 PM

13.4 A Microwave Injection-Locking Outphasing Modulator with 30dB Dynamic Range and 22% System Efficiency in 45nm CMOS SOI
M. Mehrjoo[1], J. Buckwalter[1,2]
[1]University of California, San Diego, CA
[2]University of California, Santa Barbara, CA

3:45 PM

13.5 A 4-Antenna-Path Beamforming Transceiver for 60GHz Multi-Gb/s Communication in 28nm CMOS
G. Mangraviti[1], K. Khalaf[1,2], Q. Shi[1,2], K. Vaesen[1], D. Guermandi[1], V. Giannini[1,3], S. Brebels[1], F. Frazzica[1], A. Bourdoux[1], C. Soens[1], W. Van Thillo[1], P. Wambacq[1,2]
[1]imec, Heverlee, Belgium
[2]Vrije Universiteit Brussel, Brussels, Belgium
[3]now with Texas Instruments, Dallas, TX

4:15 PM

13.6 A 42Gb/s 60GHz CMOS Transceiver for IEEE 802.11ay
R. Wu, S. Kawai, Y. Seo, N. Fajri, K. Kimura, S. Sato, S. Kondo, T. Ueno, T. Siriburanon, S. Maki, B. Liu, Y. Wang, N. Nagashima, M. Miyahara, K. Okada, A. Matsuzawa
Tokyo Institute of Technology, Tokyo, Japan

4:30 PM

13.7 A 0.22mm² CMOS Resistive Charge-Based Direct-Launch Digital Transmitter with -159dBc/Hz Out-of-Band Noise
P. E. Paro Filho[1,2], M. Ingels[1], P. Wambacq[1,2], J. Craninckx[1]
[1]imec, Leuven, Belgium
[2]Vrije Universiteit Brussel, Brussels, Belgium

Conclusion 4:45 PM

Next-Generation Processing

Session Chair: ***Paul Liang,*** *MediaTek, Hsinchu, Taiwan*
Associate Chair: ***Marian Verhelst,*** *KU Leuven, Heverlee, Belgium*

1:30 PM

14.1 A 126.1mW Real-Time Natural UI/UX Processor with Embedded DS2 Deep-Learning Core for Low-Power Smart Glasses
S. Park, S. Choi, J. Lee, M. Kim, J. Park, H-J. Yoo
KAIST, Daejeon, Korea

2:00 PM

14.2 A 502GOPS and 0.984mW Dual-Mode ADAS SoC with RNN-FIS Engine DS2 for Intention Prediction in Automotive Black-Box System
K. J. Lee, K. Bong, C. Kim, J. Jang, H. Kim, J. Lee, K-R. Lee, G. Kim, H-J. Yoo
KAIST, Daejeon, Korea

2:30 PM

14.3 A 0.55V 1.1mW Artificial-Intelligence Processor with PVT DS2 Compensation for Micro Robots
Y. Kim, D. Shin, J. Lee, Y. Lee, H-J. Yoo
KAIST, Daejeon, Korea

Break 3:00 PM

3:15 PM

14.4 A 21.5M-Query-Vectors/s 3.37nJ/Vector Reconfigurable k-Nearest-Neighbor Accelerator with Adaptive Precision in 14nm Tri-Gate CMOS
H. Kaul, M. A. Anders, S. K. Mathew, G. Chen, S. K. Satpathy, S. K. Hsu, A. Agarwal, R. K. Krishnamurthy
Intel, Hillsboro, OR

3:45 PM

14.5 Eyeriss: An Energy-Efficient Reconfigurable Accelerator for Deep DS2 Convolutional Neural Networks
Y-H. Chen[1], T. Krishna[1], J. Emer[1,2], V. Sze[1]
[1]Massachusetts Institute of Technology, Cambridge, MA
[2]Nvidia, Westford, MA

4:15 PM

14.6 A 1.42TOPS/W Deep Convolutional Neural Network Recognition Processor for Intelligent IoE Systems
J. Sim, J-S. Park, M. Kim, D. Bae, Y. Choi, L-S. Kim
KAIST, Daejeon, Korea

4:45 PM

14.7 A 4Gpixel/s 8/10b H.265/HEVC Video Decoder Chip for 8K Ultra HD Applications
D. Zhou, S. Wang, H. Sun, J. Zhou, J. Zhu, Y. Zhao, J. Zhou, S. Zhang, S. Kimura, T. Yoshimura, S. Goto
Waseda University, Kitakyushu, Japan

Conclusion 5:15 PM

Oversampling Data Converters

Session Chair: ***Venkatesh Srinivasan,*** *Texas Instruments, Dallas, TX*
Associate Chair: ***Tai-Cheng Lee,*** *National Taiwan University, Taipei, Taiwan*

1:30 PM

15.1 A 24.7mW 45MHz-BW 75.3dB-SNDR SAR-Assisted CT ΔΣ Modulator with 2nd-Order Noise Coupling in 65nm CMOS
B. Wu, S. Zhu, B. Xu, Y. Chiu
University of Texas, Dallas, TX

2:00 PM

15.2 A 2.2GHz Continuous-Time ΔΣ ADC with -102dBc THD and 25MHz BW
L. Breems[1], M. Bolatkale[1], H. Brekelmans[1], S. Bajoria[1], J. Niehof[1], R. Rutten[1], B. Oude-Essink[2], F. Fritschij[2], J. Singh[2], G. Lassche[2]
[1]NXP Semiconductors, Eindhoven, The Netherlands
[2]Catena Microelectronics, Delft, The Netherlands

2:30 PM

15.3 A 1V 77dB-DR 72dB-SNDR 10MHz-BW 2-1 MASH CT ΔΣM
B. Nowacki[1,2], N. Paulino[1,2], J. Goes[1,2]
[1]DEE, FCT, Universidade NOVA de Lisboa, Caparica, Portugal
[2]CTS-UNINOVA, Caparica, Portugal

2:45 PM

15.4 A 280μW 24kHz-BW 98.5dB-SNDR Chopped Single-Bit CT ΔΣM Achieving <10Hz 1/f Noise Corner Without Chopping Artifacts
S. Billa, A. Sukumaran, S. Pavan
IIT Madras, Chennai, India

Break 3:00 PM

3:15 PM

15.5 A 930mW 69dB-DR 465MHz-BW CT 1-2 MASH ADC in 28nm CMOS
Y. Dong[1], J. Zhao[1], W. Yang[1], T. Caldwell[2], H. Shibata[2], R. Schreier[2], Q. Meng[3], J. Silva[1], D. Paterson[1], J. Gealow[1]
[1]Analog Devices, Wilmington, MA
[2]Analog Devices, Toronto, Canada
[3]Analog Devices, Cambridge, MA

3:45 PM

15.6 A 160MHz-BW 72dB-DR 40mW Continuous-Time ΔΣ Modulator in 16nm CMOS with Analog ISI-Reduction Technique
S-H. Wu, T-K. Kao, Z-M. Lee, P. Chen, J-Y. Tsai
MediaTek, Hsinchu, Taiwan

4:15 PM

15.7 A 1.65mW 0.16mm² Dynamic Zoom-ADC with 107.5dB DR in 20kHz BW
B. Gönen[1], F. Sebastiano[1], R. van Veldhoven[2], K. A. A. Makinwa[1]
[1]Delft University of Technology, Delft, The Netherlands
[2]NXP Semiconductors, Eindhoven, The Netherlands

4:45 PM

15.8 A 22.3b 1kHz 12.7mW Switched-Capacitor ΔΣ Modulator with Stacked Split-Steering Amplifiers
M. Steiner[1], N. Greer[2]
[1]ams AG, Unterpremstaetten, Austria
[2]West Silicon EURL, Hottot les Bagues, France

Conclusion 5:15 PM

Innovations in Circuits and Systems Enabled by Novel Technologies

Session Chair: ***Pirooz Parvarandeh,*** *Genia, Los Altos, CA*
Associate Chair: ***Shuichi Nagai,*** *Panasonic, Osaka, Japan*

1:30 PM

16.1 A Nanogap Transducer Array on 32nm CMOS for Electrochemical DNA Sequencing
D. A. Hall[1,2], J. S. Daniels[1], B. Geuskens[3], N. Tayebi[1], G. M. Credo[1], D. J. Liu[1], H. Li[1], K. Wu[1], X. Su[1], M. Varma[1], O. Elibol[1]
[1]Intel, Santa Clara, CA; [2]University of California, San Diego, CA; [3]Intel, Hillsboro, OR

2:00 PM

16.2 A Keccak-Based Wireless Authentication Tag with per-Query Key Update and Power-Glitch Attack Countermeasures DS2
C. S. Juvekar[1], H-M. Lee[1], J. Kwong[2], A. P. Chandrakasan[1]
[1]Massachusetts Institute of Technology, Cambridge, MA
[2]Texas Instruments, Dallas, TX

2:30 PM

16.3 A 16×16 pixels SPAD-based 128-Mb/s Quantum Random Number Generator with -74dB Light Rejection Ratio and -6.7ppm/°C Bias Sensitivity on Temperature
N. Massari[1], L. Gasparini[1], A. Tomasi[2], A. Meneghetti[2], H. Xu[1], D. Perenzoni[1], G. Morgari[3], D. Stoppa[1]
[1]Fondazione Bruno Kessler, Trento, Italy; [2]University of Trento, Povo, Italy
[3]Telsy, Torino, Italy

Break 3:00 PM

3:15 PM

16.4 A Flexible EEG Acquisition and Biomarker Extraction System Based on Thin-Film Electronics
T. Moy, L. Huang, W. Rieutort-Louis, S. Wagner, J. C. Sturm, N. Verma
Princeton University, Princeton, NJ

3:45 PM

16.5 A Flexible Thin-Film Pixel Array with a Charge-to-Current Gain of 59μA/pC and 0.33% Nonlinearity and a Cost Effective Readout Circuit for Large-Area X-ray Imaging
F. De Roose[1,2], K. Myny[2], S. Steudel[2], M. Willigems[2], S. Smout[2], T. Piessens[3], J. Genoe[1,2], W. Dehaene[1,2]
[1]KU Leuven, Leuven, Belgium; [2]imec, Heverlee, Belgium; [3]ICsense, Leuven, Belgium

4:00 PM

16.6 Flexible Thin-Film NFC Transponder Chip Exhibiting Data Rates Compatible to ISO NFC Standards Using Self-Aligned Metal-Oxide TFTs
K. Myny, S. Steudel, imec, Leuven, Belgium

4:15 PM

16.7 A Fully-Integrated Half-Duplex Data/Power Transfer System with up to 40Mb/s Data Rate, 23mW Output Power and On-Chip 5kV Galvanic Isolation
P. Lombardo[1], V. Fiore[1], E. Ragonese[2], G. Palmisano[1]
[1]University of Catania, Catania, Italy; [2]STMicroelectronics, Catania, Italy

4:45 PM

16.8 A 3-to-40V 10-to-30MHz Automotive-Use GaN Driver with Active BST Balancing and V_{sw} Dual-Edge Dead-Time Modulation Achieving 8.3% Efficiency Improvement and 3.4ns Constant Propagation Delay
X. Ke[1], J. Sankman[2], M. K. Song[1], P. Forghani[2], D. Ma[1]
[1]University of Texas, Dallas, TX; [2]Texas Instruments, Dallas, TX

Conclusion 5:15 PM

Demonstration Session 2, Tuesday, February 2nd 5:00-7:00 PM

This year, the Demonstration Session extending in selected regular papers, both Academic and Industrial, will take place on Monday February 1st, and Tuesday February 2nd, from 5 pm until 7 pm in the Golden Gate Hall. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2016, as noted by the symbol **DS2**

Tuesday, February 2nd

9:30 AM

10.3 An Analog Front-End for 100BASE-T1 Automotive Ethernet in 28nm CMOS

9:00 AM

11.2 3D Ultrasonic Fingerprint Sensor-on-a-Chip

10:15 AM

11.4 1650μm² Thermal-Diffusivity Sensors with Inaccuracies Down to ±0.75°C in 40nm CMOS

4:45 PM

12.8 Synchronized Floating Current Mirror for Maximum LED Utilization in Multiple-String Linear LED Drivers

1:30 PM

14.1 A 126.1mW Real-Time Natural UI/UX Processor with Embedded Deep-Learning Core for Low-Power Smart Glasses

2:00 PM

14.2 A 502GOPS and 0.984mW Dual-Mode ADAS SoC with RNN-FIS Engine for Intention Prediction in Automotive Black-Box System

2:30 PM

14.3 A 0.55V 1.1mW Artificial-Intelligence Processor with PVT Compensation for Micro Robots

3:45 PM

14.5 Eyeriss: An Energy-Efficient Reconfigurable Accelerator for Deep Convolutional Neural Networks

2:00 PM

16.2 A Keccak-Based Wireless Authentication Tag with per-Query Key Update and Power-Glitch Attack Countermeasures

Wednesday, February 3rd

8:30 AM

20.1 A 300GHz 40nm CMOS Transmitter with 32-QAM 17.5Gb/s/ch Capability over 6 Channels

11:45 AM

21.8 An All-in-One (Qi, PMA and A4WP) 2.5W Fully Integrated Wireless Battery Charger IC for Wearable Applications

10:15 AM

22.4 A 172μW Compressive Sampling Photoplethysmographic Readout with Embedded Direct Heart-Rate and Variability Extraction from Compressively Sampled Data

10:45 AM

22.5 A 0.5V 55μW 64×2-Channel Binaural Silicon Cochlea for Event-Driven Stereo-Audio Sensing

2:00 PM

23.2 A 32Gb/s Bidirectional 4-Channel 4pJ/b Capacitively Coupled Link in 14nm CMOS for Proximity Communication

1:30 PM

24.1 A 0.6V 8mW 3D Vision Processor for a Navigation Device for the Visually Impaired

2:30 PM

26.3 A 1.3nJ/b IEEE 802.11ah Fully Digital Polar Transmitter for IoE Applications

3:30 PM

26.5 A 0.7V 1.5-to-2.3mW GNSS Receiver with 2.5-to-3.8dB NF in 28nm FD-SOI

2:00 PM

27.2 An Oversampling SAR ADC with DAC Mismatch Error Shaping Achieving 105dB SFDR and 101dB SNDR over 1kHz BW in 55nm CMOS

1:30 PM

28.1 A Handheld 50pM-Sensitivity Micro-NMR CMOS Platform with B-Field Stabilization for Multi-Type Biological/Chemical Assays

2:00 PM

28.2 A 14GHz Battery-Operated Point-of-Care ESR Spectrometer Based on a 0.13μm CMOS ASIC

2:30 PM

28.3 CMOS Biosensor IC Focusing on Dielectric Relaxations of Biological Water with 120GHz and 60GHz Oscillator Arrays

3:15 PM

28.4 A Battery-Powered Efficient Multi-Sensor Acquisition System with Simultaneous ECG, BIO-Z, GSR, and PPG

TIMETABLE OF ISSCC 2016 SESSIONS

ISSCC 2016 • Sunday January 31st

Tutorials

8:30 AM	**T1:** Understanding Phase Noise in LC VCOs	**T2:** Basics of Memory Tiers in Compute Systems	**T3:** High-Voltage Power Devices, Converter Topologies and Applications
10:30 AM	**T4:** System-Level Power-Management Techniques	**T5:** Basics of SAR ADCs: Circuits & Architectures	**T6:** Optical Interconnects: Design and Analysis
1:30 PM	**T7:** Asynchronous Circuit Design and Methodology for Low-Power IoE	**T8:** Noise Simulation in Mixed-Signal SoCs	
3:30 PM	**T9:** Circuit Design for Low-Power Wireless Applications	**T10:** Circuit Design Considerations for Implantable Devices	

Forums

8:00 AM	**F1:** Designing Secure Systems: Manufacturing, Circuits and Architectures	**F2:** Data Converter Calibration and Dynamic Matching Techniques

Events Below in Bold Box are Included with your Conference Registration

Evening Sessions

7:30 PM	**ES1:** Student Research Preview: Short Presentations with Poster Session	**8:00 PM**	**ES2:** Computing Architectures Paving the Path to Power Efficiency

ISSCC 2016 • Monday February 1st

Paper Sessions

8:30 AM	**Session 1:** Plenary Session				
1:30 PM	**Session 2:** RF Frequency Synthesis Techniques	**Session 3:** Ultra-High-Speed Transceivers	**Session 4:** Digital Processors	**Session 5:** Analog Techniques	**Session 6:** Image Sensors

5:00 PM to 7:00 PM – Demonstration Session • 5:15 PM – Author Interviews • Social Hour

Evening Events

8:00 PM	**EE1:** Class of 2025 – Where Will Be the Best Jobs?	**EE2:** Do We Need to Downscale Our Radios Below 20nm?

ISSCC 2016 • Tuesday February 2nd

Paper Sessions

8:30 AM	**Session 7:** Nonvolatile Memory Solutions	**Session 8:** Low-Power Digital Circuits	**Session 9:** High-Performance Wireless	**Session 10:** Advanced Wireline Transceivers and PLLs	**Session 11:** Sensors and Displays
1:30 PM	**Session 12:** Efficient Power Conversion	**Session 13:** Wireless Systems	**Session 14:** Next-Generation Processing	**Session 15:** Oversampling Data Converters	**Session 16:** Innovations in Circuits and Systems Enabled by Novel Technologies

5:00 PM to 7:00 PM – Demonstration Session • 5:15 PM – Author Interviews • Social Hour

Evening Events

8:00 PM	**EE3:** Survey Says!	**EE4:** Eureka! The Best Moments of Solid-State Circuit Design in the 2000s

ISSCC 2016 • Wednesday February 3rd

Paper Sessions

8:30 AM	**Session 17:** SRAM **Session 18:** High-Bandwidth DRAM	**Session 19:** Digital PLLs	**Session 20:** RF-to-THz Transceiver Techniques	**Session 21:** Harvesting and Wireless Power	**Session 22:** Systems and Instruments for Human-Machine Interfaces
1:30 PM	**Session 23:** Electrical and Optical Link Innovations	**Session 24:** Ultra-Efficient Computing **Session 25:** mm-Wave THz Sensing	**Session 26:** Wireless for IoE	**Session 27:** Hybrid and Nyquist Data Converters	**Session 28:** Biological Sensors for Point of Care

5:15 PM – Author Interviews • Social Hour

ISSCC 2016 • Thursday February 4th

8:00 AM	**Short Course:** Circuits for the Internet of Everything			
8:00 AM	**F3:** Radio Architectures and Circuits Towards 5G	**F4:** Emerging Short-Reach and High-Density Interconnect Solutions for Internet of Everything	**F5:** Advanced IC Design for Ultra Low-Noise Sensing	**F6:** Circuit, Systems and Data Processing for Next Generation Wearable and Implantable Medical Devices

EE3: Survey Says!

Organizers: **Harry Lee,** *MIT, Cambridge, MA*
Matt Straayer, *Maxim Integrated, North Chelmsford, MA*

Moderator: **Chris Mangelsdorf**, *Analog Devices, San Diego, CA*

Modeled after the US game show Family Feud, this event features two teams (assisted by the audience) that will compete to name the most popular responses to survey questions related to data converters. The teams are composed of world-renowned data-converter experts. Survey questions probe both professional and personal sides, for example: What is the first thing you would do after you tape-out? What excuse would you make to your manager to get more time to tape-out? What is the most common cause of data-converter design failure? What would you do first if you made $10M from your start-up? The audience will take sides and participate to help their favorite team in case they are having difficulty. This is an opportunity to learn how others in the field cope with various situations and also get a glimpse into their lighter-hearted side of life.

Panelists: **SeongHwan Cho**, *KAIST, Daejeon, Korea*
Marco Corsi, *Texas Instruments, Oak Point, TX*
Michael Flynn, *University of Michigan, Ann Arbor, MI*
Harmke de Groot, *imec/Holst Centre, Eindhoven, The Netherlands*
Franco Maloberti, *University of Pavia, Pavia, Italy*
Takashi Oshima, *Hitachi, Tokyo, Japan*
David Robertson, *Analog Devices, Wilmington, MA*
Behzad Razavi, *University of California, Los Angeles, CA*

EE4: Eureka! The Best Moments of Solid-State Circuit Design in the 2000s

Organizers: **Woogeun Rhee,** *Tsinghua University, Beijing, China*
Eric Klumperink, *University of Twente, Enschede, The Netherlands*

Moderator: **Hossein Hashemi**, *University of Southern California, Los Angeles, CA*

Eureka moments are exciting, but do the resulting ideas also work out as hoped for? Do they have impact on the field? Well-known experts from various fields will share their ups and downs related to recent innovations in solid-state circuits and put them in a historical perspective with earlier developments. This panel features six entertaining presentations given by leading experts in the areas of power conversion, digital clock generation, mm-Wave, wireless, biomedical SoC, and wireline systems.

Panelists: **Seth R. Sanders**, *University of California, Berkeley, CA*
R. Bogdan Staszewski, *University College Dublin, Dublin, Ireland*
Ali Hajimiri, *Caltech, Pasadena, CA*
Bram Nauta, *University of Twente, Enschede, The Netherlands*
Hoi-Jun Yoo, *KAIST, Daejeon, Korea*
Bryan Casper, *Intel, OR*

SRAM

Session Chair: ***Hugh Mair,*** *MediaTek, Austin, TX*
Associate Chair: ***Atsushi Kawasumi,*** *Toshiba, Kawasaki, Japan*

8:30 AM

17.1 A 10nm FinFET 128Mb SRAM with Assist Adjustment System for Power, Performance, and Area Optimization
T. Song, W. Rim, S. Park, Y. Kim, J. Jung, G. Yang, S. Baek, J. Choi, B. Kwon, Y. Lee, S. Kim, G. Kim, H-S. Won, J-H. Ku, S. S. Paak, E. Jung, S. S. Park, K. Kim
Samsung Electronics, Hwaseong, Korea

9:00 AM

17.2 5.6Mb/mm² 1R1W 8T SRAM Arrays Operating down to 560mV Utilizing Small-Signal Sensing with Charge-Shared Bitline and Asymmetric Sense Amplifier in 14nm FinFET CMOS Technology
J. Keane, J. Kulkarni, K-H. Koo, S. Nalam, Z. Guo, E. Karl, K. Zhang
Intel, Hillsboro, OR

9:30 AM

17.3 A Reconfigurable Dual-Port Memory with Error Detection and Correction in 28nm FDSOI
M. Khayatzadeh[1], M. Saligane[1], J. Wang[1], M. Alioto[2], D. Blaauw[1], D. Sylvester[1]
[1]University of Michigan, Ann Arbor, MI
[2]National University of Singapore, Singapore

Break 10:00 AM

High-Bandwidth DRAM

Session Chair: ***Chulwoo Kim,*** *Korea University, Seoul, Korea*
Associate Chair: ***Martin Brox,*** *Micron, Munich, Germany*

10:15 AM

18.1 A 20nm 9Gb/s/pin 8Gb GDDR5 DRAM with an NBTI Monitor, Jitter Reduction Techniques and Improved Power Distribution
H-Y. Joo, S-J. Bae, Y-S. Sohn, Y-S. Kim, K-S. Ha, M-S. Ahn, Y-J. Kim, Y-J. Kim, Y-J. Kim, J-H. Kim, W-J. Choi, C-H. Shin, S. H. Kim, B-C. Kim, S-B. Ko, K-I. Park, S-J. Jang, G-Y. Jin
Samsung Electronics, Hwaseong, Korea

10:45 AM

18.2 A 1.2V 20nm 307GB/s HBM DRAM with At-Speed Wafer-Level I/O Test Scheme and Adaptive Refresh Considering Temperature Distribution
K. Sohn, W-J. Yun, R. Oh, C-S. Oh, S-Y. Seo, M-S. Park, D-H. Shin, W-C. Jung, S-H. Shin, J-M. Ryu, H-S. Yu, J-H. Jung, K-W. Nam, S-K. Choi, J-W. Lee, U. Kang, Y-S. Sohn, J-H. Choi, C-W. Kim, S-J. Jang, G-Y. Jin
Samsung Electronics, Hwaseong, Korea

11:15 AM

18.3 A 1.2V 64Gb 8-Channel 256GB/s HBM DRAM with Peripheral-Base-Die Architecture and Small-Swing Technique on Heavy Load Interface
J. C. Lee, J. Kim, K. W. Kim, Y. J. Ku, D. S. Kim, C. Jeong, T. S. Yun, H. Kim, H. S. Cho, Y. O. Kim, J. H. Kim, J. H. Kim, S. Oh, H. S. Lee, K. H. Kwon, D. B. Lee, Y. J. Choi, J. Lee, H. G. Kim, J. H. Chun, J. Oh, S. H. Lee
SK hynix, Icheon, Korea

11:45 AM

18.4 An 1.1V 68.2GB/s 8Gb Wide-IO2 DRAM with Non-Contact Microbump I/O Test Scheme
Y. J. Yoon, B. D. Jeon, B. S. Kim, K. U. Kim, T. Y. Lee, N. Kwak, W. Y. Shin, N. Y. Kim, Y. Hong, K. P. Kang, D. Y. Ka, S. J. Lee, Y. S. Kim, Y. K. Noh, J. Kim, D. K. Kang, H. U. Song, H. G. Kim, J. Oh
SK hynix, Icheon, Korea

Conclusion 12:15 PM

Digital PLLs

Session Chair: ***John Maneatis,*** *True Circuits, Mountain View, CA*
Associate Chair: ***Kathy Wilcox,*** *AMD, Boxborough, MA*

8:30 AM

19.1 A 0.5-to-9.5GHz 1.2µs-Lock-Time Fractional-N DPLL with ±1.25% UI Period Jitter in 16nm CMOS For Dynamic Frequency and Core-Count Scaling in SoC
F. Ahmad, G. Unruh, A. Iyer, P-E. Su, S. Abdalla, B. Shen, M. Chambers, I. Fujimori
Broadcom, Irvine, CA

9:00 AM

19.2 A 0.2-to-1.45GHz Subsampling Fractional-N All-Digital MDLL with Zero-Offset Aperture PD-Based Spur Cancellation and In-Situ Timing Mismatch Detection
S. Kundu[1], B. Kim[2], C. H. Kim[1]
[1]University of Minnesota, Minneapolis, MN
[2]Rambus, Sunnyvale, CA

9:30 AM

19.3 A 2.4GHz 1.5mW Digital MDLL Using Pulse-Width Comparator and Double Injection Technique in 28nm CMOS
H. Kim[1,2], Y. Kim[1], T. Kim[2], H. Park[2], S. Cho[1]
[1]KAIST, Daejeon, Korea
[2]Samsung Electronics, Hwaseong, Korea

Break 10:00 AM

10:15 AM

19.4 A 0.17-to-3.5mW 0.15-to-5GHz SoC PLL with 15dB Built-In Supply Noise Rejection and Self-Bandwidth Control in 14nm CMOS
K-Y. J. Shen, S. F. Syed Farooq, Y. Fan, K. M. Nguyen, Q. Wang, A. Elshazly, N. Kurd
Intel, Hillsboro, OR

10:45 AM

19.5 A 3.2GHz Digital Phase-Locked Loop with Background Supply-Noise Cancellation
C-W. Yeh, C-E. Hsieh, S-I. Liu
National Taiwan University, Taipei, Taiwan

11:00 AM

19.6 Voltage-Scalable Frequency-Independent Quasi-Resonant Clocking Implementation of a 0.7-to-1.2V DVFS System
F. U. Rahman, V. S. Sathe
University of Washington, Seattle, WA

11:15 AM

19.7 A 65nm CMOS ADPLL with 360µW 1.6ps-INL SS-ADC-Based Period-Detection-Free TDC
A. Sai, S. Kondo, T. T. Ta, H. Okuni, M. Furuta, T. Itakura
Toshiba, Kawasaki, Japan

11:45 AM

19.8 A 0.0021mm² 1.82mW 2.2GHz PLL Using Time-Based Integral Control in 65nm CMOS
J. Zhu, R. K. Nandwana, G. Shu, A. Elkholy, S-J. Kim, P. K. Hanumolu
University of Illinois, Urbana-Champaign, IL

Conclusion 12:15 PM

RF-to-THz Transceiver Techniques

Session Chair: ***Harish Krishnaswamy,*** *Columbia University, New York, NY*
Associate Chair: ***Jussi Ryynanen,*** *Aalto University, Espoo, Finland*

8:30 AM

20.1 DS2 **A 300GHz 40nm CMOS Transmitter with 32-QAM 17.5Gb/s/ch Capability over 6 Channels**
K. Katayama[1], K. Takano[1], S. Amakawa[1], S. Hara[2], A. Kasamatsu[2], K. Mizuno[3], K. Takahashi[3], T. Yoshida[1], M. Fujishima[1]
[1]Hiroshima University, Hiroshima, Japan
[2]National Institute of Information and Communications Technology, Koganei, Japan
[3]Panasonic, Yokohama, Japan

9:00 AM

20.2 A Frequency-Reconfigurable mm-Wave Power Amplifier with Active-Impedance Synthesis in an Asymmetrical Non-Isolated Combiner
C. R. Chappidi, K. Sengupta, Princeton University, Princeton, NJ

9:30 AM

20.3 An 86-to-94.3GHz Transmitter with 15.3dBm Output Power and 9.6% Efficiency in 65nm CMOS
Y. Chao[1], L. Li[2], H. C. Luong[1]
[1]Hong Kong University of Science and Technology, Hong Kong, China
[2]Southeast University, Nanjing, China

Break 10:00 AM

10:15 AM

20.4 A 300GHz Wirelessly Locked 2×3 Array Radiating 5.4dBm with 5.1% DC-to-RF Efficiency in 65nm CMOS
S. Jameson, E. Halpern, E. Socher, Tel Aviv University, Tel Aviv, Israel

10:30 AM

20.5 1.4THz, -13dBm-EIRP Frequency Multiplier Chain Using Symmetric- and Asymmetric-CV Varactors in 65nm CMOS
Z. Ahmad, M. Lee, K. K. O, University of Texas, Dallas, TX

10:45 AM

20.6 A 28GHz Efficient Linear Power Amplifier for 5G Phased Arrays in 28nm Bulk CMOS
S. Shakib[1], H-C. Park[2], J. Dunworth[2], V. Aparin[2], K. Entesari[1]
[1]Texas A&M University, College Station, TX; [2]Qualcomm, San Diego, CA

11:00 AM

20.7 An RF-PA Supply Modulator Achieving 83% Efficiency and -136dBm/Hz Noise for LTE-40MHz and GSM 35dBm Applications
J-S. Paek, Y-S. Youn, J-H. Choi, D-S. Kim, J-H. Jung, Y-H. Choo, S-J. Lee, S-C. Lee, T. B. Cho, I-Y. Kang
Samsung Electronics, Hwaseong, Korea

11:30 AM

20.8 A Dual-Frequency 0.7-to-1GHz Balance Network for Electrical Balance Duplexers
B. Hershberg[1], B. van Liempd[1,2], X. Zhang[1], P. Wambacq[1,2], J. Craninckx[1]
[1]imec, Heverlee, Belgium; [2]Vrije Universiteit Brussel, Brussels, Belgium

11:45 AM

20.9 A 1.92mW Filtering Transimpedance Amplifier for RF Current Passive Mixers
T. Y. Liu, A. Liscidini, University of Toronto, Toronto, Canada

12:00 PM

20.10 A 68.1-to-96.4GHz Variable-Gain Low-Noise Amplifier in 28nm CMOS
M. Vigilante, P. Reynaert, KU Leuven, Leuven, Belgium

Conclusion 12:15 PM

Harvesting and Wireless Power

Session Chair: ***Anton Bakker,*** *Arctic Sand, San Jose, CA*
Associate Chair: ***Yuan Gao,*** *Institute of Microelectronics, Singapore, Singapore*

8:30 AM

21.1 A Single-Cycle MPPT Charge-Pump Energy Harvester Using a Thyristor-Based VCO Without Storage Capacitor
X. Liu, E. Sanchez-Sinencio, Texas A&M University, College Station, TX

9:00 AM

21.2 A 4μW-to-1mW Parallel-SSHI Rectifier for Piezoelectric Energy Harvesting of Periodic and Shock Excitations with Inductor Sharing, Cold Start-up and up to 681% Power Extraction Improvement
D. A. Sanchez[1], J. Leicht[1], E. Jodka[1], E. Fazel[1], Y. Manoli[1,2]
[1]University of Freiburg - IMTEK, Freiburg, Germany
[2]Hahn-Schickard, Villingen-Schwenningen, Germany

9:30 AM

21.3 A 200nA Single-Inductor Dual-Input-Triple-Output (DITO) Converter with Two-Stage Charging and Process-Limit Cold-Start Voltage for Photovoltaic and Thermoelectric Energy Harvesting
Y. Lu[1], S. Yao[1], B. Shao[2], P. Brokaw[3]
[1]Analog Devices, Shanghai, China
[2]Analog Devices, Wilmington, MA
[3]Analog Devices, San Jose, CA

9:45 AM

21.4 A >78%-Efficient Light Harvester over 100-to-100klux with Reconfigurable PV-Cell Network and MPPT Circuit
I. Lee, W. Lim, A. Teran, J. Phillips, D. Sylvester, D. Blaauw
University of Michigan, Ann Arbor, MI

Break 10:00 AM

10:15 AM

21.5 A Current-Mode Wireless Power Receiver with Optimal Resonant Cycle Tracking for Implantable Systems
M. Choi[1], T. Jang[1], J. Jeong[1,2], S. Jeong[1], D. Blaauw[1], D. Sylvester[1]
[1]University of Michigan, Ann Arbor, MI
[2]Korea University, Seoul, Korea

10:45 AM

21.6 A 1.2cm² 2.4GHz Self-Oscillating Rectifier-Antenna Achieving -34.5dBm Sensitivity for Wirelessly Powered Sensors
J. Kang, P. Y. Chiang, A. Natarajan
Oregon State University, Corvallis, OR

11:15 AM

21.7 A 6.78MHz 6W Wireless Power Receiver with a 3-Level 1× / ½ × / 0× Reconfigurable Resonant Regulating Rectifier
L. Cheng, W-H. Ki, T. T. Wong, T. S. Yim, C-Y. Tsui
Hong Kong University of Science and Technology, Hong Kong, China

11:45 AM

21.8 DS2 An All-in-One (Qi, PMA and A4WP) 2.5W Fully Integrated Wireless Battery Charger IC for Wearable Applications
J. T. Hwang, D. S. Lee, J. H. Lee, S. M. Park, K. W. Jin, M. J. Ko, H. I. Shin, S. O. Jeon, D. H. Kim, J. Rhee
MAPS, Yongin, Korea

Conclusion 12:15 PM

Systems and Instruments for Human-Machine Interfaces

Session Chair: ***Long Yan,*** *Samsung Electronics, Hwaseong, Korea*
Associate Chair: ***Refet Firat Yazicioglu,*** *GlaxoSmithKline, Herent, Belgium*

8:30 AM

22.1 Implanted Integrated Circuit Requirements For Brain - Machine Interfaces
K. Shenoy,
Stanford University, Palo Alto, CA

9:00 AM

22.2 A 176-Channel 0.5cm³ 0.7g Wireless Implant for Motor Function Recovery after Spinal Cord Injury
Y-K. Lo, C-W. Chang, Y-C. Kuan, S. Culaclii, B. Kim, K. Chen, P. Gad, V. R. Edgerton, W. Liu
University of California, Los Angeles, CA

9:30 AM

22.3 A 141µW Sensor SoC on OLED/OPD Substrate for SpO_2/ExG Monitoring Sticker
Y. Lee, H. Lee, J. Jang, J. Lee, M. Kim, J. Lee, H. Kim, K-R. Lee, K. Kim, H. Cho, S. Yoo, H-J. Yoo
KAIST, Daejeon, Korea

Break 10:00 AM

10:15 AM

22.4 A 172µW Compressive Sampling Photoplethysmographic Readout with Embedded Direct Heart-Rate and Variability Extraction from Compressively Sampled Data DS2
P. Venkata Rajesh[1,2], J. M. V. Sarmiento[3], L. Yan[1], A. Bozkurt[3], C. Van Hoof[1,2], N. Van Helleputte[1], R. F. Yazicioglu[1], M. Verhelst[2]
[1]imec, Leuven, Belgium; [2]KU Leuven, Leuven, Belgium
[3]North Carolina State University, Raleigh, NC

10:45 AM

22.5 A 0.5V 55µW 64×2-Channel Binaural Silicon Cochlea for Event-Driven Stereo-Audio Sensing DS2
M. Yang, C-H. Chien, T. Delbruck, S-C. Liu
ETH Zurich/University of Zurich, Zurich, Switzerland

11:15 AM

22.6 A 22V Compliant 56µW Active Charge Balancer Enabling 100% Charge Compensation even in Monophasic and 36% Amplitude Correction in Biphasic Neural Stimulators
N. Butz[1], A. Taschwer[2], Y. Manoli[1,2,3], M. Kuhl[1,3]
[1]University of Freiburg - IMTEK, Freiburg, Germany
[2]Hahn-Schickard, Villingen-Schwenningen, Germany
[3]BrainLinks-BrainTools Cluster of Excellence, Freiburg, Germany

11:45 AM

22.7 A 966-Electrode Neural Probe with 384 Configurable Channels in 0.13µm SOI CMOS
C. Mora Lopez[1], S. Mitra[1], J. Putzeys[1], B. Raducanu[1,2], M. Ballini[1], A. Andrei[1], S. Severi[1], M. Welkenhuysen[1], C. Van Hoof[1,2], S. Musa[1], R. F. Yazicioglu[1]
[1]imec, Leuven, Belgium; [2]KU Leuven, Heverlee, Belgium

12:00 PM

22.8 Multi-Functional Microelectrode Array System Featuring 59,760 Electrodes, 2048 Electrophysiology Channels, Impedance and Neurotransmitter Measurement Units
V. Viswam, J. Dragas, A. Shadmani, Y. Chen, A. Stettler, J. Müller, A. Hierlemann
ETH Zurich, Basel, Switzerland

Conclusion 12:15 PM

Electrical and Optical Link Innovations

Session Chair: ***Frank O'Mahony,*** *Intel, Portland, OR*
Associate Chair: ***Simone Erba,*** *STMicroelectronics, Pavia, Italy*

1:30 PM

23.1 A 16Mb/s-to-8Gb/s 14.1-to-5.9pJ/b Source Synchronous Transceiver Using DVFS and Rapid On/Off in 65nm CMOS
G. Shu, W. Choi, S. Saxena, S-J. Kim, M. Talegaonkar, R. Nandwana, A. Elkholy, D. Wei, T. Nandi , P. K. Hanumolu
University of Illinois, Urbana-Champaign, IL

2:00 PM

23.2 A 32Gb/s Bidirectional 4-Channel 4pJ/b Capacitively Coupled Link in 14nm CMOS for Proximity Communication DS2
C. Thakkar, S. Sen, J. E. Jaussi, B. Casper
Intel, Hillsboro, OR

2:30 PM

23.3 A 6Gb/s 3-Tap FFE Transmitter and 5-Tap DFE Receiver in 65nm/0.18µm CMOS for Next-Generation 8K Displays
M. Hekmat, S. Song, N. Jaffari, S. Sankaranarayanan, C. Huang, M. Han, G. Malhotra, J. Kamali, A. Amirkhany, W. Xiong
Samsung Semiconductor, San Jose, CA

Break 3:00 PM

3:15 PM

23.4 A 56Gb/s 300mW Silicon-Photonics Transmitter in 3D-Integrated PIC25G and 55nm BiCMOS Technologies
E. Temporiti[1], G. Minoia[1], M. Repossi[1], D. Baldi[1], A. Ghilioni[2], F. Svelto[2]
[1]STMicroelectronics, Pavia, Italy
[2]University of Pavia, Pavia, Italy

3:45 PM

23.5 A Dual 64Gbaud 10kΩ 5% THD Linear Differential Transimpedance Amplifier with Automatic Gain Control in 0.13µm BiCMOS Technology for Optical Fiber Coherent Receivers
A. Awny[1], R. Nagulapalli[1,2], D. Micusik[1,3], J. Hoffmann[4], G. Fischer[1], D. Kissinger[1,5], A. C. Ulusoy[1]
[1]IHP, Frankfurt(Oder), Germany
[2]now with Inphi Corporation, Northampton, United Kingdom
[3]now with Rohde & Schwarz, Munich, Germany
[4]Finisar, Berlin, Germany
[5]TU Berlin, Berlin, Germany

4:00 PM

23.6 A 30Gb/s 0.8pJ/b 14nm FinFET Receiver Data-Path
P. A. Francese, M. Brändli, C. Menolfi, M. Kossel, T. Morf, L. Kull, A. Cevrero, H. Yueksel, I. Oezkaya, D. Luu, T. Toifl
IBM Zurich Research Laboratory, Rüshlikon, Switzerland

4:15 PM

23.7 A 16Gb/s 1 IIR + 1 DT DFE Compensating 28dB Loss with Edge-Based Adaptation Converging in 5µs
S. Shahramian, B. Dehlaghi, A. Chan Carusone
University of Toronto, Toronto, Canada

4:45 PM

23.8 A 40Gb/s 14mW CMOS Wireline Receiver
A. Manian, B. Razavi
University of California, Los Angeles, CA

Conclusion 5:15 PM

Ultra-Efficient Computing: Application-Inspired and Analog-Assisted Digital

Session Chair: ***Antoine Dupret,*** *CEA-LETI-MINATEC, Grenoble, France*

Associate Chair: ***Subhasish Mitra,*** *Stanford University, Stanford, CA*

1:30 PM

24.1 A 0.6V 8mW 3D Vision Processor for a Navigation Device for the Visually Impaired DS2

D. Jeon[1,2], N. Ickes[1], P. Raina[1], H-C. Wang[1], A. Chandrakasan[1]

[1]Massachusetts Institute of Technology, Cambridge, MA

[2] now at Seoul National University, Suwon, Korea

2:00 PM

24.2 A 2.5GHz 7.7TOPS/W Switched-Capacitor Matrix Multiplier with Co-designed Local Memory in 40nm

E. H. Lee, S. S. Wong

Stanford University, Stanford, CA

2:30 PM

24.3 A 36.8 2b-TOPS/W Self-Calibrating GPS Accelerator Implemented Using Analog Calculation in 65nm LP CMOS

S. Skrzyniarz[1,2], L. Fick[2], J. Shah[2], Y. Kim[2], D. Sylvester[2], D. Blaauw[2], D. Fick[1], M. B. Henry[1]

[1]Isocline, Austin, TX

[2]University of Michigan, Ann Arbor, MI

Break 3:00 PM

mm-Wave THz Sensing

Session Chair: ***Brian Ginsburg,*** *Texas Instruments, Dallas, TX*
Associate Chair: ***Minoru Fujishima,*** *Hiroshima University, Hiroshima, Japan*

3:15 PM

25.1 A Fully Integrated 0.55THz Near-Field Sensor with a Lateral Resolution down to 8µm in 0.13µm SiGe BiCMOS
J. Grzyb[1], B. Heinemann[2], U. R. Pfeiffer[1]
[1]University of Wuppertal, Wuppertal, Germany
[2]IHP, Frankfurt, Germany

3:45 PM

25.2 A 210-to-305GHz CMOS Receiver for Rotational Spectroscopy
Q. Zhong, W. Choi, C. Miller, R. Henderson, K. K. O
University of Texas, Dallas, TX

4:15 PM

25.3 A 40-to-330GHz Synthesizer-Free THz Spectroscope-on-Chip Exploiting Electromagnetic Scattering
X. Wu, K. Sengupta
Princeton University, Princeton, NJ

4:45 PM

25.4 A 0.43K-Noise-Equivalent-ΔT 100GHz Dicke-Free Radiometer with 100% Time Efficiency in 65nm CMOS
A. Tang[1,2], Y. Kim[2], Q. J. Gu[1]
[1]University of California, Davis, CA
[2]Jet Propulsion Laboratory, Pasadena, CA

5:00 PM

25.5 A 320GHz Subharmonic-Mixing Coherent Imager in 0.13µm SiGe BiCMOS
C. Jiang[1], A. Mostajeran[1], R. Han[2], M. Emadi[3], H. Sherry[4], A. Cathelin[4], E. Afshari[1]
[1]Cornell University, Ithaca, NY
[2]Massachusetts Institute of Technology, Cambridge, MA
[3]Qualcomm, San Jose, CA
[4]STMicroelectronics, Crolles, France

Conclusion 5:15 PM

Wireless for IoE

Session Chair: ***Kenichi Okada,*** *Tokyo Institute of Technology, Tokyo, Japan*
Associate Chair: ***Jan van Sinderen,*** *NXP Semiconductors, Eindhoven, The Netherlands*

1:30 PM

26.1 A 5.5mW ADPLL-Based Receiver with Hybrid-Loop Interference Rejection for BLE Application in 65nm CMOS
H. Okuni, A. Sai, T. T. Ta, S. Kondo, T. Tokairin, M. Furuta, T. Itakura
Toshiba, Kawasaki, Japan

2:00 PM

26.2 An Ultra-Low-Power Receiver Using Transmitted-Reference and Shifted Limiters for In-Band Interference Resilience
D. Ye, R. van der Zee, B. Nauta, University of Twente, Enschede, The Netherlands

2:30 PM

26.3 A 1.3nJ/b IEEE 802.11ah Fully Digital Polar Transmitter for IoE Applications DS2
A. Ba, Y-H. Liu, J. van den Heuvel, P. Mateman, B. Busze, J. Gloudemans, P. Vis, J. Dijkhuis, C. Bachmann, G. Dolmans, K. Philips, H. de Groot
Holst Centre / imec, Eindhoven, The Netherlands

Break 3:00 PM

3:15 PM

26.4 A 160-to-960MHz ETSI Class-1-Compliant IoE Transceiver with 100dB Blocker Rejection, 70dB ACR and 800pA Standby Current
N. Kearney[1], C. Billon[1], M. Deeney[1], E. Evans[2], K. Khan[1], H. Li[3], S. Liang[2], K. Mulvaney[1], K. A. O'Donoghue[1], S. O'Mahony[1], P. Quinlan[1], S. Selvanayagam[2], S. Onkar[4], C. Agrawal[4]
[1]Analog Devices, Cork, Ireland; [2]Analog Devices, Newbury, United Kingdom
[3]Analog Devices, Wilmington, MA; [4]Analog Devices, Bangalore, India

3:30 PM

26.5 A 0.7V 1.5-to-2.3mW GNSS Receiver with 2.5-to-3.8dB NF in 28nm FD-SOI DS2
K. Yamamoto[1], K. Nakano[1], G. Hidai[1], Y. Kondo[1], H. Tomiyama[1], H. Takano[1], F. Kondo[1], Y. Shinohe[1], H. Takeuchi[1], N. Ozawa[1], S. Harada[2], S. Eto[2], M. Kishikawa[3], D. Ide[3], H. Tagami[3], M. Katakura[3], N. Shoji[1]
[1]Sony, Atsugi, Japan; [2]Sony LSI Design, Atsugi, Japan
[3]Sony LSI Design, Fukuoka, Japan

3:45 PM

26.6 A Programmable Receiver Front-End Achieving >17dBm IIP3 at <1.25×BW Frequency Offset
S. Hameed[1], N. Sinha[1], M. Rachid[2], S. Pamarti[1]
[1]University of California, Los Angeles, CA; [2]Silvus Technologies, Los Angeles, CA

4:15 PM

26.7 A 10mm³ Syringe-Implantable Near-Field Radio System on Glass Substrate
Y. Shi, M. Choi, Z. Li, G. Kim, Z. Foo, H-S. Kim, D. Wentzloff, D. Blaauw
University of Michigan, Ann Arbor, MI

4:45 PM

26.8 A 236nW -56.5dBm-Sensitivity Bluetooth Low-Energy Wakeup Receiver with Energy Harvesting in 65nm CMOS
N. E. Roberts[1], K. Craig[1], A. Shrivastava[1], S. N. Wooters[1], Y. Shakhsheer[1], B. H. Calhoun[1], D. D. Wentzloff[2]
[1]PsiKick, Charlottesville, VA; [2]PsiKick, Ann Arbor, MI

5:00 PM

26.9 A 0.038mm² SAW-less Multiband Transceiver Using an N-Path SC Gain Loop
G. Qi[1], P-I. Mak[1], R. P. Martins[1,2]
[1]University of Macau, Macau, China; [2]Instituto Superior Tecnico, Lisbon, Portugal

Conclusion 5:15 PM

Hybrid and Nyquist Data Converters

Session Chair: ***Stephane Le Tual,*** *STMicroelectronics, Crolles, France*
Associate Chair: ***Kostas Doris,*** *NXP Semiconductors, Eindhoven, The Netherlands*

1:30 PM

27.1 A 12b 2GS/s Dual-Rate Hybrid DAC with Pulsed Timing-Error Pre-Distortion and In-Band Noise Cancellation Achieving >74dBc SFDR up to 1GHz in 65nm CMOS
S. Su, M. S-W. Chen, University of Southern California, Los Angeles, CA

2:00 PM

27.2 An Oversampling SAR ADC with DAC Mismatch Error Shaping Achieving 105dB SFDR and 101dB SNDR over 1kHz BW in 55nm CMOS DS2
Y-S. Shu, L-T. Kuo, T-Y. Lo, MediaTek, Hsinchu, Taiwan

2:30 PM

27.3 Area-Efficient 1GS/s 6b SAR ADC with Charge-Injection-Cell-Based DAC
K. D. Choo, J. Bell, M. P. Flynn, University of Michigan, Ann Arbor, MI

2:45 PM

27.4 A 0.35mW 12b 100MS/s SAR-Assisted Digital Slope ADC in 28nm CMOS
C-C. Liu, MediaTek, Hsinchu, Taiwan

Break 3:00 PM

3:15 PM

27.5 A 4GS/s Time-Interleaved RF ADC in 65nm CMOS with 4GHz Input Bandwidth
M. Straayer[1], J. Bales[2], D. Birdsall[2], D. Daly[1], P. Elliott[2], B. Foley[1], R. Mason[2], V. Singh[3], X. Wang[2]
[1]Maxim Integrated Products, North Chelmsford, MA
[2]Maxim Integrated Products, Fort Collins, CO
[3]Maxim Integrated Products, San Jose, CA

3:45 PM

27.6 A 4GS/s 13b Pipelined ADC with Capacitor and Amplifier Sharing in 16nm CMOS
J. Wu[1,2], A. Chou[1], T. Li[1], R. Wu[1], T. Wang[1], G. Cusmai[1], S-T. Lin[3], C-H. Yang[3], G. Unruh[1], S. R. Dommaraju[1], M. M. Zhang[1], P. T. Yang[3], W-T. Lin[3], X. Chen[1], D. Koh[1], Q. Dou[1], H. M. Geddada[1], J-J. Hung[1], M. Brandolini[1], Y. Shin[1], H-S. Huang[3], C-Y. Chen[1], A. Venes[1]
[1]Broadcom, Irvine, CA
[2]now with Tongji University, Shanghai, China
[3]Broadcom, Hsinchu, Taiwan

4:15 PM

27.7 A 10b 2.6GS/s Time-Interleaved SAR ADC with Background Timing-Skew Calibration
C-Y. Lin, Y-H. Wei, T-C. Lee
National Taiwan University, Taipei, Taiwan

4:45 PM

27.8 A 0.076mm² 12b 26.5mW 600MS/s 4×-Interleaved Subranging SAR-ΔΣ ADC with On-Chip Buffer in 28nm CMOS
A. Venca, N. Ghittori, A. Bosi, C. Nani
Marvell, Pavia, Italy

Conclusion 5:15 PM

Biological Sensors for Point of Care

Session Chair: ***Peter Chung-Yu Wu,*** *National Chiao Tung University, Hsinchu, Taiwan*
Associate Chair: ***Jan Genoe,*** *imec, Leuven, Belgium*

1:30 PM

28.1 A Handheld 50pM-Sensitivity Micro-NMR CMOS Platform with B-Field Stabilization for Multi-Type Biological/Chemical Assays DS2

K-M. Lei[1], H. Heidari[2,3], P-I. Mak[1], M-K. Law[1], F. Malobert[2], R. P. Martins[1,4]
[1]University of Macau, Macau, China
[2]University of Pavia, Pavia, Italy
[3]University of Glasgow, Glasgow, United Kingdom
[4]Instituto Superior Tecnico, Lisbon, Portugal

2:00 PM

28.2 A 14GHz Battery-Operated Point-of-Care ESR Spectrometer Based on a 0.13µm CMOS ASIC DS2

J. Handwerker, B. Schlecker, U. Wachter, P. Radermacher, M. Ortmanns, J. Anders
University of Ulm, Ulm, Germany

2:30 PM

28.3 CMOS Biosensor IC Focusing on Dielectric Relaxations of Biological Water with 120GHz and 60GHz Oscillator Arrays DS2

T. Mitsunaka[1], N. Ashida[1], A. Saito[1], K. Iizuka[1], T. Suzuki[2], Y. Ogawa[2], M. Fujishima[3]
[1]SHARP, Tenri, Japan
[2]Kyoto University, Kyoto, Japan
[3]Hiroshima University, Higashi-Hiroshima, Japan

Break 3:00 PM

3:15 PM

28.4 A Battery-Powered Efficient Multi-Sensor Acquisition System with Simultaneous ECG, BIO-Z, GSR, and PPG DS2

M. Konijnenburg[1], S. Stanzione[1], L. Yan[2], D-W. Jee[2], J. Pettine[1], R. Van Wegberg[1], H. Kim[2], C. van Liempd[1], R. Fish[3], J. Schluessler[3], H. de Groot[1], C. Van Hoof[1,2], R. F. Yazicioglu[2], N. Van Helleputte[2]
[1]Holst Centre / imec, Eindhoven, The Netherlands
[2]imec, Leuven, Belgium
[3]Samsung Electronics, Menlo Park, CA

3:45 PM

28.5 A 0.6V 0.015mm² Time-Based Biomedical Readout for Ambulatory Applications in 40nm CMOS

R. Mohan[1,2], S. Zaliasl[3], G. Gielen[1,2], C. Van Hoof[1,2], N. Van Helleputte[1], R. F. Yazicioglu[1]
[1]imec, Leuven, Belgium
[2]KU Leuven, Leuven, Belgium
[3]Holst Centre / imec, Eindhoven, The Netherlands

4:15 PM

28.6 A ±50mV Linear-Input-Range VCO-Based Neural-Recording Front-End with Digital Nonlinearity Correction

W. Jiang[1], V. Hokhikyan[1], H. Chandrakumar[1], V. Karkare[2], D. Markovic[1]
[1]University of California, Los Angeles, CA
[2]Silicon Laboratories, Sunnyvale, CA

4:45 PM

28.7 CMOS Monolithic Airborne-Particulate-Matter Detector Based on 32 Capacitive Sensors with a Resolution of 65zF rms

P. Ciccarella, M. Carminati, M. Sampietro, G. Ferrari
Politecnico di Milano, Milano, Italy

Conclusion 5:15 PM

ISSCC 2016 Short Course
Circuits for the Internet of Everything

Organizer: **Wim Dehaene,** *KU Leuven, Leuven, Belgium*

The Internet of Everything (IoE) is today one of the main drivers for further development in the semiconductor industry. Academic research is also focusing on this application domain. The Internet of Everything poses new challenges to circuit design mainly for the creation of energy efficient design of IoE nodes. The holistic view on IoE projects the presence of several layers of hardware in the IoE system ranging from tiny sensor nodes all around in the environment, over user terminals to huge server infrastructure. The layer closest to the physical world is that of the sensor nodes. For these nodes to be omnipresent, they will have to be running on an independent supply – either batteries that last for years or energy harvesting. Ultra-efficient, low-energy design is a key asset in this context.

This short course aims to give an overview of the challenges that modern circuit design has to face, and the solutions it can offer, in the context of design for the Internet of Everything. The course will start by addressing the topic of "processors for IoE". The typical needs for digital processing in an IoE node will be discussed. In this part the general picture of circuits for IoE will also be sketched. The second topic addresses the radio design for IoE, followed by sensor interfaces and time references. These three circuit classes are essential parts of any IoE node and also comprise the core challenges of circuit design for the IoE.

Short Course Agenda

Time:	Topic:
8:00 AM	Breakfast
8:20 AM	Introduction by Chair
8:30 AM	**Processors for the Internet of Everything** ***Shichin Ouyang,*** *MediaTek, USA, San Jose, CA*
10:00 AM	Break
10:30 AM	**Radios for IoT** ***Hooman Darabi,*** *Broadcom Corporation, Irvine, CA*
12:15 PM	Lunch
1:20 PM	**Sensor Interfaces for IoE** ***Nick Van Helleputte,*** *imec, Leuven, Belgium*
2:50 PM	Break
3:20 PM	**Frequency References for IoE** **Fabio Sebastiano,** *Delft University of Technology, Delft, The Netherlands*
4:50 PM	Conclusion

Processors for the Internet of Everything

Shichin Ouyang, *MediaTek, USA, San Jose, CA*

Application processors used in desktop or mobile devices focus mainly on delivering highest performance with highest power efficiency. However, processors in today's IoE SoCs also need to provide real-time processing and responsiveness, high scalability and high configurability to meet a variety of IoE application uses, high flexibility to integrate the user's own in-house features and high-security features at each level and each node on the connected systems to avoid attack or error conditions. The focus of optimization on IoE processors therefore depends heavily on application scenarios and SoC architectures, with emphasis on ultra-low-power operation. The presentation will review the IoE processor challenges mentioned above, summarize some of the well-known solutions currently in use, and introduce recently developed SoC architectures, systems, physical implementations, and circuit innovations.

About the presenter*:*
Shichin Ouyang received his B.S. from National TsingHua University, Taiwan, and his M.S. from Stanford University, CA, both in Electrical Engineering. He has been working with MediaTek Inc since 2008, where he is currently a Deputy Director of CPU design and implementation division of MediaTek, Singapore. Before joining MediaTek, he was with SUN Microsystems from 1999 to 2008 as a timing lead and a digital circuit designer on multiple Ultra-Sparc processors. At MediaTek, his team was responsible for delivering the first quad-core Cortex-A7 Smartphone processor and first Heterogeneous Multi-processor Big-Little for tablet. His division's current focus is on design and implementation of processor subsystems to achieve the low power goals for IoE/wearable SoCs.

Radios for IoT

Hooman Darabi, *Broadcom Corporation, Irvine, CA*

At the heart of the IoE network are the radios that enable a reliable and secure connection between the objects. An IoE radio must, however, satisfy very exacting specifications. Low cost, very low power consumption, and small physical size are among the critical requirements to enable a reliable and efficient IoE system. In this part of the course we offer architectural and circuit-level considerations of both receivers and transmitters for IoE applications. An overview of IoE radio requirements along with system-level analysis of suitable architectures is offered. Key radio circuits are presented, followed by several case studies and a detailed discussion of their pros and cons.

About the presenter:
Hooman Darabi received the BS and MS degrees both in Electrical Engineering from Sharif University of Technology, Tehran in 1994, and 1996 respectively. He received the Ph.D. degree in electrical engineering from the University of California, Los Angeles, in 1999. He is currently a Sr. Technical Director, and a Fellow, with Broadcom Corporation, Irvine, CA. He is also an adjunct professor with the University of California, Los Angeles. His interests include analog and RF IC design for wireless communications. Hooman is an IEEE Fellow, and served as an IEEE distinguished lecturer from 2012-2014. He is the author of the book RF Integrated Circuits and Systems.

Sensor interfaces for IoE

Nick Van Helleputte, *imec, Leuven, Belgium*

While IoE spans very diverse and broad application domains, a lot of those require extensive sensing. Individual nodes in the IoE can be equipped with a multitude of diverse sensors like gas, temperature, humidity, pressure, position and various biomedical sensors. Area-efficient, high-performance and low-power sensor interface design is thus an important prerequisite for successful deployment of the IoE. This short course chapter will address exactly these topics. A brief overview of various sensor types and how to interface them will be discussed. The unique design challenges for sensor interfaces will be addressed. The short course will discuss in depth state-of-the-art instrumentation amplifier designs as well as transimpedance amplifier designs, both of which are at the heart of sensor interfaces. Advanced circuit design techniques like chopping, bootstrapping, and offset cancellation will be explained. Finally, a look into novel and promising research areas like time-domain sensor interface design will conclude the short course.

About the presenter*:*
Nick Van Helleputte received the MS degree in electrical engineering in 2004 from the Katholieke Universiteit Leuven, Belgium. He received his Ph.D. degree from the same institute in 2009 with research on RF and analog circuits for (ultra-)wideband low-power wireless receivers. He joined imec in 2009 as an Analog R&D Design Engineer and is currently team leader of biomedical circuits and systems at imec. His research focus is on ultra-low-power circuits for biomedical applications.

Frequency References for IoE

Fabio Sebastiano, *Delft University of Technology, Delft, The Netherlands*

The IoE nodes need radios that are small, cheap and energy efficient. Frequency references are required for those radios to select the right band for wireless communication. Moreover, a frequency reference enables time synchronization between the nodes in the IoE network, which allows the radio to turn off when transmission or reception are not expected, thus resulting in power saving. Highly accurate frequency references can be implemented using quartz crystals but since such external components would limit the miniaturization and energy efficiency of IoE nodes, fully integrated alternatives must be adopted. In addition, such references must guarantee the required accuracy over the wide temperature range expected in several IoE applications and over the supply voltage variations caused by the energy scavengers or the batteries powering the IoE node. This last part of the short course will present the requirements for such fully integrated frequency references and review several alternatives for their implementation. The main sources of inaccuracy and the techniques to minimize their effect will be analyzed, with particular emphasis on supply sensitivity and temperature compensation.

About the presenter:
Fabio Sebastiano holds degrees from the University of Pisa, Italy (B.Sc., 2003 - M.Sc., 2005), from Sant'Anna School of Advanced Studies, Pisa, Italy (M.Sc., 2006) and from Delft University of Technology, The Netherlands (Ph.D., 2011). From 2006 to 2013, he was with NXP Semiconductors Research in Eindhoven, The Netherlands, where he conducted research on fully integrated CMOS frequency references, deep-submicron temperature sensors and area-efficient interfaces for magnetic sensors. In 2013, he joined Delft University of Technology, where he is currently an Assistant Professor. His main research interests are sensor read-outs, fully integrated frequency references and cryogenic electronics.

F3: Radio Architectures and Circuits Towards 5G

Organizer: **Stefano Pellerano,** *Intel, Hillsboro, OR*

Committee: **Ahmad Mirzaei**, *Broadcom, Irvine, CA*
Chih-Ming Hung, *MediaTek, Taipei, Taiwan*
Jan Craninckx, *IMEC, Leuven, Belgium*
Kenichi Okada, *Tokyo Institute of Technology, Tokyo, Japan*
Vojkan Vidojkovic *Intel Mobile Communications, Duisburg, Germany*

In the last two decades data-rates in wireless communication systems have been increasing exponentially. This trend is continuing with the fifth generation of wireless systems (5G) that will require peak rates in excess of Gb/s for many users, several hundred thousands of simultaneous connections for massive sensor deployments, and substantially improved spectral efficiency, coverage and signaling. How will the wireless technology deliver these promises? This forum will focus on current state-of-the-art and future directions of the key circuit techniques and system architectures that will enable the 5G revolution, including advanced MIMO, carrier aggregation, mm-Wave radios, large phased-array transceivers, and in-band full duplex operation. Compact low-loss front-end modules for future 5G systems will also be addressed.

Forum Agenda

Time:	Topic:
8:00 AM	Breakfast
8:20 AM	Introduction by Chair
8:30 AM	**Overview of 5G Requirements and Future Wireless Networks** ***Sven Mattisson,*** *Ericsson, Lund, Sweden*
9:20 AM	**5G Technologies and Deployment in 2020 and Beyond** ***Takehiro Nakamura,*** *NTT DoCoMo, Kanagawa, Japan*
10:10 AM	Break
10:35 AM	**RX Architectures and Circuits Towards 5G – A Path Towards 100 Receivers** ***Aleksandar Tasic,*** *Qualcomm, San Diego, CA*
11:25 AM	**TX architecture and Circuits Towards 5G** ***Zdravko Boos,*** *Intel, Munich, Germany*
12:15 PM	Lunch
1:20 PM	**Design Techniques for Reduced Cross-Talk in Carrier-Aggregation Systems** ***Masoud Kahrizi****, Broadcom, Irvine, CA*
2:10 PM	**In-Band Full Duplex: System Considerations and Transceiver Design** ***Bram Nauta,*** *University of Twente, Enschede, The Netherlands*
3:00 PM	Break
3:20 PM	**mm-Wave Beamforming Transceivers** ***Hossein Hashemi,*** *University of Southern California, Los Angeles, CA*
4:10 PM	**Compact Low-Loss Front-End Modules for Future 5G Systems** ***Makoto Kawashima,*** *Murata, Kyoto, Japan*
5:00 PM	Closing remarks by Chair

F4: Emerging Short-Reach and High-Density Interconnect Solutions for Internet of Everything

Organizer: **Ichiro Fujimori,** *Broadcom, Irvine, CA*

Committee: **Martin Brox,** *Micron, Munich, Germany*
Elad Alon, *University of California, Berkeley, Berkeley, CA*
Pavan Hanumolu, *University of Illinois, Urbana-Champaign, Urbana, IL*
Gerritt den Besten, *NXP Semiconductors, Eindhoven, The Netherlands*
Hideyuki Nosaka, *NTT Atsugi, Japan*

Ubiquitous connectivity within devices ranging from miniature sensors to racks for cloud data-centers is critical to enabling the "Internet of Everything". Industry predictions suggest that the number of IoE devices may reach 200 billion by 2020, further increasing the demands placed on high-speed networks. Power-efficient short-reach interconnect solutions will be required to support everything from sensor interfaces to mobile platforms to core computation. Furthermore, high-density chip-to-chip solutions will be required to support communication and computation associated with massively-scaled data traffic, demanding the use of emerging technologies such as 2.5D/3D heterogeneous integration, and new high bandwidth memories. The combination of all of these requirements will demand new circuit and system architectures in the electrical, optical, and contactless arenas. This forum will explore advances in such emerging interconnect solutions for the Internet of Everything.

Forum Agenda

Time:	Topic:
8:00 AM	Breakfast
8:20 AM	**Introduction** ***Ichiro Fujimori,*** *Broadcom, Irvine, CA*
8:30 AM	**Heterogeneous System Integration Using Silicon Interposer and 3D Stacking Technology** ***Eric Beyne,*** *imec, Leuven, Belgium*
9:15 AM	**The Hybrid Memory Cube (HMC) 480G Short Reach Interface** ***Marlon Gunderson,*** *Micron Technology, Minneapolis, MN*
10:00 AM	Break
10:20 AM	**High Bandwidth Memory (HBM) Stacked DRAM Interfaces** ***Dong Uk Lee,*** *SK Hynix, Icheon, Korea*
11:05 AM	**Power-Efficient Parallel Interfaces for High-Density Short Reach Interconnects** ***Tod Dickson,*** *IBM, Yorktown Heights, NY*
11:50 AM	Lunch
12:55 PM	**Near-Field Coupling Integration Technology** ***Tadahiro Kuroda,*** *Keio University, Tokyo, Japan*
1:40 PM	**50 Gbits/sec: The Next Mainstream Wireline Interconnect Lane Bit Rate** ***Chris Cole,*** *Finisar, Sunnyvale, CA*
2:25 PM	Break
2:45 PM	**High-Speed and Low-Power SerDes Architectures Using Chord Signaling** ***Amin Shokrollahi,*** *Kandou Bus, Lausanne, Switzerland*
3:30 PM	**CMOS Photonics for Ultra-Dense Communication** ***Vladimir Stojanovic,*** *UC Berkeley, Berkeley, CA*
4:15 PM	**Rapid-on/off Burst-Mode Interconnects for Power Scalable Servers and Mobile Platforms** ***Tejasvi Anand,*** *Oregon State University, Corvallis, OR*
5:00 PM	Conclusion

F5: Advanced IC Design for Ultra-Low-Noise Sensing

Organizer: **Makoto Ikeda,** *The University of Tokyo, Tokyo, Japan*

Committee: **David Stoppa**, *Fondazione Bruno Kessler, Trento, Italy*
Michiel Pertijs, *TU Delft, Delft, The Netherlands*
Yusuke Oike, *Sony, Kanagawa, Japan*
Maurits Ortmanns, *University of Ulm, Ulm, Germany*
Vadim Ivanov, *Texas Instruments, Tucson, AZ*
Fu-Lung Hsueh, *TSMC, Hsinchu,Taiwan*

This Forum is intended to provide an in-depth overview of noise modeling and simulation, and of analog, mixed-signal, and system-level solutions for low-noise sensing. State-of-the-art techniques to tackle noise in image sensors, mechanical sensors, temperature sensors, magnetic sensors and bio-sensors will be critically analyzed. The forum will explicitly address the trade-off between noise and energy consumption in such sensors, thus providing the audience with valuable insight into the design of sensor interfaces for the Internet of Everything.

Forum Agenda

Time	Topic
8:00 AM	Breakfast
8:30 AM	**Introduction** ***Makoto Ikeda,*** *The University of Tokyo, Tokyo, Japan*
8:35 AM	**NOISE: You Love It or You Hate It** ***Albert Theuwissen,*** *Harvest Imaging, Belgium & Delft University of Technology, Delft,The Netherlands*
9:20 AM	**Low-Noise Energy-Efficient Amplifier Design** ***Willy Sansen,*** *KULeuven, Leuven, Belgium*
10:05 AM	Break
10:30 AM	**Energy-Efficient High-Resolution ADCs** ***Youngcheol Chae,*** *Yonsei University, Seoul, Korea*
11:15 AM	**Readout Circuits for Capacitive MEMS Sensors** ***Vladimir Petkov,*** *Robert Bosch Research and Technology Center, Palo Alto, CA*
12:00 PM	Lunch
1:00 PM	**Low-Noise Image Sensors** ***Shoji Kawahito,*** *Shizuoka University, Hamamatsu, Japan*
1:45 PM	**Designing High-Resolution CMOS Temperature Sensors** ***Kofi Makinwa,*** *Delft University of Technology, Delft, The Netherlands*
2:30 PM	Break
2:50 PM	**Low-Noise Isolated Current Sensing Using Integrated Fluxgate Magnetometers** ***Martijn Snoeij,*** *Texas Instruments, Freising, Germany*
3:35 PM	**The Design of Low-power, High-Resolution Biomedical Sensors and Interfaces** ***Tim Denison,*** *Medtronic PLC, Minneapolis, MN*
4:20 PM	**Noise in Single-Photon-Counting Image Sensors** ***Neale A.W. Dutton,*** *STMicroelectronics, Edinburgh, United Kingdom*
5:05 PM	Closing Remarks

F6: Circuit, Systems and Data Processing for Next-Generation Wearable and Implantable Medical Devices

Organizers: **Kush Gulati,** *Omni Design Technologies, Milpitas, CA*
Firat Yazicioglu, *GlaxoSmithKline, Herent, Belgium*

Committee: **Antoine Dupret,** *CEA LIST, Yvette, France*
Roman Genov, *University of Toronto, Toronto, Canada*
Peter Chung-Yu Wu, *National Chiao Tung University, Hsinchu, Taiwan*
Long Yan, *Samsung Electronics, Hwaseong, Korea*

There are exciting new developments in health care wearables, fitness trackers and therapeutic implantable devices. This advancement is fueled, in part, by the miniaturization of sensors and associated electronics. One of the greatest opportunities in wearables and implanted devices is the wealth of data that can be extracted from these devices and the high-quality information that can emerge by combining data from multiple sources for effective utilization by physicians. Longitudinal data, generated by continuous monitoring of physiological and vital parameters, can increase therapy efficacy and lead to the invention of new biomarkers. However, continuous and unobtrusive monitoring requires extreme miniaturization and minimal dependence on energy constraints. This creates challenges on integrated circuits and requires new techniques directed towards lowering energy consumption and reducing area and volume. This forum will provide an overview of the challenges of the various systems, circuits and heterogeneous technologies that are essential for building next generation on- and in-body medical devices.

Forum Agenda

Time	Topic
8:00 AM	Breakfast
8:20 AM	**Introduction** ***Kush Gulati,*** *Omni Design Technologies, Milpitas, CA*
8:30 AM	**Living Longer and Healthier:** **Persuasive Wearable Technology for Prevention, Cure and Care** ***Chris Van Hoof,*** *imec and KULeuven, Leuven, Belgium*
9:20 AM	**Closed Loop and Context Aware Therapeutic Implants** ***Michel Decré,*** *Medtronic Eindhoven Design Center, Eindhoven, The Netherlands*
10:10 AM	Break
10:35 AM	**Making Sense of the Signals: Algorithms and Platforms for Data-Driven Analysis of Medical-Sensor Signals** ***Naveen Verma,*** *Princeton University, Princeton, NJ*
11:25 AM	**Home-Use Sensors as a Means to Dramatically Cut Clinical Research Costs** ***Jose Bohorquez,*** *Skulpt, San Francisco, CA*
12:15 PM	Lunch
1:20 PM	**Self-Powered Implantable Biomedical Electronics Enabled by Flexible Piezoelectric Energy Harvesting** ***Keon Jae Lee,*** *KAIST, Daejeon, Korea*
2:10 PM	**Miniaturization of Medical Implantable Devices and Products** ***Eric Chow,*** *Cyberonics, Houston, TX*
3:00 PM	Break
3:20 PM	**Ultra-Low Power Wireless Systems for Biological and Physiological Monitoring** ***Alison Burdett,*** *Toumaz Group, Oxford, United Kingdom*
4:10 PM	**Implantable Neurotechnologies for Electroceuticals: Integrating Micro/Nano, VLSI, Data/Power, Systems** ***Nitish Thakor,*** *SINAPSE Institute, Singapore; Johns Hopkins University, Baltimore, MD*
5:00 PM	Closing Remarks

INTERNATIONAL TECHNICAL PROGRAM COMMITTEE

EXECUTIVE COMMITTEE

CONFERENCE CHAIR
Anantha Chandrakasan, Massachusetts Institute of Technology, Cambridge, MA

EXECUTIVE COMMITTEE SECRETARY, DATA TEAM CHAIR
SeongHwan Cho, KAIST, Daejeon, Korea

PRESS COORDINATOR
Alison Burdett, Toumaz Microsystems, Abingdon, United Kingdom

WEB SITE AND A/V CHAIR
Trudy Stetzler, Houston, TX

DIRECTOR OF FINANCE AND BOOK DISPLAY COORDINATOR
Bryant Griffin, Penfield, NY

PROGRAM CHAIR
Kevin Zhang, Intel, Hillsboro, OR

PROGRAM VICE-CHAIR
Boris Murmann, Stanford University, Stanford, CA

STUDENT FORUM CHAIR AND UNIVERSITY RECEPTIONS
Jan van der Spiegel, University of Pennsylvania, Philadelphia, PA

DEMONSTRATION SESSION CHAIR
Uming Ko, MediaTek, Austin TX

ITPC FAR EAST REGIONAL CHAIR
Tsung-Hsien Lin, National Taiwan University, Taipei, Taiwan

ITPC FAR EAST REGIONAL VICE-CHAIR
Atsuki Inoue, Fujitsu, Kawasaki, Japan

ITPC EUROPEAN REGIONAL CHAIR
Maurits Ortmanns, University of Ulm, Institute of Microelectronics, Ulm, Germany

ITPC EUROPEAN REGIONAL VICE CHAIR
David Stoppa, Fondazione Bruno Kessler, Trento, Italy

ADCOM REPRESENTATIVE
Bryan Ackland, Stevens Institute of Technology, Hoboken, NJ

DIRECTOR OF PUBLICATIONS AND PRESENTATIONS
Laura Fujino, University of Toronto, Toronto, Canada

PRESS LIAISON AND ARC CHAIR
Kenneth C. Smith, University of Toronto, Toronto, Canada

FORUMS CHAIR
Andreia Cathelin, STMicroelectronics, Crolles, France

EDUCATIONAL EVENTS CHAIR (SHORT COURSE/TUTORIALS)
Ali Sheikholeslami, University of Toronto, Toronto, Canada

DIRECTOR OF OPERATIONS
Melissa Widerkehr, Widerkehr and Associates, Montgomery Village, MD

TECHNICAL EDITORS

Jason H. Anderson, University of Toronto, Toronto, Canada
Leonid Belostotski, The University of Calgary, Calgary, Canada
Dustin Dunwell, Kapik Integration, Toronto, Canada
Vincent Gaudet, University of Waterloo, Waterloo, Canada
Glenn Gulak, University of Toronto, Toronto, Canada
James W. Haslett, The University of Calgary, Calgary, Canada
Dave Halupka, Kapik Integration, Toronto, Canada
Kostas Pagiamtzis, Semtech, Burlington, Canada
Kenneth C. Smith, University of Toronto, Toronto, Canada

MULTI-MEDIA COORDINATOR

Dave Halupka, Kapik Integration, Toronto, Canada

INTERNATIONAL TECHNICAL PROGRAM COMMITTEE

PROGRAM CHAIR:
Kevin Zhang, Intel, Hillsboro, OR

PROGRAM VICE CHAIR:
Boris Murmann, Stanford University, Stanford, CA

ANALOG SUBCOMMITTEE

Chair: Axel Thomsen, Cirrus Logic, Austin, TX
Anton Bakker, Arctic Sand, San Jose, CA
Marco Berkhout, NXP Semiconductors, Nijmegen, The Netherlands
Yuan Gao, IME, A*STAR, Singapore
Zhilian Hong, Fudan University, Shanghai, China
Vadim Ivanov, Texas Instruments, Tucson, AZ
Xicheng Jiang, Broadcom, Irvine, CA
Tsung-Hsien Lin, National Taiwan University, Taipei, Taiwan
Dragan Maksimovic, University of Colorado, Boulder, CO
Piero Malcovati, University of Pavia, Pavia, Italy
Philip Mok, HKUST, Clear Water Bay, Hong Kong
Makoto Nagata, Kobe University, Kobe, Japan
Jaejin Park, Samsung Electronics, Hwasung, Korea
Tim Piessens, ICsense, Leuven, Belgium
Edgar Sanchez Sinencio, Texas A&M University, College Station, TX
Christoph Sandner, Infineon Technologies, Villach, Austria
Stefano Stanzione, IMEC-NL, Eindhoven, The Netherlands
Makoto Takamiya, University of Tokyo, Tokyo, Japan

DATA CONVERTERS SUBCOMMITTEE

Chair: Un-Ku Moon, Oregon State University, Corvallis, OR
Kostas Doris, NXP, Eindhoven, The Netherlands
Pieter Harpe, Eindhoven University of Technology, Eindhoven, The Netherlands
Tetsuya Iizuka, University of Tokyo, Tokyo, Japan
Tai-Cheng Lee, National Taiwan University, Taipei, Taiwan
Hae-Seung Lee, Massachusetts Institute of Technology, Cambridge, MA
Stéphane Le Tual, STMicroelectronics, Crolles, France
Takahiro Miki, Renesas Electronics, Tokyo, Japan
Gerhard Mitteregger, MediaTek Wireless, West Malling, United Kingdom
Jan Mulder, Broadcom, Bunnik, The Netherlands
Ken Nishimura, Keysight Technologies, Santa Clara, CA
Maurits Ortmanns, University of Ulm, Ulm, Germany
Seung-Tak Ryu, KAIST, Daejeon, Korea
Richard Schreier, Analog Devices, Toronto, Canada
Venkatesh Srinivasan, Texas Instruments, Dallas, TX
Matt Straayer, Maxim Integrated Products, North Chelmsford, MA
Seng-Pan U (Ben), University of Macau, Taipa, Macau

DIGITAL ARCHITECTURES & SYSTEMS (DAS) SUBCOMMITTEE

Chair: Stephen Kosonocky, Advanced Micro Devices, Fort Collins, CO
David Flynn, ARM, Cambridge, United Kingdom
Takashi Hashimoto, Panasonic, Osaka, Japan
Paul Liang, MediaTek, Hsinchu, Taiwan
Dejan Markovic, UCLA, Los Angeles, CA
Mahesh Mehendale, Texas Instruments, Bangalore, India
Byeong-Gyu Nam, Chungnam National University, Daejeon, Korea
Michael Polley, Samsung, Richardson, TX
Luke Shin, Oracle, Santa Clara, CA
Marian Verhelst, KU Leuven, Heverlee, Belgium

DIGITAL CIRCUITS (DCT) SUBCOMMITTEE

Chair: Stefan Rusu, TSMC, San Jose, CA
Edith Beigné, CEA-LETI, Grenoble, France
Vivek De, Intel, Hillsboro, OR
Eric Fluhr, IBM, Austin, TX
Atsuki Inoue, Fujitsu, Kawasaki, Japan
Yusuf Leblebici, Swiss Federal Institute of Technology, Lausanne, Switzerland
John Maneatis, True Circuits, Los Altos, CA
Bing Sheu, National Chiao Tung University, Hsinchu, Taiwan
Yasuhisa Shimazaki, Renesas, Tokyo, Japan
Youngmin Shin, Samsung, Hwansung, Korea
Dennis Sylvester, University of Michigan, Ann Arbor, MI
Kathy Wilcox, AMD, Boxborough, MA

IMMD SUBCOMMITTEE

Chair: Makoto Ikeda, University of Tokyo, Tokyo, Japan
Ralf Brederlow, Texas Instruments, Freising, Germany
Yoon-Kyung Choi, Samsung, Hwaseong, Korea
Peng Cong, Google, Mountain View, CA
Jun Deguchi, Toshiba, Kawasaki, Japan
Keith Fife, 4Catalyzer, Guilford, CT
Roman Genov, University of Toronto, Toronto, Canada
TaeChan Kim, Korea University, Yongin, Korea
Pedram Lajevardi, Robert Bosch, Palo Alto, CA
Wentai Liu, UCLA, Los Angeles, CA
Yoshiharu Nakajima, Japan Display, Kanagawa, Japan
Yusuke Oike, Sony, Kanagawa, Japan
Michiel Pertijs, TU Delft, Delft, The Netherlands
Joseph Shor, Bar Ilan University, Ramat Gan, Israel
David Stoppa, Fondazione Bruno Kessler, Trento, Italy
Peter Chung-Yu Wu, National Chiao Tung, University, Hsinchu City, Taiwan
Yong Ping Xu, National University of Singapore, Singapore
Refet Firat Yazicioglu, GlaxoSmithKline, Herent, Belgium

MEMORY SUBCOMMITTEE

Chair: Leland Chang, IBM T. J. Watson Research Center, Yorktown Heights, NY
Martin Brox, Micron, Munchen, Germany
Jonathan Chang, TSMC, Hsinchu, Taiwan
Sungdae Choi, SK Hynix Semiconductor, Icheon, Korea
Fatih Hamzaoglu, Intel, Hillsboro, OR
Jin-Man Han, Samsung Electronics, Hwasung, Korea
Uksong Kang, Samsung, Hwaseong, Korea
Atsushi Kawasumi, Toshiba, Kawasaki, Japan
Chulwoo Kim, Korea University, Seoul, Korea
Takashi Kono, Renesas, Tokyo, Japan
Hugh Mair, MediaTek, Fairview, TX
Chun Shiah, Etron, Hsinchu, Taiwan
Rob Sprinkle, Google, Mountain View, CA
Takefumi Yoshikawa, National Institute of Technology, Nagano College, Nagano, Japan

RF SUBCOMMITTEE

Chair: Piet Wambacq, imec, Heverlee, Belgium
Minoru Fujishima, Hiroshima University, Hiroshima, Japan
Xiang Gao, Marvell, Santa Clara, CA
Brian Ginsburg, Texas Instruments, Dallas, TX
Payam Heydari, University of California, Irvine, Irvine, CA
Chih-Ming Hung, MediaTek, Taipei, Taiwan
Tae Wook Kim,Yonsei University, Seoul, Korea
Harish Krishnaswamy, Columbia University in the City of New York, New York, NY
Antonio Liscidini, Univeristy of Toronto, Toronto, Canada
Andrea Mazzanti, Università di Pavia, Pavia, Italy
Ahmad Mirzaei, Broadcom, Irvine, CA
Kohei Onizuka, Toshiba, Kawasaki, Japan
Ullrich Pfeiffer, University of Wuppertal, Wuppertal, Germany
Jiayoon Zhiyu Ru, Broadcom, Irvine, CA
Jussi Ryynanen, Aalto University, Espoo, Finland
Carlo Samori, Politecnico di Milano, Milano, Italy
Hyunchol Shin, Kwangwoon University, Seoul, Korea
Vojkan Vidojkovic, Intel Mobile Communications, Duisburg, Germany

TECHNOLOGY DIRECTIONS SUBCOMMITTEE

Chair: Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands
Antoine Dupret, CEA LIST, Yvette, France
Hiroshi Fuketa, AIST, Ibaraki, Japan
Jan Genoe, imec, Leuven, Belgium
Kush Gulati, Omni Design, Milpitas, CA
Fu-Lung Hsueh, TSMC, Hsinchu,Taiwan
Shahriar Mirabbasi, University of British, Columbia, Vancouver, Canada
Subhasish Mitra, Stanford University,Stanford, CA
Masato Motomura, Hokkaido University, Sapporo, Japan
Shuichi Nagai, Panasonic, Osaka, Japan
Pirooz Pavarandeh, Genia, Santa Clara, CA
Yogesh K. Ramadass, Texas Instruments, San Jose, CA
Patrick Reynaert, KU Leuven, Leuven, Belgium
David Ruffieux, CSEM, Neuchated, Switzerland
Alice Wang, MediaTek, Hsinchu, Taiwan
Long Yan, Samsung Electronics, Hwaseong, Korea

WIRELESS SUBCOMMITTEE

Chair: Aarno Pärssinen, University of Oulu, Espoo, Finland

Ali Afsahi, Broadcom, San Diego, CA
Pierre Busson, ST Microelectronics, Crolles, France
Jan Craninckx, IMEC, Leuven, Belgium
Guang-Kaai Dehng, Mediatek, Hsinchu, Taiwan
Danielle Griffith, Texas Instruments, Richardson, TX
Chun-Huat Heng, National University of Singapore, Singapore
Eric Klumperink, University of Twente, Enschede, The Netherlands
Kyoo Hyun Lim, FCI, Seongnam, Korea
Li Lin, Marvell Semiconductor, Santa Clara, CA
Alyosha Molnar, Cornell University, Ithaca, NY
Kenichi Okada, Tokyo Institute of Technology, Tokyo, Japan
Stefano Pellerano, Intel, Hillsboro, OR
Woogeun Rhee, Tsinghua University, Beijing, China
Yuu Watanabe, Denso, Tokyo, Japan
Jan Van Sinderen, NXP Semiconductors, Eindhoven, The Netherlands

WIRELINE SUBCOMMITTEE

Chair: Daniel Friedman, IBM Thomas J. Watson Research Center, Yorktown Heights, NY

Elad Alon, University of California, Berkeley, Berkeley, CA
Ajith Amerasekera, Texas Instruments, Dallas, TX
Hyeon-Min Bae, KAIST, Daejong, Korea
Gerrit den Besten, NXP semiconductors, Eindhoven, The Netherlands
Ken Chang, Xilinx, San Jose, CA
Nicola Da Dalt, Altera, San Jose, CA
Azita Emami, California Institute of Technology, Pasadena, CA
Simone Erba, STMicroelectronics, Pavia, Italy
Ichiro Fujimori, Broadcom, Irvine, CA
Pavan Kumar Hanumolu, University of Illinois, Urbana-Champaign, Urbana, IL
Chewnpu Jou, TSMC, Hsinchu, Taiwan
Jaeha Kim, Seoul National University, Seoul, Korea
Roberto Nonis, Infineon, Villach, Austria
Hideyuki Nosaka, NTT Atsug, Japan
Frank O'Mahony, Intel, Hillsboro, OR
Hisakatsu Yamaguchi, Fujitsu Laboratories, Kawasaki, Japan

EUROPEAN REGIONAL SUBCOMMITTEE

ITPC EUROPEAN REGIONAL CHAIR
Maurits Ortmanns, University of Ulm, Ulm, Germany

ITPC EUROPEAN REGIONAL VICE CHAIR
David Stoppa, Fondazione Bruno Kessler, Trento, Italy

ITPC EUROPEAN REGIONAL SECRETARY
Marian Verhelst, KU Leuven, Heverlee, Belgium

Edith Beigné, CEA-LETI, Grenoble, France
Marco Berkhout, NXP Semiconductors, Nijmegen, The Netherlands
Gerrit den Besten, NXP Semiconductors, Eindhoven, The Netherlands
Ralf Brederlow, Texas Instruments, Freising, Germany
Martin Brox, Micron, Munchen, Germany
Pierre Busson, ST Microelectronics, Crolles, France
Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands
Jan Craninckx, IMEC, Leuven, Belgium
Nicola Da Dalt, Altera, San Jose, CA
Kostas Doris, NXP, Eindhoven, The Netherlands
Antoine Dupret, CEA LIST, Gif-sur-Yvette, France
Simone Erba, STMicroelectronics, Pavia, Italy
David Flynn, ARM, Cambridge, United Kingdom
Jan Genoe, imec, Leuven, Belgium
Pieter Harpe, Eindhoven University, Eindhoven, The Netherlands
Eric Klumperink, University of Twente, Enschede, The Netherlands
Yusuf Leblebici, Swiss Federal Institute of Technology, Lausanne, Switzerland
Stéphane Le Tual, STmicroelectronics, Crolles, France
Piero Malcovati, University of Pavia, Pavia, Italy
Andrea Mazzanti, Università di Pavia, Pavia, Italy
Gerhard Mitteregger, MediaTek Wireless, West Malling, United Kingdom
Jan Mulder, Broadcom, Bunnik, The Netherlands
Roberto Nonis, Infineon, Villach, Austria
Aarno Pärssinen, University of Oulu, Espoo, Finland
Michiel Pertijs, TU Delft, Delft, The Netherlands
Ullrich Pfeiffer, University of Wuppertal, Wuppertal, Germany
Tim Piessens, ICsense, Leuven, Belgium
Patrick Reynaert, KU Leuven, Leuven, Belgium
David Ruffieux, CSEM, Neuchated, Switzerland
Jussi Ryynanen, Aalto University, Espoo, Finland

European Members (continued):

Carlo Samori, Politecnico di Milano, Milano, Italy
Christoph Sandner, Infineon Technologies, Villach, Austria
Joseph Shor, Bar Ilan University, Ramat Gan, Israel
Jan Van Sinderen, NXP Semiconductors, Eindhoven, The Netherlands
Stefano Stanzione, IMEC-NL, Eindhoven, The Netherlands
Vojkan Vidojkovic, Intel Mobile Communications, Duisburg, Germany
Piet Wambacq, imec, Heverlee, Belgium
Refet Firat Yazicioglu, GlaxoSmithKline, Herent, Belgium

FAR EAST REGIONAL SUBCOMMITTEE

ITPC FAR EAST REGIONAL CHAIR
Tsung-Hsien Lin, National Taiwan University, Taipei, Taiwan

ITPC FAR EAST REGIONAL VICE-CHAIR
Atsuki Inoue, Fujitsu, Kawasaki, Japan

ITPC FAR EAST REGIONAL SECRETARY
Sungdae Choi, SK Hynix Semiconductor, Icheon, Korea

Hyeon-Min Bae, KAIST, Daejong, Korea
Jonathan Chang, TSMC, Hsinchu, Taiwan
Yoon-Kyung Choi, Samsung, Hwaseong, Korea
Jun Deguchi, Toshiba, Kawasaki, Japan
Guang-Kaai Dehng, Mediatek, Hsinchu, Taiwan
Minoru Fujishima, Hiroshima University, Hiroshima, Japan
Hiroshi Fuketa, AIST, Ibaraki, Japan
Yuan Gao, ASTAR, Singapore
Jin-Man Han, Samsung Electronics, Hwasung, Korea
Takashi Hashimoto, Panasonic, Fukuoka, Japan
Chun-Huat Heng, National University of Singapore, Singapore
Zhilian Hong, Fudan University, Shanghai, China
Fu-Lung Hsueh, TSMC, Hsinchu, Taiwan
Chih-Ming Hung, MediaTek, Taipei, Taiwan
Makoto Ikeda, University of Tokyo, Tokyo, Japan
Tetsuya Iizuka, University of Tokyo, Tokyo, Japan
Chewnpu Jou, TSMC, Hsinchu, Taiwan
Uksong Kang, Samsung, Hwaseong, Korea
Atsushi Kawasumi, Toshiba, Kawasaki, Japan
Chulwoo Kim, Korea University, Seoul, Korea
Jaeha Kim, Seoul National University, Seoul,Korea
TaeChan Kim, Korea University, Korea
Tae Wook Kim, Yonsei University, Seoul, Korea
Takashi Kono, Renesas, Tokyo, Japan
Tai-Cheng Lee, National Taiwan University, Taipei, Taiwan
Paul Liang, MediaTek, Hsinchu, Taiwan
Kyoo Hyun Lim, FCI, Seongnam, Korea
Mahesh Mehendale, Texas Instruments, Bangalore, India
Takahiro Miki, Renesas Electronics, Tokyo, Japan
Philip Mok, HKUST, Clear Water Bay, Hong Kong
Masato Motomura, Hokkaido University, Sapporo, Japan
Shuichi Nagai, Panasonic, Osaka, Japan
Makoto Nagata, Kobe University, Kobe, Japan
Yoshiharu Nakajima, Japan Display, Kanagawa, Japan
Byeong-Gyu Nam, Chungnam National University, Daejeon, Korea
Hideyuki Nosaka, NTT, Atsugi, Japan
Yusuke Oike, Sony, Atsugi, Japan
Kenichi Okada, Tokyo Institute of Technology, Tokyo, Japan
Kohei Onizuka, Toshiba, Kawasaki, Japan
Jaejin Park, Samsung Electronics, Hwasung, Korea
Woogeun Rhee, Tsinghua University, Beijing, China
Seung-Tak Ryu, KAIST, Daejeon, Korea
Bing Sheu, National Chiao Tung University, Hsinchu, Taiwan
Chun Shiah, Etron, Hsinchu, Taiwan
Yasuhisa Shimazaki, Renesas, Tokyo, Japan
Hyunchol Shin, Kwangwoon University, Seoul, Korea
Youngmin Shin, Samsung, Hwansung, Korea
Makoto Takamiya, University of Tokyo, Tokyo, Japan
Seng-Pan U (Ben), University of Macau, Taipa, Macau
Alice Wang, MediaTek, Hsinchu, Taiwan
Yuu Watanabe, Denso, Tokyo, Japan
Peter Chung-Yu Wu, National Chiao Tung University, Hsinchu, Taiwan
Yong Ping Xu, National University of Singapore, Singapore
Hisakatsu Yamaguchi, Fujitsu Laboratories, Kawasaki, Japan
Long Yan, Samsung Electronics, Hwaseong, Korea
Takefumi Yoshikawa, National Institute of Technology, Nagano College, Nagano, Japan

HOW TO REGISTER FOR ISSCC

Online: This is the fastest, most convenient way to register and will give you immediate email confirmation of your events. To register online (which requires a credit card), go to the ISSCC website at www.isscc.org and select the link to the registration website.

FAX, mail or email: Use the "2016 IEEE ISSCC Registration Form" which can be downloaded from the registration website. All payments must be made in U.S. Dollars, by credit card or check. Checks must be made payable to "ISSCC 2016". It will take several days before you receive email confirmation when you register using the form. **Registration forms received without full payment will not be processed until payment is received at YesEvents.** Please read the descriptions and instructions on the back of the form carefully.

On site: The On-site Registration and Advance Registration Pickup Desks at ISSCC 2016 will be located in the Yerba Buena Ballroom Foyer at the San Francisco Marriott Marquis. All participants, except as noted below, should register or pick up their registration materials at these desks as soon as possible. **Pre-registered Presenting Authors and pre-registered members of the ISSCC Program and Executive Committees must go to the Nob Hill Room, Ballroom level, to collect their conference materials.**

REGISTRATION DESK HOURS:

Saturday,	January 30	4:00 pm to 7:00 pm
Sunday,	January 31	6:30 am to 8:30 pm
Monday,	February 1	6:30 am to 3:00 pm
Tuesday,	February 2	8:00 am to 3:00 pm
Wednesday,	February 3	8:00 am to 3:00 pm
Thursday,	February 4	7:00 am to 2:00 pm

Students must present their Student ID at the Registration Desk to receive the student rates. Those registering at the IEEE Member rate must provide their IEEE Membership number.

Deadlines: The deadline for registering at the Early Registration rates is 11:59 pm Pacific Time **Monday January 4, 2016.** After January 4th, and on or before 11:59 pm Pacific Time **Monday January 11, 2016**, registrations will be processed **at the Late Registration rates. After January 11th, you must register at the on-site rates.** You are urged to register early to obtain the lowest rates and ensure your participation in all aspects of ISSCC.

Cancellations/Adjustments/Substitutions: Prior to 11:59 pm Pacific Time **Monday January 11, 2016,** conference registration can be cancelled. Fees paid will be refunded (less a processing fee of $75). Registration category or credit card used can also be changed (for a processing fee of $35). Send an email to the registration contractor at ISSCCinfo@yesevents.com to cancel or make other adjustments. **No refunds will be made after 11:59 pm Pacific Time January 11, 2016.** Paid registrants who do not attend the conference will be sent all relevant conference materials. Transfer of registration to someone else is allowed with **WRITTEN** permission from the original registrant.

IEEE MEMBERSHIP SAVES ON ISSCC REGISTRATION

Take advantage of reduced ISSCC fees by joining the Solid-State Circuits Society today, or by using your IEEE membership number. If you're an IEEE member and have forgotten your member number, simply phone IEEE at 1(800) 678-4333 and ask. IEEE membership staff will take about two minutes to look up your number for you. If you come to register on site without your membership card, you can phone IEEE then, too. Or you can request a membership number look-up by email by using the online form at: www.ieee.org/about/help/member_support.html. If you're not an IEEE member, consider joining before you register to save on your fees. Join online at www.ieee.org/join any time and you'll receive your member number by email. If you join IEEE at the conference, you can also select a free Society membership. This offer is not available to existing IEEE members.

GRAD STUDENT MENTORING SESSION

This will be a special complimentary event for grad students, early career engineers and faculty within 15 years of their first degree, where several leading experts from industry and academia, IEEE Solid-States Circuits Society Executives and Distinguished Lecturers will have a mentoring session on career coaching, entrepreneurship, publications and answer all your questions both in town hall style and 1 on 1. There will be Complimentary snacks and beverages for all participants. Student participants get 1 year complimentary SSCS membership. Event is open to all conference attendees and pre-registration is not compulsory, but RSVP to emrea@ieee.org is recommended.

SSCS MEMBERSHIP – A VALUABLE PROFESSIONAL RESOURCE FOR YOUR CAREER GROWTH

Get Connected! Stay Current! Invest in your Career! Membership in the Solid-State Circuit Society offers you the chance to explore solutions within a global community of colleagues in our field. Membership extends to you the opportunity to grow and share your knowledge, hone your expertise, expand or specialize your network of colleagues, advance your career, and give back to the profession and your local community.

SSCS MEMBERSHIP DELIVERS:

- Networking with peers -Educational development -Leadership opportunities
- Tools for career growth -Recognition for your achievements

We invite you to join or renew today to participate in exclusive educational events, access to leading research and best practice literature, and start your own career legacy by mentoring students and young professionals entering our field. It all starts with becoming a member of the Solid-State Circuit Society where you can:

-Connect with your Peers – valuable networking opportunities through our world-class conferences, publication offerings, social media extensions, and interactive educational opportunities.

-Keep up with the latest trends and cutting-edge developments in our industry – through our electronic newsletters, member magazine "Solid-State Circuits Magazine", and our award winning "Journal of Solid-State Circuits".

-Access valuable career and educational tools - saving you both time and money with 24/7 access to our website and member-only professional development and educational material; Distinguished Lecturer Tours, Tutorials, and webinars by subject matter experts.

-Access exclusive SSCS Conference Digests for ISSCC, CICC, A-SSCC, ESSCIRC, and Symposium on VLSI Circuits.

-Access publications and EBooks – discounted access to vast online document libraries of journals, standards, and conference papers offer you one-third of the world's technical research to keep your knowledge current. New publications included in your SSCS membership are the "RFIC Virtual Journal" and the "Journal on Exploratory Solid-State Computational Devices and Circuits", a new open access publication.

SSCS MEMBERSHIP SAVES EVEN MORE ON ISSCC REGISTRATION

This year, SSCS members will again receive an exclusive benefit of a $40 discount on the registration fee for ISSCC in addition to the IEEE discount. Also, the SSCS will again reward our members with a $10 Starbucks gift card when they attend the Conference as an SSCS member in good standing.

Join or renew your membership with IEEE's Solid-State Circuit Society today at sscs.ieee.org – you will not want to miss out on the opportunities and benefits your membership will provide now and throughout your career.

ITEMS INCLUDED IN REGISTRATION

Technical Sessions: Registration includes admission to all technical and evening sessions starting Sunday evening and continuing throughout Monday, Tuesday and Wednesday. ISSCC does not offer partial conference registrations.

Technical Book Display: Several technical publishers will have collections of professional books and textbooks for sale during the Conference. The Book Display will be open on Monday from Noon to 7:00 pm; on Tuesday from 10:00 am to 7:00 pm; and on Wednesday from 10:00 am to 3:00 pm.

Demonstration Sessions: Hardware demonstrations will support selected papers.

Author Interviews: Author Interviews will be held Monday, Tuesday and Wednesday evenings. Authors from each day's papers will be available to discuss their work.

Social Hour: Social Hour refreshments will be available starting at 5:15 pm.

University Events: Several universities are planning social events during the Conference. Check the University Events display at the conference for the list of universities, locations and times of these events.

ISSCC Duffel Bag: A convenient duffel bag for travel or sports will be given to all Conference registrants.

Publications: Conference registration includes:

-The **Digest of Technical Papers** in hard copy and by download. The Digest book will be distributed during registration hours beginning on Sunday at 10:00 am.

-**Papers Visuals:** The visuals from all papers presented will be available by download.

-**Demonstration Session Guidebook:** A descriptive guide to the Demonstration Session will be available by download.

-**Note:** Instructions will be provided for access to all downloads. Downloads will be available both during the Conference and for a limited time afterwards.

OPTIONAL EVENTS

Educational Events: Many educational events are available at ISSCC for an additional fee. There are ten 90-minute Tutorials and two all-day Forums on Sunday. There are four additional all-day Forums on Thursday as well as an all-day Short Course. All events include a course handout in color. The Forums and Short Course also include breakfast, lunch and break refreshments. See the schedule for details of the topics and times.

Women's Networking Event: ISSCC will be offering a networking event for women in solid-state circuits on **Monday at 12:15 pm**. This luncheon is an opportunity to hear from an accomplished speaker, get to know other women in the profession and discuss a range of topics including leadership, work-life balance, and professional development. This event is open to women only at a discounted fee.

OPTIONAL PUBLICATIONS

ISSCC 2016 Publications: The following ISSCC 2016 publications can be purchased in advance or on site:

2016 ISSCC Download USB: All of the downloads included in conference registration **(mailed in March).**

2016 Tutorials DVD: All of the 90 minute Tutorials **(mailed in May).**

2016 Short Course DVD: "Circuits for the Internet of Everything" **(mailed in May)**.

Short Course and Tutorial DVDs contain audio and written English transcripts synchronized with the presentation visuals. In addition, the Short Course DVD contains a pdf file of the presentations suitable for printing, and pdf files of key reference material.

Earlier ISSCC Publications: Selected publications from earlier conferences can be purchased. There are several ways to purchase this material:

-Items listed on the registration form can be purchased with registration and picked up at the conference.

-Visit the ISSCC Publications Desk. This desk is located in the registration area and has the same hours as conference registration. With payment by cash, check or credit card, you can purchase materials at this desk. See the order form at the Conference for titles and prices.

-Visit the ISSCC website at www.isscc.org and click on the link "SHOP ISSCC" where you can order online or download an order form to mail, email or fax. For a small shipping fee, this material will be sent to you immediately and you will not have to wait until you attend the Conference to get it.

HOW TO MAKE HOTEL RESERVATIONS

Due to special events in San Francisco, there will be great demand for all hotel rooms. Make your hotel reservation early, no matter which hotel you choose.

Online: ISSCC participants are urged to make their hotel reservations at the San Francisco Marriott Marquis online. Go to the conference website and click on the Hotel Reservation link. **Conference room rates are $269 for a single/double, $289 for a triple and $309 for a quad** (per night plus tax). In addition, ISSCC attendees booked in the ISSCC group receive **in-room Internet access for free**. All online reservations require the use of a credit card. Online reservations are confirmed immediately. You should print the page containing your confirmation number and reservation details and bring it with you when you travel to ISSCC.

Telephone: Call 877-622-3056 (US) or 415-896-1600 and ask for "Reservations." When making your reservation, identify the group as ISSCC 2016 to get the group rate.

Hotel Deadline: Reservations must be received at the San Francisco Marriott Marquis no later than 5 pm Pacific Time January 8, 2016 to obtain the special ISSCC rates. A limited number of rooms are available at these rates. **Once this limit is reached or after January 8th, the group rates may no longer be available and reservations will be filled at the best available rate.** Changes: Before the hotel deadline, your reservation can be changed by calling the telephone numbers above. After the hotel deadline, call the Marriott Marquis at 415-896-1600 (ask for "Reservations"). Have your hotel confirmation number ready.

IEEE NON-DISCRIMINATION POLICY

IEEE is committed to the principle that all persons shall have equal access to programs, facilities, services, and employment without regard to personal characteristics not related to ability, performance, or qualifications as determined by IEEE policy and/or applicable laws.

EVENT PHOTOGRAPHY

Attendance at, or participation in, this conference constitutes consent to the use and distribution by IEEE of the attendee's image or voice for informational, publicity, promotional and/or reporting purposes in print or electronic communications media. Video recording by participants and other attendees during any portion of the conference is not allowed without special prior written permission of IEEE.

REFERENCE INFORMATION

TAKING PICTURES, VIDEOS OR AUDIO RECORDINGS DURING ANY OF THE SESSIONS IS NOT PERMITTED

Conference Website:	www.isscc.org
ISSCC Email:	ISSCC@ieee.org
Registration questions:	ISSCCinfo@yesevents.com
Hotel Information:	San Francisco Marriott Marquis Phone: 415-896-1600 55 Fourth Street San Francisco, CA 94103
Press Information:	Kenneth C. Smith Phone: 416-418-3034 University of Toronto Email: lcfujino@aol.com
Registration:	YesEvents Phone: 410-559-2200 or 800-937-8728 Fax: 410-559-2217 1700 Reisterstown Road #236 Baltimore, MD 21208 Email: issccinfo@yesevents.com

Hotel Transportation: Visit the ISSCC website "Attendees" page for helpful travel links and to download a document with directions and pictures of how to get from the San Francisco Airport (SFO) to the Marriott Marquis. You can get a map and driving directions from the hotel website at www.marriott.com/hotels/travel/sfodt-san-francisco-marriott-marquis/

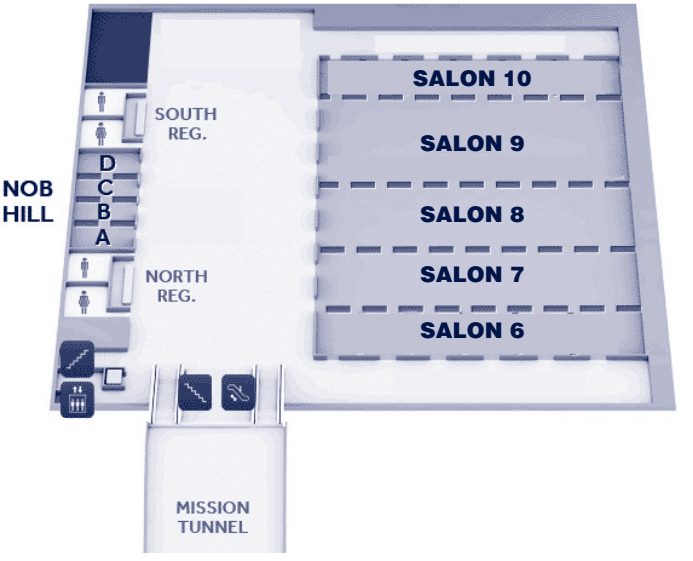
Next ISSCC Dates and Location: ISSCC 2017 will be held on February 5-9, 2017 at the San Francisco Marriott Marquis Hotel.

Subcommittee Chairs

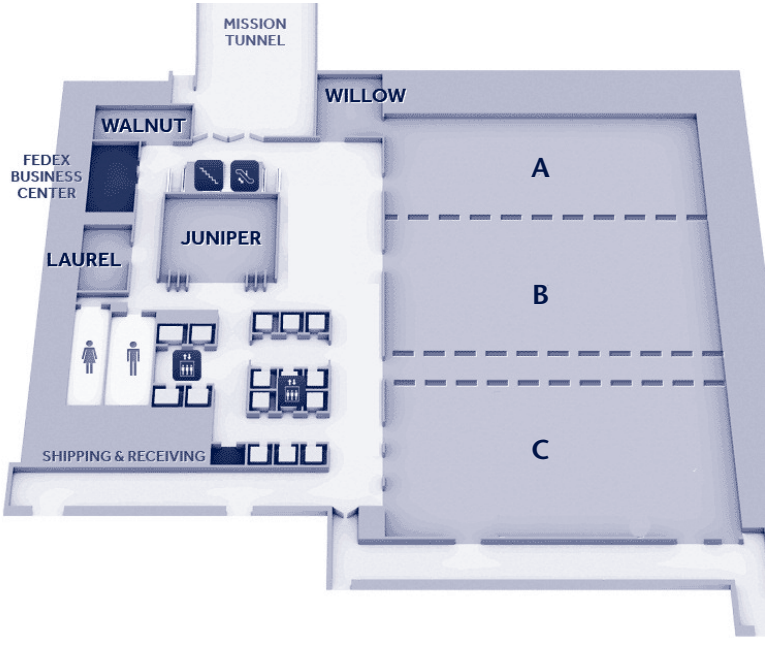
Analog:	Axel Thomsen
Data Converters:	Un-Ku Moon
Digital Architectures & Systems:	Stephen Kosonocky
Digital Circuits:	Stefan Rusu
Imagers, MEMS, Medical & Displays:	Makoto Ikeda
Memory:	Leland Chang
RF:	Piet Wambacq
Technology Directions:	Eugenio Cantatore
Wireless:	Aarno Pärssinen
Wireline:	Daniel Friedman

Program-Committee Chair: Kevin Zhang
Program-Committee Vice-Chair: Boris Murmann
Conference Chair: Anantha Chandrakasan

Lower B2 Level - Yerba Buena Ballroom



B2 Level - Golden Gate Hall



IEEE

445 Hoes Lane
P.O. Box 1331
Piscataway, NJ 08855-1331
USA

ISSCC.org

sscs.ieee.org

ISSCC 2016 ADVANCE PROGRAM