

ADVANCE PROGRAM



2018 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

FEBRUARY
11, 12, 13, 14, 15

CONFERENCE THEME:

SILICON ENGINEERING A SOCIAL WORLD

SAN FRANCISCO
MARRIOTT MARQUIS HOTEL

NEW THIS YEAR!
INDUSTRY SHOWCASE;
Impact of ICs on Product Design

THURSDAY ALL-DAY

4 FORUMS: CIRCUITS/ARCHITECTURES FOR WIRELESS SENSING/RADAR/IMAGING; TECHNIQUES FOR mm-WAVE MULTI-ANTENNA SYSTEMS; ADVANCED OPTICAL COMMUNICATIONS; ENERGY-EFFICIENT ANALOG

SHORT-COURSE: HARDWARE FOR MACHINE LEARNING INFERENCE

SUNDAY ALL-DAY

2 FORUMS: INTELLIGENT ENERGY SYSTEMS FOR IoT; FINFETs & FDSOI IN MIXED-SIGNAL DESIGN

10 TUTORIALS: LOW-JITTER PLLs FOR WIRELESS; NV FOR MEMORY, LOGIC, & AI; BASICS OF QUANTUM COMPUTING; ECC 5G/NVM; HYBRID DESIGN OF ADCs; CMOS SINGLE-PHOTON DETECTION; ADAPTIVE & RESILIENT CIRCUITS; SWITCHED-MODE POWER-CONVERTER DESIGN; DIGITAL-RF TRANSMITTERS; ADC-BASED SERIAL LINKS

2 EVENING EVENTS: GRADUATE STUDENT RESEARCH IN PROGRESS; WORKSHOP ON CIRCUITS FOR SOCIAL GOOD

**5-DAY
PROGRAM**

ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and application to maintain technical currency, and to network with leading experts.

CONFERENCE TECHNICAL HIGHLIGHTS

On Sunday, February 11th, the day before the official opening of the Conference, ISSCC 2018 offers:

- A choice of up to 4 of a total of 10 Tutorials, or
- A choice of 1 of 2 all-day Advanced-Circuit-Design Forums

The 90-minute tutorials offer background information and a review of the basics in specific circuit- and system-design topics. In the all-day Advanced-Circuit-Design Forums, leading experts present state-of-the-art design strategies in a workshop-like format. The Forums are targeted at designers experienced in the technical field.

On Sunday evening, there are two events: A Workshop on “Circuits for Social Good” will be offered starting at 6:00 pm. In addition, the Student-Research Preview, featuring one-minute introductory presentations followed by a poster session from selected graduate-student researchers from around the world will begin at 7:30 pm. Introductory remarks at the Preview will be provided by a distinguished member of the solid-state circuit community, Professor Tom Lee, Stanford University.

On Monday, February 12th, ISSCC 2018 at 8:30 am offers four plenary papers on the theme: “Silicon Engineering A Social World”. On Monday at 1:30 pm, there begin five parallel technical sessions, followed by a Social Hour at 5:15 pm open to all ISSCC attendees. The Social Hour, held in conjunction with Book Displays and Author Interviews, will also include a Demonstration Session, featuring posters and live demonstrations of selected papers from industry and academia. On Monday evening at 8:00 pm there are 2 events entitled “Industry Showcase” and “Figures-of-Merit on Trial”.

On Tuesday, February 13th, there are five parallel technical sessions, both morning and afternoon. A Social Hour open to all ISSCC attendees will follow. The Social Hour, held in conjunction with Book Displays and Author Interviews, will also include a second Demonstration Session. Tuesday evening includes two events, entitled “Lessons Learned — Great Circuits that Didn’t Work (Oops, If Only I Had Know)” and “Can Artificial Intelligence Replace my Job — The Dawn of a New IC Industry with AI”.

On Wednesday, February 14th, there will be five parallel technical sessions, both morning and afternoon, followed by Author Interviews.

On Thursday, February 15th, ISSCC offers a choice of five all-day events:

- A Short Course entitled: “Hardware for Machine Learning Inference”
- Four Advanced-Circuit-Design Forums entitled:
 - “Circuits and Architectures for Wireless Sensing, Radar, and Imaging”
 - “Circuit and System Techniques for mm-Wave Multi-Antenna Systems”
 - “Advanced Optical Communication:
From Devices, Circuits, and Architectures, to Algorithms”
 - “Advances in Energy-Efficient Analog Design”

For the first time, this year, there is an option which allows an attendee to sample parts of all 5 Thursday offerings. Registration for educational events on Sunday and Thursday will be filled on a first-come first-served basis. Use of the ISSCC Web-Registration Site (<http://www.isscc.org>) is strongly encouraged. Registrants will be provided with immediate confirmation on registration for the Conference, Tutorials, Forums, and the Short Course.

Need Additional Information? Go to: www.isscc.org

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There are a total of 10 tutorials this year on 10 different topics. Each tutorial, selected through a competitive process within each subcommittee of the ISSCC, presents the basic concepts and working principles of a single topic. These tutorials are intended for non-experts, graduate students and practicing engineers who wish to explore and understand a new topic.

Ali Sheikholeslami
ISSCC Education Chair

8:30 AM

T1 Low-Jitter PLLs for Wireless Transceivers

Xiang Gao, Credo Semiconductor, Fremont, CA

PLLs and frequency synthesizers are key building blocks in wireless transceivers. With the trend of higher data-rate, higher carrier frequency and higher order of modulation, the jitter or phase noise requirement becomes more demanding given a limited power budget. This tutorial starts from the fundamentals of PLL jitter and power consumption. Various sources of PLL jitter and power will be identified and analyzed, and design methodologies to optimize them on both the block and system level will be presented. Finally, the working principle and recent advances of the low jitter sub-sampling PLL architecture will be discussed.

Xiang Gao received the B.E. degree from the Zhejiang University, Hangzhou, China, in 2004 and the M.Sc. (cum laude) and Ph.D. (cum laude) degrees from the University of Twente, Enschede, The Netherlands, in 2006 and 2010 respectively, both in electrical engineering. From 2010 to 2016, he was a principal engineer and design manager with Marvell Semiconductor, Santa Clara, CA, focusing on wireless transceiver circuits. He is now an Engineering Director with Credo Semiconductor, Milpitas, CA, working on high-speed SerDes. He has published 20 papers and holds 8 patents. He is an IEEE senior member.

8:30 AM

T2 Nonvolatile Circuits for Memory, Logic, and Artificial Intelligence

Meng-Fan Chang, National Tsing-Hua University, Hsinchu, Taiwan

Memory has proven a major bottleneck in the development of energy-efficient chips for IoT applications and artificial intelligence (AI). Recent nonvolatile memory (NVM) devices not only serve as nonvolatile memory macros, but also enable the development of nonvolatile logics (nvLogics) for nonvolatile processors as well as computing-in-memory (CIM) for AI chips. In this tutorial, we begin with an introduction to various NVM technologies (i.e. MRAM, PCM, ReRAM) and the fundamental circuits used in NVM macros. We then review various state-of-the-art circuit techniques for low-power, high-speed on-chip NVM macros. In the third part of the tutorial, we examine some of the challenges involved in the further development of these technologies and review examples of NVM enabled nvLogics (i.e. nvFlipflop, nvSRAM, nvTCAM) for nonvolatile processors and CIMs for AI chips.

Professor Chang received his M.S. from Pennsylvania State University and his Ph.D. degree from National Chiao Tung University in Taiwan. He is currently a full Professor at National Tsing Hua University, Taiwan. Before 2006, he has worked in industry over 10 years.

Between 1997 and 2006, Dr. Chang worked in the design of circuits for SRAM/Flash compilers at Mentor Graphics (New Jersey, US), TSMC (Taiwan), and IPLib (Taiwan). His research interests include circuit design for volatile and nonvolatile memory, in-memory-computing, artificial intelligence chips, and neuromorphic computing.

Since 2010, Professor Chang has co-authored 35+ top-tier conference papers (14 ISSCC, 14 VLSI, 8 IEDM, and 4 DAC), 30+ IEEE journal papers, and 40+ granted US patents. He is an associate editor for IEEE TVLSI, IEEE TCAD, and IEICE Electronics, and has been serving on the TPC for ISSCC, IEDM (Chair of Memory Technology for 2017), A-SSCC, IEEE CAS Society (Chair Elect of NG-TC), and numerous conferences. He has also been serving as the Associate Executive Director for Taiwan's National Program of Intelligent Electronics (NPIE) since 2011.

8:30 AM

T3 **Basics of Quantum Computing***Edoardo Charbon, EPFL, Neuchatel, Switzerland*

The tutorial introduces quantum computing to a general audience. It begins with the concept of qubit and its representation, followed by 1-qubit quantum gates and qubit measurement. It will then move on to 2-qubit states, entanglement, and 2-qubit gates. Switching gears, the tutorial will discuss quantum Fourier transforms, unitary transforms, and quantum arithmetic. Finally, we will go through a simple quantum algorithm and discuss solid-state implementations of networks of qubits, highlighting the challenges for reading and controlling them. We conclude with future perspectives.

Edoardo Charbon received the Diploma from ETH Zurich in 1988, the M.S. degree from UC San Diego in 1991, and the Ph.D. degree from UC Berkeley in 1995 all in electrical engineering and EECS. He was with Cadence Design Systems from 1995 to 2000. In 2000, he joined Canesta, Inc., as its Chief Architect. Since 2002, he has been a faculty member at EPFL and, from 2008-2016, at TU Delft.

He has authored over 250 papers and two books; he holds 20 patents. His current research interests include 3D imaging, advanced biomedical imaging, quantum integrated circuits, and cryo-CMOS for quantum computing and sensing. Dr. Charbon is a Distinguished Visiting Scholar with the W. M. Keck Institute for Space, California Institute of Technology, a Fellow of the Kavli Institute of Nanoscience Delft, a Distinguished Lecturer of the IEEE Photonics Society, and a Fellow of the IEEE.

10:30 AM

T4 **Error-Correcting Codes in 5G/NVM Applications***Hsie-Chia Chang, National Chiao Tung University, HsinChu, Taiwan*

The growing needs of efficient data transmission and storage are driving information delivery technologies to new frontiers. Either in the new radio (NR) links of 5G communications, or in emerging non-volatile memories (NVMs) with continuously increasing capacity, error correcting codes (ECCs) are essential and crucial in maintaining the data correctness. In this tutorial, we will cover major concepts in ECC design and architecture, including multi-Gb/s LDPC-BC, energy-efficient LDPC-CC, and Polar/Turbo decoders that fulfill different requirements in various 5G scenarios. For NVM applications, we will introduce 1-error and 2-error correcting scheme with parallel architectures for NOR flash, as well as BCH and LDPC coding schemes for NAND/3D-NAND, to address low-latency and high-throughput solutions.

Hsie-Chia Chang received the B.S., M.S., and Ph.D. degrees from National Chiao Tung University, Hsinchu, Taiwan, in 1995, 1997, and 2002, respectively, all in electronics engineering.

He was with OSP/DE1, MediaTek Corporation, from 2002 to 2003, where he was involved in decoding architectures for combo single chip. In 2003, he joined the faculty of the Electronics Engineering Department, National Chiao-Tung University, where he has been a Professor since 2010. His research interests include algorithms and VLSI architectures in signal processing, in particular, error control codes and crypto-systems. He has published more than 100 IEEE journal/conference papers, and more than 50 U.S./Taiwan patents. Recently, he has focussed on designing high code-rate ECC schemes for flash memory, PUF implementation for secure MCU system, and multi-Gb/s chip implementations for wireless communications.

Dr. Chang served as the Deputy Director General with the Chip Implementation Center, Taiwan, since 2017. He has also served as an Associate Editor of the IEEE Transactions on Circuits and Systems I: Regular Papers since 2012, as well as served as a Technical Program Committee Member of the IEEE Asian Solid-State Circuits Conference from 2011 to 2013, and the International Solid-State Circuits Conference in 2018. He was a recipient of the Outstanding Youth Electrical Engineer Award from the Chinese Institute of Electrical Engineering in 2010, and the Outstanding Youth Researcher Award from the Taiwan IC Design Society in 2011.

10:30 AM

T5 Hybrid Design of Analog-to-Digital Converters*Seng-Pan (Ben) U, University of Macau, Macau, Macau*

Traditionally, ADC architectures have been sorted into distinct categories such as FLASH, SAR, pipeline, and delta-sigma. Recently, improvements in ADC power, speed, and resolution have been enabled by hybrid approaches that combine techniques from many ADC architectures. Further, this trend of hybrid design is extended beyond the choice of quantizer to include a mix of circuit topologies in key ADC building blocks. The resulting degrees of freedom allow designers to fully optimize their converters, leading to performance levels beyond what can be achieved with conventional architectures. This tutorial will start with a general overview of key ADC architectures (e.g. Flash, SAR, pipeline and delta-sigma), highlighting basic operation and design trade-offs. Second, the architectural hybrid designs in consideration of various quantizer options will be discussed. Last, illustrative examples of hybrid circuit topologies and techniques will be discussed, with emphasis on design choices that enabled performance benefits for the specific application of interest.

Seng-Pan (Ben) U received the dual Ph.D. degree from University of Macau (UM) and Instituto Superior Técnico, Portugal in 2002. He is currently Professor and Deputy Director of State-Key Laboratory of Analog & Mixed-Signal (AMS) VLSI of UM. He is also the co-founder & corporate R&D director and Macau site general manager of Synopsys Macau Ltd (Former Chipidea Microelectronics Macau).

He co-authored 200+ publications, 4 books and co-held 14 US patents. He was A-SSCC 2013 tutorial speaker for energy efficient data converters and SSCS Distinguished Lecturer (2014-2015). He is co-recipient of the 2014 ESSCIRC Best paper award, and also the advisor for student awards of SSCS Pre-doc Achievement Award, ISSCC Silk-Road Award, A-SSCC Student Design Contest in data converter field. He was the 1st recipient from Macau of the National science & technology (S&T) award and Ho Leung Ho Lee Foundation award. He received 7 Macau S&T Awards, 2 business awards, and government Honorary Title of Value.

He is currently IEEE Fellow and was also elected as the Scientific Chinese of the Year 2012 and recently appointed as a member of the Science and Technology Commission of China Ministry of Education. He is TPC of ISSCC, data converter sub-committee chair of A-SSCC, analog sub-committee chair of VLSI-DAT and editorial board member of Journal AICSP.

10:30 AM

T6 Single-Photon Detection in CMOS*Matteo Perenzoni, Fondazione Bruno Kessler, Trento, Italy*

Every single photon carries information in position, time, etc. Single-photon devices are now demonstrated and available in several CMOS technologies, but the needed circuits and architectures are completely different from conventional visible light sensors.

This tutorial starts from the description of structure and operation of a single-photon detector, and it continues on the definition of circuits for the front-end electronics needed to efficiently manage the extracted information, addressing challenges and requirements. Then, it concludes with an overview of the different architectures that are specific for each application field, with examples in the biomedical, consumer, and space domain.

Matteo Perenzoni received the Laurea degree in Electronics Engineering from the University of Padova, Italy, in 2002. In January 2004, he joined Fondazione Bruno Kessler (FBK), Trento, Italy, as a research scientist, where he now leads the Integrated Radiation and Image Sensors (IRIS) research unit. He has been collaborating as contract professor with the University of Trento, and visiting researcher at TU Delft. His research interests include the design of advanced image sensors from single-photon to multispectral sensing.

1:30 PM

T7 Basics of Adaptive and Resilient Circuits*Keith A. Bowman, Qualcomm, Raleigh, NC*

Dynamic device and circuit parameter variations degrade processor performance, energy efficiency, yield, and reliability across all market segments, ranging from small embedded cores in an IoT to large multicore servers. This tutorial introduces the primary variations during a processor's operational lifetime, including transient voltage droops, temperature changes, and radiation-induced soft errors, as well as persistent transistor and interconnect aging. This presentation then describes the negative impact of these variations on timing and data retention in logic and embedded memory across a wide range of voltages and clock frequencies. To mitigate these adverse effects from dynamic variations, this tutorial presents adaptive and resilient circuits, while highlighting the key design trade-offs and testing implications for product deployment.

Keith Bowman is a Principal Engineer and Manager in the Processor Research Team at Qualcomm Technologies, Inc. in Raleigh, NC. He pioneered the invention, design, and test of Qualcomm's first commercially successful circuit for mitigating the adverse effects of supply voltage droops. He received the Ph.D. degree from the Georgia Institute of Technology and worked at Intel for 12 years. He has published over 70 technical conference and journal papers and presented over 30 tutorials on variation-tolerant circuit designs. He currently serves on the ISSCC technical program committee.

1:30 PM

T8 Fundamentals of Switched-Mode Power-Converter Design*Hoi Lee, The University of Texas at Dallas, Richardson, TX*

Switched-mode power converters are very popular in power management IC designs for voltage conversions and are widely adopted for today's smart phones and tablets thanks to their high power-conversion efficiency and high-output-power capability. Their applications also include high-voltage and high-power automotive systems, LED lighting, and renewable energy systems. In this tutorial, switched-mode power-converter fundamentals and the design of CMOS switched-mode power converters will be covered. Topics include an overview of non-isolated power-converter topologies such as buck, boost, and non-inverting buck-boost; loss analysis and comparisons between continuous and discontinuous conduction-mode operations; different control schemes; and frequency compensation between voltage-mode and current-mode operations. Topics also include detailed circuit implementations of building blocks like FET-based and filter-based current sensors, dead-time control and gate drivers and the state-of-the-art designs. Practical design examples are used throughout the presentation. Advanced topic includes the discussions of three-level converters.

Hoi Lee received the B.Eng., M.Phil., and Ph.D. degrees in Electrical and Electronic Engineering from the Hong Kong University of Science and Technology. Since 2005, he has been with the Department of Electrical and Computer Engineering, the University of Texas at Dallas, Richardson, TX, where he is a Professor. His research interests include power-management integrated circuits, power-converter topologies and control methodologies, wireless power and energy-harvesting circuits, and analog and mixed-signal integrated circuits.

Dr. Lee serves as an Associate Editor of IEEE Transactions on Circuits and Systems-I Regular Papers. He is also on the Technical Program Committees of ISSCC, CICC, and ISPSD. He has authored or coauthored over 100 peer-reviewed conference and journal papers. He received 2011 NSF CAREER Award and was the recipient of the CICC 2002 Best Student Paper Award.

3:30 PM

T9 Digital RF Transmitters*Renaldi Winoto, Tectus, Saratoga, CA*

Direct digital-to-RF conversion at the antenna interface offers many exciting opportunities to push the performance envelope of RF transmitters in efficiency, area, signal bandwidth, and modulation quality. This tutorial will provide a complete overview of digital transmitter architectures, starting from digital bits at the symbol rate all the way to the antenna. We will start at the heart of this architecture, with a review of state-of-the-art, high-efficiency, digital PA topologies. Then we will discuss all auxiliary circuits and digital signal-processing tricks needed around the PA core to enable the transmitter to meet strict signal fidelity and spectrum cleanliness requirement while to simultaneously provide the PA core with the optimal environment for highest efficiency. Topics for discussion include: digital sample-rate conversion, 1-D and 2-D digital pre-distortion for wideband signals, and peculiarities of signal processing in the polar domain.

Renaldi Winoto received his Bachelors degree from Cornell University in 2003 and his Ph.D. degree from University of California, Berkeley in 2009. He was with Marvell Semiconductors from 2009 to 2017 where he worked as an Engineering Director and led a group responsible for definitions of RF transceiver architectures and designs of RF power amplifiers for Wireless LAN. In 2017, he joined Tectus Corporation, a stealth-mode start-up. He is a member of the technical program committee for RFIC and ISSCC. His research interest is in mixed-signal and radio-frequency circuits for wireless communication systems.

3:30 PM

T10 ADC-Based Serial Links: Design and Analysis*Sam Palermo, Texas A&M University, College Station, TX*

Growing serial I/O data rates, over both severe low-pass electrical and dispersive optical channels, necessitate increased equalization complexity and consideration of more bandwidth-efficient modulation schemes, such as four-level pulse-amplitude modulation (PAM4). Serial links which utilize ADC-based receiver front-ends offer a potential solution, as they enable more powerful and flexible DSP for equalization and symbol detection and can easily support advanced modulation schemes. This tutorial will provide an overview of key concepts in ADC-based serial links that support operation over high-loss channels. Topics covered include high-speed ADC topologies, digital equalizers, benefits of partial analog equalization, modeling approaches, and calibration techniques.

Samuel Palermo received the B.S. and M.S. degrees in electrical engineering from Texas A&M University, College Station, TX in 1997 and 1999, respectively, and the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA in 2007.

From 1999 to 2000, he was with Texas Instruments, Dallas, TX, where he worked on the design of mixed-signal integrated circuits for high-speed serial data communication. From 2006 to 2008, he was with Intel Corporation, Hillsboro, OR, where he worked on high-speed optical and electrical I/O architectures. In 2009, he joined the Electrical and Computer Engineering Department of Texas A&M University where he is currently an associate professor. His research interests include high-speed electrical and optical interconnect architectures, RF photonics, high performance clocking circuits, and integrated sensor systems.

Dr. Palermo is a recipient of a 2013 NSF-CAREER award. He is a member of Eta Kappa Nu and IEEE. He has served as an associate editor for IEEE Transactions on Circuits and System – II from 2011 to 2015 and has served on the IEEE CASS Board of Governors from 2011 to 2012. He is currently a distinguished lecturer for the IEEE Solid-State Circuits Society. He was a coauthor of the Jack Raper Award for Outstanding Technology-Directions Paper at the 2009 International Solid-State Circuits Conference, the Best Student Paper at the 2014 Midwest Symposium on Circuits and Systems, and the Best Student Paper at the 2016 Dallas Circuits and Systems Conference. He received the Texas A&M University Department of Electrical and Computer Engineering Outstanding Professor Award in 2014 and the Engineering Faculty Fellow Award in 2015.

F1: Intelligent Energy-Efficient Systems at the Edge of IoT

Organizer: Vivek De, Intel, Hillsboro, Oregon

Committee: Dennis Sylvester, University of Michigan, Ann Arbor, MI
 James Myers, ARM, Cambridgeshire, United Kingdom
 Jun Deguchi, Toshiba Memory Corporation, Kawasaki, Japan
 Shinichiro Shiratake, Toshiba Technology Development, Yokohama, Japan
 Ingrid Verbauwhede, KU Leuven, Leuven, Belgium

Energy efficiency as well as security of ubiquitous smart, secure and connected devices at the edge nodes of IoT are critical for realizing robust and intelligent end-to-end cyberphysical systems that deliver compelling new experiences and capabilities based on deep learning and other natural computing technologies for big data applications. This forum brings together low-power SoC as well as sensor, data converter, memory & wireless circuits designers, and machine learning & security hardware experts, to discuss the challenges and recent advances in the development of these edge node devices. All of the key hardware technologies – extremely energy-efficient smart sensors/imagers and analog-to-digital/information converters, high-density memory/storage, ultra-low-power wireless connectivity, intelligent compute and learning engines, and hardware security features – are presented. These technologies must be incorporated optimally across the distributed end-to-end cyberphysical systems spanning the front-end physical interfaces, the distributed network components and the back-end cloud infrastructure, to achieve sustainable cognition, intelligent decision and action capabilities for a range of autonomous IoT applications.

Forum Agenda

<u>Time:</u>	<u>Topic:</u>
8:00 AM	Breakfast
8:20 AM	Introduction by Chair
8:30 AM	Smart and Energy-Efficient Integrated Sensors <i>Bruno W. Garlepp, TDK, San Jose, CA</i>
9:20 AM	Low Power Analog Front Ends & Data Converters <i>Gabriele Manganaro, Analog Devices, Wilmington, MA</i>
10:10 AM	Break
10:35 AM	Intelligent Energy-efficient Memory/Storage Systems <i>Shinobu Fujita, Toshiba, Kawasaki, Japan</i>
11:25 AM	Ultra-Low Power Wireless Connectivity <i>Carolynn Bernier, CEA-LETI-MINATEC, Grenoble, France</i>
12:15 PM	Lunch
1:20 PM	Compressive Imaging for CMOS Image Sensors <i>Yusuke Oike, Sony Semiconductor Solutions, Atsugi, Japan</i>
2:10 PM	Ultra-Low Power SoCs for Local Sensor Data Processing <i>David Bol, Université Catholique de Louvain, Louvain-la-Neuve, Belgium</i>
3:00 PM	Break
3:20 PM	Natural Computing with Ising Model for Combinatorial Optimization <i>Masanao Yamaoka, Hitachi, Tokyo, Japan</i>
4:10 PM	Hardware Security at the Edge of IoT <i>Sanu Mathew, Intel, Hillsboro, OR</i>
5:00 PM	Closing remarks by Chair

F2: FinFETs & FDSOI – A Mixed Signal Circuit Designer’s Perspective

Organizers: Venkatesh Srinivasan, *Texas Instruments, Dallas, TX*
 Stéphane Le Tual, *STMicroelectronics, Crolles, France*
 Tai-Cheng Lee, *National Taiwan University, Taipei, Taiwan*

Committee: John Long, *University of Waterloo, Waterloo, Canada*
 Xin He, *NXP, Eindhoven, The Netherlands*
 Jaeha Kim, *Seoul National University, Seoul, Korea*

Moderator: David Robertson, *Analog Devices, Wilmington, MA*

With circuit design in the nanometer regime, designers have a choice between transistors in FinFETs or FDSOI technology. This Forum brings together experts from industry and academia to discuss the opportunities these technologies present for designers. The experts will present the physics/modeling of FinFETs & FDSOI transistors followed by an in-depth analysis of design considerations for modules spanning analog/mixed-signal to mm-Wave regimes. The Forum will conclude with a panel discussion with the speakers.

Forum Agenda

Time:	Topic:
8:00 AM	Breakfast and Forum Opening
8:30 AM	FinFET Basics: Reconsideration of the Capabilities from Fundamental Device Concepts <i>Digh Hisamoto, Hitachi, Kokubunji, Tokyo, Japan</i>
9:15 AM	RF & mm-Wave Design in FinFET Technology <i>Steven Callender, Intel, Hillsboro, OR</i>
10:00 AM	Break
10:15 AM	FDSOI Basics – Physics, Device Performance and RF & mm-Wave Design Enablement <i>Patrick Scheer, STMicroelectronics, Crolles, France</i>
11:00 AM	Millimeter-Wave FDSOI Power Amplifiers for 5G Mobile Communications <i>Eric Kerherve, University of Bordeaux, Talence, France</i>
11:45 AM	Lunch
1:00 PM	FinFETs for Analog & Mixed-Signal Designs <i>Lawrence Loh, MediaTek, San Jose, CA</i>
1:45 PM	High Speed Transceivers Using FinFETs <i>Ken Chang, Xilinx, San Jose, CA</i>
2:30 PM	Break
2:45 PM	The Fourth Terminal in FDSOI <i>Borivoje Nikolic, University of California at Berkeley, Berkeley, CA</i>
3:30 PM	RF, mm-Wave and Fiber-Optics Design in FDSOI CMOS Technologies <i>Sorin P. Voinigescu, University of Toronto, Toronto, Canada</i>
4:15 PM	Panel Discussion Moderator: David Robertson, Analog Devices, Wilmington, MA

EE1: Student Research Preview (SRP)

The Student Research Preview (SRP) will highlight selected student research projects in progress. The SRP consists of 25 one-minute presentations followed by a Poster Session, by graduate students from around the world, which have been selected on the basis of a short submission concerning their on-going research. Selection is based on the technical quality and innovation of the work. This year, the SRP will be presented in three theme sections: Communications and Power; Deep Learning and Biomedical Circuits; Memory, Sensors, and Mixed-Signal Circuits.

The Student Research Preview will include a brief talk by a distinguished member of the solid-state circuits community, Professor Tom Lee, Stanford University. SRP begins at 7:30 pm on Sunday, February 11th. SRP is open to all ISSCC registrants.

Chair	SeongHwan Cho	KAIST
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Advisor	Jan Van der Spiegel	University of Pennsylvania
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Chun-Huat Heng	National University of Singapore, Singapore
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Qiang Li	University of Electronic Science & Tech., China
Shih-Chii Liu	University of Zurich /ETH Zurich, Switzerland
Shahriar Mirabbasi	University of British Columbia, Canada
Tinoosh Mohsenin	University of Maryland, MD
Cormac O'Connell	TSMC, Canada
Mondira Pant	Intel, MA
Shanthi Pavan	Indian Institute of Technology, India
Jae-sun Seo	Arizona State University, AZ
Mingoo Seok	Columbia University, NY
Farhana Sheikh	Intel, OR
Bing Sheu	Chang Gung University, Taiwan
GuoXing Wang	Shanghai Jiao Tong University, China
Jeffrey Weldon	University of Hawaii, HI
Chung-Yu Wu	National Chiao Tung University, Taiwan
Jerald Yoo	National University of Singapore, Singapore
Samira Zaliasl	IMEC, Belgium

EE2: Workshop on Circuits for Social Good**Chair:** Vivienne Sze, Massachusetts Institute of Technology, Cambridge, MA**Organizers:**

Alison Burdett, Sensium Healthcare, Abingdon, Oxfordshire, United Kingdom
Sonia Leon, Intel, Santa Clara, California
Rikky Muller, University of California, Berkeley, Berkeley, CA
Farhana Sheikh, Intel, Hillsboro, OR
Yildiz Sinangil, Apple, Cupertino, CA
Trudy Stetzler, Halliburton, Houston, TX
Ingrid Verbauwheide, KU Leuven, Leuven, Belgium
Alice Wang, MediaTek, San Jose, California
Rabia Tugce Yazicigil, Massachusetts Institute of Technology, Cambridge, MA

The Workshop on Circuits for Social Good highlights various ways that circuits can help address some of the most important challenges facing society today, ranging from health care to energy conservation.

The program aims to give a broad perspective on how one can have meaningful societal impact. It begins with several keynotes and invited talks from industry, academia and startups, followed by interactive round-table discussions on topics, including machine learning, medical devices, next generation communications, security and IoT, as well as discussions on career paths in research, product development, and entrepreneurship.

KEYNOTES**6:00 - 6:30 PM****Winning the Game in a Male-Dominated Industry*****Teresa H. Meng***

Reid Weaver Dennis Professor in Electrical Engineering, Emerita,
Stanford University, Palo Alto, CA; Founder of Atheros Communications

6:30 - 7:00 PM**Low-Power Design: How Can We Help Become Green?*****Nevine Nassif***

Intel Fellow, Hudson, MA

INVITED TALKS**7:00 - 7:15 PM****Pioneering Ultra-Low Power Technologies to Empower Personal Healthcare*****Esther Rodriguez-Villegas***

Professor/Chair in Low Power Electronics at Imperial College London, United Kingdom
Founder and CEO at Acurable; Co-Founder and CSO at TainiTec.

7:15 - 7:30 PM**Driving A Ground-Breaking Ultrathin Flexible Printed Battery to Market -
My Journey From Technologist to Entrepreneur*****Christine Ho***

Co-Founder and CEO at Imprint Energy, Alameda, CA

EE2:**Workshop on Circuits for Social Good****Research and Career Round Tables (Talk to an Expert!)****7:30pm - 8:00pm**

Short Pitches from Each Table

8:00pm - 9:00pm

Round Table Discussions

Next-Generation CommunicationsAlyssa Apsel, Professor at Cornell, Ithaca, NY
Azita Emami, Professor at Caltech, Pasadena, CA**Machine Learning & Multimedia Systems**Vivienne Sze, Associate Professor at MIT, Cambridge, MA
Marian Verhelst, Assistant Professor at KU Leuven, Leuven, Belgium**Medical Devices and Applications**Rikky Muller, Assistant Professor at University of California,
Berkeley, Berkeley, CA
Esther Rodriguez-Villegas, Professor at Imperial College London,
London, United Kingdom**Security and IoT**Edith Beigne, Senior Scientist at CEA-LETI, Grenoble, France
Ingrid Verbauwhede, Professor at KU Leuven, Leuven, Belgium**Careers in Industry**Andreia Cathelin, Fellow at ST Microelectronics, Crolles, France
Yildiz Sinangil, Circuit Designer at Apple, Cupertino, CA
Trudy Stetzler, Engineering Project Manager at Halliburton, Houston, TX
Bich-Yen Nguyen, Senior Fellow at Soitec, Austin, TX
Sonia Leon, Principal Engineer at Intel, Santa Clara, CA**Careers in Academia**Terri Fiez, Professor & Vice Chancellor of Research at University of Colorado Boulder,
Boulder, CO
Milin Zhang, Assistant Professor, Tsinghua University, Beijing, China**Entrepreneurship**Christine Ho, Co-Founder of Imprint Energy, Alameda, CA
Teresa H. Meng, Founder of Atheros Communications, Palo Alto

Plenary Session — Invited Papers

Chair: *Anantha Chandrakasan, Massachusetts Institute of Technology, Cambridge, MA*
ISSCC Conference Chair

Associate Chair: *Alison Burdett, Sensium Healthcare, Abingdon, United Kingdom*
ISSCC International Technical-Program Chair

FORMAL OPENING OF THE CONFERENCE

8:30 AM

1.1 Semiconductor Innovation: Is the party over or just getting started?

8:45 AM

Vincent Roche, *President & CEO, Analog Devices, Norwood, MA*

The future pace of semiconductor innovation is by no means certain. A little more than a decade ago, Dennard scaling ground to a halt. Symposia and media outlets have been speculating on what comes after Moore's Law for years now. Beyond these technology challenges, business challenges, as well, are putting pressure on traditional semiconductor innovation: semiconductor prices continue their steady decline while small geometry wafer fab facilities now cost close to \$10B to build.

In this environment, is there any room for continued innovation or is the future of the semiconductor industry defined by incrementalism, commoditization, and financial engineering? If our future is the latter, how will we meet the demands of a world where businesses, governments, and societies are digitizing at a blazing pace? The spread of pervasive ubiquitous sensing, rapid advances in artificial intelligence, heterogeneous integration, and the continued impact of digitization on virtually every industry on earth will require more, not less, semiconductor innovation.

The physicist and philosopher Thomas Kuhn might describe our situation as the crisis that catalyzes a new paradigm. So what is the next paradigm for semiconductor innovation? What is our path forward as scientists, technologists, and an industry?

1.2 Brain-Inspired Technologies: Towards Chips that Think

9:20 AM

Barbara De Salvo, *Deputy Director for Science and Long Term Research,*
CEA-Leti, Grenoble, France

Since the late 50s, brain-inspired computing has been regarded as an interesting alternative to conventional computational paradigms. Today, the omnipresence of "big data" and worldwide social interactions requires technologies capable of analyzing complex objects (such as sounds, images, or videos), in real time, and interact with humans in a cognitive way. The demand for computational efficiency and "intelligent" features has gone well beyond what can be achieved with traditional solutions. The advent of the Internet-of-Things has also introduced a new paradigm that supports a decentralized and hierarchical communication architecture, where a great deal of analytics processing should be done at the edge and at the end-devices instead of in the cloud. Specialized low-power architectures, inspired by the human brain, have thus recently become one of the most active research areas in the computing landscape, offering tremendous opportunities for novel applications. To map the embedded systems requirements, new challenges in brain-inspired technologies should be addressed, in particular automatic sensor fusion, system fault tolerance and data-privacy while achieving high recognition accuracy, low power consumption, and reducing cost.

In this talk, we will illustrate a research strategy – one encompassing algorithms, circuits, and components – to develop brain-inspired technologies and meet the needs of 21st-century applications. To explore the architecture of neural networks, an open software platform has been created and several neural network circuits conceived and fabricated. The use of innovative components, such as emerging resistive memories, advanced CMOS, and 3D technologies has been explored to allow for the implementation of cognitive tasks in neural networks. Those novel components bring memory closer to the processing unit and offer extraordinary potential to implement "intelligent" features, approaching the way knowledge is created and processed in the human brain. Several concrete examples will be given to illustrate how brain-inspired technologies are developed using a holistic research approach, where process development and integration, circuit design, system architecture, and learning algorithms are simultaneously optimized, opening the door to new disruptive applications.

ISSCC, SSCS, IEEE AWARD PRESENTATIONS **9:55 AM****BREAK** **10:20 AM****1.3 Future Mobile Society Enabled by Semiconductor Technology** **10:45 AM****Yukihiro Kato**, *Executive Director, DENSO, Aichi, Japan*

The automotive industry is in the midst of a once-in-a-century greatest transformation. The transformation of the automobile is a consequence of three technology trends: (1) electrification, (2) driving automation, and (3) vehicle interconnection. All three of these require dramatic advancement within semiconductor technologies. In this talk, our vision of the future mobile society is presented, focusing especially on automotive semiconductor electronics. To promote the electrification of the car, power semiconductors are a key technology. The energy conversion efficiency of the motor has been increased by IGBTs, and next-generation SiC MOSFETs will further increase efficiency. However, to put automated driving to practical use, both advanced sensors and intelligent SoCs are required. Improved performance of sensors, such as cameras, LIDARs, and millimeter-wave radars, with increased range and resolution are required to precisely monitor the total environment of the car. Path planning for automated driving involves recognizing the vehicle's proximity to nearby objects and the free space available. In this process, deep learning is an exceedingly useful method and highly sophisticated SoCs with GPUs are essential for its implementation. Finally, from the viewpoint of a connected vehicle, cars will shift from lumps of metal into something like a giant smartphone! Of course, in the connected vehicle, you can make a phone call, receive and/or transmit emails, do shopping, make payments, and so on. As well, updated maps are constantly available. But, also, each vehicle must be constantly aware of the status and intent of nearby vehicles. Clearly, to implement the intricacies of such an interconnected vehicle network, we need a myriad of semiconductors including communication ICs.

**1.4 50 Years of Computer Architecture:
From Mainframe CPUs to Neural-Network TPUs** **11:15 AM****David Patterson**, *Google, Mountain View, CA, University of California, Berkeley, CA*

This talk reviews a half-century of computer architecture: We start with the IBM System 360, which in 1964 introduced the concept of "binary compatibility". Next, came the idea of the "dominant microprocessor architecture", for which the early candidate was the Intel 432 which was shortly replaced by the emergency introduction of the Intel 80x86 in 1978. However, for the next 20 years, the Reduced Instruction Set Computers (RISC) became dominant. Then, the Very Long Instruction Word (VLIW) HP/Intel Itanium architecture was heralded as their replacement in 2001, but instead the role was usurped by AMD's introduction of the 64 bit 80x86. Thus, while the 80x86 dominated the PC-Era, RISCs have led thereafter, currently with 20B shipped annually (versus 0.4B 80x86s). Since the ending of Moore's Law and Dennard scaling has stalled performance of general-purpose microprocessors, domain-specific computer architectures are the only option left. An early example of this trend introduced by Google in 2015 is the Tensor Processing Unit (TPU) for cloud-based deep neural networking .

PRESENTATION TO PLENARY SPEAKERS **11:50 AM****CONCLUSION** **11:55 AM**

Processors

Session Chair: **Thomas Burd**, Advanced Micro Devices, Sunnyvale, CA
 Associate Chair: **Muhammad Khellah**, Intel, Hillsboro, OR

1:30 PM

2.1 SkyLake-SP: A 14nm 28-Core Xeon Processor

DS1 S. M. Tam, H. Muljono, M. Huang, S. Iyer, K. Royneogi, N. Satti, R. Qureshi, W. Chen, T. Wang, H. Hsieh, S. Vora, E. Wang, Intel, Santa Clara, CA

2:00 PM

2.2 IBM z14™: 14nm Microprocessor for the Next-Generation Mainframe

DS1 C. Berry¹, J. Warnock², J. Isakson³, J. Badar³, B. Bell⁴, F. Malmgioglio¹, G. Mayer⁵, D. Hamid¹, J. Surprise¹, D. Wolpert¹, O. Geva⁶, B. Huott¹, L. Siga⁷, S. Carey¹, R. Rizzolo¹, R. Nigaglioni³, M. Cichanowski³, D. Chidambarao⁷, C. Jacob¹, A. Saporito¹, A. O'neill¹, R. Sonnelitter¹, C. Zoellin¹, M. Wood¹, J. Neves¹

¹IBM Systems, Poughkeepsie, NY; ²IBM Systems, Yorktown Heights, NY

³IBM Systems, Austin, TX; ⁴IBM Systems, Rochester, MN

⁵IBM Systems, Boeblingen, Germany; ⁶IBM Systems, Tel Aviv, Israel

⁷IBM Systems, Hopewell Junction, NY

2:30 PM

2.3 An Energy-Efficient Graphics Processor Featuring Fine-Grain DVFS with Integrated Voltage Regulators, Execution-Unit Turbo, and Retentive Sleep in 14nm Tri-Gate CMOS

P. Meinerzhagen¹, C. Tokunaga¹, A. Malavasi¹, V. Vaidya¹, A. Mendon¹, D. Mathaikutty¹, J. Kulkarni¹, C. Augustine¹, M. Cho¹, S. Kim¹, G. Matthew¹, R. Jain¹, J. Ryan¹, C-C. Peng¹, S. Paul¹, S. Vangal¹, B. Perez Esparza¹, L. Cuellar¹, M. Woodruff¹, B. Iyer¹, S. Maiyuran², G. Chinya¹, C. Zou¹, Y. Liao¹, K. Ravichandran¹, H. Wang¹, M. Khellah¹, J. Tschanz¹, V. De¹, ¹Intel, Hillsboro, OR; ²Intel, Folsom, CA

Break 3:00 PM

3:15 PM

2.4 "Zeppelin": An SoC for Multichip Architectures

DS1 N. Beck¹, S. White¹, M. Paraschou², S. Naffziger², ¹AMD, Boxborough, MA
²AMD, Fort Collins, CO

3:45 PM

2.5 An Energy-Efficient Reconfigurable DTLs Cryptographic Engine for End-to-End Security in IoT Applications

U. Banerjee, C. Juvekar, A. Wright, Arvind, A. P. Chandrakasan
 Massachusetts Institute of Technology, Cambridge, MA

4:15 PM

2.6 A 595pW 14pJ/Cycle Microcontroller with Dual-Mode Standard Cells and Self-Startup for Battery-Indifferent Distributed Sensing

L. Lin, S. Jain, M. Alioto, National University of Singapore, Singapore

4:45 PM

2.7 A cm-Scale Self-Powered Intelligent and Secure IoT Edge Mote Featuring an Ultra-Low-Power SoC in 14nm Tri-Gate CMOS

T. Karnik¹, D. Kurian², P. Aseron¹, R. Dorrance¹, E. Alpman¹, A. Nicoara¹, R. Popov¹, L. Azarenkov¹, M. Moiseev¹, L. Zhao¹, S. Ghosh¹, R. Misoczki¹, A. Gupta², A. M², S. Muthukumar², S. Bhandari², Y. Satish², K. Jain², R. Flory¹, C. Kanthapani¹, E. Quijano³, B. Jackson¹, H. Luo⁴, S. Kim¹, V. Vaidya¹, A. Elsherbini⁵, R. Liu¹, F. Sheikh¹, O. Tickoo¹, I. Klotchkov¹, M. Sastry¹, S. Sun¹, M. Bhartiya², A. Srinivasan¹, Y. Hoskote⁶, H. Wang⁴, V. De¹, ¹Intel, Hillsboro, OR; ²Intel, Bangalore, India; ³Intel, Guadalajara, Mexico
⁴Intel, Santa Clara, CA; ⁵Intel, Chandler, AZ; ⁶ARM, Austin, TX

Conclusion 5:15 PM

Analog Techniques

Session Chair: *Youngcheol Chae*, Yonsei University, Seoul, Korea

Associate Chair: *Mahdi Kashmiri*, Robert Bosch, Palo Alto, CA

1:30 PM

3.1 A Quiet Digitally Assisted Auto-Zero-Stabilized Voltage Buffer with 0.6pA Input Current and 0.6 μ V Offset.

T. Rooijers, J. H. Huijsing, K. A. A. Makinwa

Delft University of Technology, Delft, The Netherlands

2:00 PM

DS1 3.2 A Regulation-Free Sub-0.5V 16/24MHz Crystal Oscillator for Energy-Harvesting BLE Radios with 14.2nJ Startup Energy and 31.8 μ W Steady-State Power

K-M. Lei¹, P-I. Mak¹, M-K. Law¹, R. P. Martins^{1,2}

¹University of Macau, Macau, China

²Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

2:30 PM

3.3 A CMOS Dual-RC Frequency Reference with \pm 250ppm Inaccuracy from -45°C to 85°C

Ç. Gürleyük, L. Pedalà, F. Sebastiano, K. A. A. Makinwa

Delft University of Technology, Delft, The Netherlands

Break 3:00 PM

3:15 PM

3.4 A 2 \times 20W 0.0013% THD+N Class-D Audio Amplifier with Consistent Performance up to Maximum Power Level

E. Cope, J. Aschieri, T. Lai, F. Zhao, W. Grandfield, M. Clifford, P. Rathfelder, Q. Liu,

S. Kavilipati, A. Vandergriff, G. Mialle, Qualcomm, Tempe, AZ

3:45 PM

3.5 A 0.0004% (-108dB) THD+N, 112dB-SNR, 3.15W Fully Differential Class-D Audio Amplifier with G_m Noise Cancellation and Negative Output-Common-Mode Injection Techniques

W-C. Wang, Y-H. Lin, MediaTek, Hsinchu, Taiwan

4:15 PM

3.6 A 0.96mA Quiescent Current, 0.0032% THD+N, 1.45W Class-D Audio Amplifier with Area-Efficient PWM-Residual-Aliasing Reduction

S-H. Chien, Y-W. Chen, T-H. Kuo; National Cheng Kung University, Tainan, Taiwan

4:45 PM

3.7 A Low-Power 3.25GS/s 4th-Order Programmable Analog FIR Filter Using Split-CDAC Coefficient Multipliers for Wideband Analog Signal Processing

S. Park¹, D. Shin², K-J. Koh¹, S. Raman¹, ¹Virginia Tech, Blacksburg, VA

²Intel, Hillsboro, OR

Conclusion 5:15 PM

mm-Wave Radios for 5G and Beyond

Session Chair: *Chun-Huat Heng*, National University of Singapore, Singapore

Associate Chair: *David McLaurin*, Analog Devices, Raleigh, NC

1:30 PM

4.1 Architectures and Technologies for the 5G mm-Wave Radio

T. Cameron, Analog Devices, Ottawa, Canada

2:00 PM

4.2 A 60GHz 144-Element Phased-Array Transceiver with 51dBm Maximum EIRP and $\pm 60^\circ$ Beam Steering for Backhaul Application

T. Sowlati, S. Sarkar, B. Perumana, W. L. Chan, B. Afshar, M. Boers, D. Shin, T. Mercer, W-H. Chen, A. Papio Toda, A. Grau Besoli, S. Yoon, S. Kyriazidou, P. Yang, V. Aggarwal, N. Vakilian, D. Rozenblit, M. Kahrizi, J. Zhang, A. Wang, P. Sen, D. Murphy, M. Mikhemar, A. Sajjadi, A. Mehrabani, B. Ibrahim, B. Pan, K. Juan, S. Xu, C. Guan, G. Geshvindman, K. Low, N. Kocaman, H. Eberhart, K. Kimura, I. Elgorriaga, V. Rousset, H. Xie, L. Shi, V. Kodavati, Broadcom, Irvine, CA

2:30 PM

4.3 A 23-to-30GHz Hybrid Beamforming MIMO Receiver Array with Closed-Loop Multistage Front-End Beamformers for Full-FoV Dynamic and Autonomous Unknown Signal Tracking and Blocker Rejection

M-Y. Huang, T. Chi, F. Wang, T-W. Li, H. Wang, Georgia Institute of Technology, Atlanta, GA

Break 3:00 PM

3:15 PM

4.4 A 28GHz Bulk-CMOS Dual-Polarization Phased-Array Transceiver with 24 Channels for 5G User and Basestation Equipment

J. D. Dunworth¹, A. Homayoun¹, B-H. Ku¹, Y-C. Ou¹, K. Chakraborty¹, G. Liu¹, T. Segoria¹, J. Lerdworatawee¹, J. W. Park¹, H-C. Park², H. Hedayati³, D. Lu¹, P. Monat¹, K. Douglas¹, V. Aparin¹, ¹Qualcomm, San Diego, CA

²*now with Samsung Electronics, Suwon, Korea; ³*now with Atlazo, San Diego, CA

3:45 PM

4.5 A Reconfigurable 28/37GHz Hybrid-Beamforming MIMO Receiver with Inter-Band Carrier Aggregation and RF-Domain LMS Weight Adaptation

S. Mondal, R. Singh, J. Paramesh, Carnegie Mellon University, Pittsburgh, PA

4:15 PM

DS1 4.6 A Fully Integrated Scalable W-Band Phased-Array Module with Integrated Antennas, Self-Alignment and Self-Test

S. Shahramian, M. Holyoak, A. Singh, B. Jalali Farahani, Y. Baeyens
Bell Laboratories, New Providence, NJ

4:45 PM

4.7 A 64GHz Full-Duplex Transceiver Front-End with an On-Chip Multifeed Self-Interference-Canceling Antenna and an All-Passive Canceler Supporting 4Gb/s Modulation in One Antenna Footprint

T. Chi, J. S. Park, S. Li, H. Wang, Georgia Institute of Technology, Atlanta, GA

Conclusion 5:15 PM

Image Sensors

Session Chair: *Hayato Wakabayashi, Sony Electronics, San Jose, CA*Associate Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan*

1:30 PM

- 5.1 A Back-Illuminated Global-Shutter CMOS Image Sensor with Pixel-Parallel 14b Subthreshold ADC**
M. Sakakibara¹, K. Ogawa¹, S. Sakai¹, Y. Tochigi¹, K. Honda¹, H. Kikuchi¹, T. Wada¹, Y. Kamikubo¹, T. Miura¹, M. Nakamizo¹, N. Jyo², R. Hayashibara², Y. Furukawa², S. Miyata², S. Yamamoto², Y. Ota¹, H. Takahashi¹, T. Taura¹, Y. Oike¹, K. Tatani¹, T. Nagano¹, T. Ezaki¹, T. Hirayama¹, ¹Sony Semiconductor Solutions, Atsugi, Japan
²Sony Semiconductor Manufacturing, Kumamoto, Japan; ³Sony LSI Design, Fukuoka, Japan

2:00 PM

- DS1 5.2 An 8K4K-Resolution 60fps 450ke⁻Saturation-Signal Organic-Photoconductive-Film Global-Shutter CMOS Image Sensor with In-Pixel Noise Canceller**
K. Nishimura¹, S. Shishido¹, Y. Miyake¹, M. Yanagida¹, Y. Satou¹, M. Shouho¹, H. Kanehara¹, R. Sakaida¹, Y. Sato¹, J. Hirase¹, Y. Tomekawa¹, Y. Abe², H. Fujinaka², Y. Matsunaga², M. Murakami¹, M. Harada¹, Y. Inoue¹,
¹Panasonic, Moriguchi, Japan; ²Panasonic Semiconductor Solutions, Nagaokakyo, Japan
³Panasonic, Kyoto, Japan

2:15 PM

- 5.3 A 1/2.8-inch 24Mpixel CMOS Image Sensor with 0.9 μ m Unit Pixels Separated by Full-Depth Deep-Trench Isolation**
Y. Kim, W. Choi, D. Park, H. Jeoung, B. Kim, Y. Oh, S. Oh, B. Park, E. Kim, Y. Lee, T. Jung, Y. Kim, S. Yoon, S. Hong, J. Lee, S. Jung, C-R. Moon, Y. Park, D. Lee, D. Chang, Samsung Electronics, Hwaseong, Korea

2:30 PM

- DS1 5.4 A 1/4-inch 3.9Mpixel Low-Power Event-Driven Back-Illuminated Stacked CMOS Image Sensor**
O. Kumagai¹, A. Niwa¹, K. Hanzawa², H. Kato¹, S. Futami¹, T. Ohyama¹, T. Imoto¹, M. Nakamizo¹, H. Murakami², T. Nishino¹, A. Bostamam¹, T. Iinuma¹, N. Kuzuya¹, K. Hatsukawa², B. Frederick², B. William², T. Wakano¹, T. Nagano¹, H. Wakabayashi², Y. Nitta¹, ¹Sony Semiconductor Solutions, Atsugi, Japan
²Sony Electronics, San Jose, CA; ³Sony LSI Design, Atsugi, Japan

Break 3:00 PM

3:15 PM

- DS1 5.5 A 1.1 μ m-Pitch 13.5Mpixel 3D-Stacked CMOS Image Sensor Featuring 230fps Full-High-Definition and 514fps High-Definition Videos by Reading 2 or 3 Rows Simultaneously Using a Column-Switching Matrix**
P-S. Chou, C-H. Chang, M. M. Mhala, C-M. Liu, C-P. Chao, C-Y. Huang, H. Tu, T. Wu, S-F. Yeh, S. Takahashi, Y. Huang, TSMC, Hsinchu, Taiwan

3:30 PM

- DS1 5.6 A 2.1 μ m 33Mpixel CMOS Imager with Multi-Functional 3-Stage Pipeline ADC for 480fps High-Speed Mode and 120fps Low-Noise Mode**
T. Yasue¹, K. Tomioka¹, R. Funatsu¹, T. Nakamura¹, T. Yamasaki¹, H. Shimamoto¹, T. Kosugi², J. Sungwook², T. Watanabe^{2,3}, M. Nagase², T. Kitajima², S. Aoyama², S. Kawahito^{2,3}
¹NHK Science & Technology Research Laboratories, Tokyo, Japan
²Brookman Technology, Hamamatsu, Japan; ³Shizuoka University, Hamamatsu, Japan

3:45 PM

- DS1 5.7 A 20ch TDC/ADC Hybrid SoC for 240 \times 96-Pixel 10%-Reflection <0.125%-Precision 200m-Range Imaging LiDAR with Smart Accumulation Technique**
K. Yoshioka¹, H. Kubota¹, T. Fukushima¹, S. Kondo¹, T. T. Ta¹, H. Okuni¹, K. Watanabe¹, Y. Ojima¹, K. Kimura¹, S. Hosoda¹, Y. Oota¹, T. Koizumi¹, N. Kawabe¹, Y. Ishii¹, Y. Iwagami¹, S. Yagi¹, I. Fujisawa², N. Kano¹, T. Sugimoto¹, D. Kurose¹, N. Waki¹, Y. Higashi², T. Nakamura¹, Y. Nagashima¹, H. Ishii¹, A. Sai¹, N. Matsumoto¹
¹Toshiba, Kawasaki, Japan; ²Toshiba Memory, Kawasaki, Japan

4:15 PM

- DS1 5.8 1Mpixel 65nm BSI 320MHz Demodulated TOF Image Sensor with 3.5 μ m Global Shutter Pixels and Analog Binning**
C. S. Bamji, S. Mehta, B. Thompson, T. Elkhatib, S. Wurster, O. Akkaya, A. Payne, J. Godbaz, M. Fenton, V. Rajasekaran, L. Prather, S. Nagaraja, V. Mogallapu, D. Snow, R. McCauley, M. Mukadam, I. Agi, S. McCarthy, Z. Xu, T. Perry, W. Qian, V-H. Chan, P. Adepu, G. Ali, M. Ahmed, A. Mukherjee, S. Nayak, D. Gampell, S. Acharya, L. Kordus, P. O'Connor, Microsoft, Mountain View, CA

4:30 PM

- 5.9 A 256 \times 256 45/65nm 3D-Stacked SPAD-Based Direct TOF Image Sensor for LiDAR Applications with Optical Polar Modulation for up to 18.6dB Interference Suppression**
A. Ronchini Ximenes¹, P. Padmanabhan², M-J. Lee², Y. Yamashita³, D. N. Young³, E. Charbon^{1,2}
¹Delft University of Technology, Delft, The Netherlands; ²EPFL, Neuchatel, Switzerland; ³TSMC, Hsinchu, Taiwan

4:45 PM

- DS1 5.10 A 32 \times 32-Pixel Time-Resolved Single-Photon Image Sensor with 44.64 μ m Pitch and 19.48% Fill-Factor with On-Chip Row/Frame Skipping Features Reaching 800kHz Observation Rate for Quantum Physics Applications**
L. Gasparini¹, M. Zarghami¹, H. Xu¹, L. Parmesan¹, M. Moreno Garcia¹, M. Unternährer², B. Bessire², A. Stefanov², D. Stoppa^{1,3}, M. Perenzoni¹, ¹Fondazione Bruno Kessler (FBK), Trento, Italy
²University of Bern, Bern, Switzerland; ³now with ams AG, Rueschlikon, Switzerland

Conclusion 5:15 PM

Ultra-High-Speed Wireline

Session Chair: **Mounir Meghelli**, IBM T. J. Watson Research Center,
Yorktown Heights, NY

Associate Chair: **Hyeon-Min Bae**, KAIST, Daejeon, Korea

1:30 PM

6.1 A 112Gb/s PAM-4 Transmitter with 3-Tap FFE in 10nm CMOS

J. Kim, A. Balankutty, R. Dokania, A. Elshazly, H. S. Kim, S. Kundu, S. Weaver, K. Yu, F. O'Mahony

Intel, Hillsboro, OR

2:00 PM

6.2 A 112Gb/s 2.6pJ/b 8-Tap FFE PAM-4 SST TX in 14nm CMOS

C. Menolfi¹, M. Braendli¹, P. A. Francese¹, T. Morf¹, A. Cevrero¹, M. Kossel¹, L. Kull¹, D. Luu^{1,2}, I. Ozkaya^{1,3}, T. Toifl¹

¹IBM Zurich Research Laboratory, Rueschlikon, Switzerland

²ETH Zurich, Zurich, Switzerland

³EPFL, Lausanne, Switzerland

2:30 PM

6.3 A 4-Lane 1.25-to-28.05Gb/s Multi-Standard 6pJ/b 40dB Transceiver in 14nm FinFET with Independent TX/RX Rate Support

M. S. Jalali, M. H. Taghavi, A. McLaren, J. Pham, K. Farzan, D. Diclemente, M. van Ierssel, W. Song, S. Asgaran, C. Holdenried, S. Sadr, Rambus, Toronto, ON, Canada

Break 3:00 PM

3:15 PM

6.4 A Fully Adaptive 19-to-56Gb/s PAM-4 Wireline Transceiver with a Configurable ADC in 16nm FinFET

P. Upadhyaya¹, C. F. Poon¹, S. W. Lim², J. Cho¹, A. Roldan², W. Zhang¹, J. Namkoong¹, T. Pham¹, B. Xu¹, W. Lin¹, H. Zhang¹, N. Narang², K. H. Tan², G. Zhang¹, Y. Frans¹, K. Chang¹

¹Xilinx, San Jose, CA; ²Xilinx, Singapore

3:45 PM

6.5 A 64Gb/s PAM-4 Transceiver Utilizing an Adaptive Threshold ADC in 16nm FinFET

L. Wang¹, Y. Fu², M. LaCroix³, E. Chong³, A. Chan Carusone¹

¹University of Toronto, Toronto, Canada; ²Huawei, Markham, Canada

³Huawei, Ottawa, Canada

4:15 PM

6.6 A 4.9pJ/b 16-to-64Gb/s PAM-4 VSR Transceiver in 28nm FDSOI CMOS

E. Depaoli¹, E. Monaco¹, G. Steffan¹, M. Mazzini¹, H. Zhang², W. Audoglio¹, O. Belotti¹, A. A. Rossi¹, G. Albasini¹, M. Pozzoni¹, S. Erba¹, A. Mazzanti²

¹STMicroelectronics, Pavia, Italy; ²University of Pavia, Pavia, Italy

4:45 PM

6.7 A 32Gb/s 133mW PAM-4 Transceiver with DFE Based on Adaptive Clock Phase and Threshold Voltage in 65nm CMOS

L. Tang, W. Gai, L. Shi, X. Xiang, K. Sheng, A. He, Peking University, Beijing, China

Conclusion 5:15 PM

Demonstration Session 1, Monday February 12th, 5:00-7:00 PM

This year, the Demonstration Session extending in selected regular papers, both Academic and Industrial, will take place on Monday February 12th, and Tuesday February 13th, from 5 pm until 7 pm in the Golden Gate Hall. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2018, as noted by the symbol **DS1**

- 2.1 SkyLake-SP: A 14nm 28-Core Xeon Processor
- 2.2 IBM z14™: 14nm Microprocessor for the Next-Generation Mainframe
- 2.4 "Zeppelin": An SoC for Multichip Architectures
- 2.5 An Energy-Efficient Reconfigurable DTLs Cryptographic Engine for End-to-End Security in IoT Applications
- 2.7 A cm-Scale Self-Powered Intelligent and Secure IoT Edge Mote Featuring an Ultra-Low-Power SoC in 14nm Tri-Gate CMOS
- 3.2 A Regulation-Free Sub-0.5V 16/24MHz Crystal Oscillator for Energy-Harvesting BLE Radios with 14.2nJ Startup Energy and 31.8μW Steady-State Power
- 4.6 A Fully Integrated Scalable W-Band Phased-Array Module with Integrated Antennas, Self-Alignment and Self-Test
- 5.2 An 8K4K-Resolution 60fps 450ke-Saturation-Signal Organic-Photoconductive-Film Global-Shutter CMOS Image Sensor with In-Pixel Noise Canceller
- 5.4 A 1/4-inch 3.9Mpixel Low-Power Event-Driven Back-Illuminated Stacked CMOS Image Sensor
- 5.5 A 1.1μm-Pitch 13.5Mpixel 3D-Stacked CMOS Image Sensor Featuring 230fps Full-High-Definition and 514fps High-Definition Videos by Reading 2 or 3 Rows Simultaneously Using a Column-Switching Matrix
- 5.6 A 2.1μm 33Mpixel CMOS Imager with Multi-Functional 3-Stage Pipeline ADC for 480fps High-Speed Mode and 120fps Low-Noise Mode
- 5.7 A 20ch TDC/ADC Hybrid SoC for 240×96-Pixel 10%-Reflection <0.125%-Precision 200m-Range Imaging LiDAR with Smart Accumulation Technique
- 5.8 1Mpixel 65nm BSI 320MHz Demodulated TOF Image Sensor with 3.5μm Global Shutter Pixels and Analog Binning
- 5.10 A 32×32-Pixel Time-Resolved Single-Photon Image Sensor with 44.64μm Pitch and 19.48% Fill-Factor with On-Chip Row/Frame Skipping Features Reaching 800kHz Observation Rate for Quantum Physics Applications
- 6.3 A 4-Lane 1.25-to-28.05Gb/s Multi-Standard 6pJ/b 40dB Transceiver in 14nm FinFET with Independent TX/RX Rate Support
- 6.4 A Fully Adaptive 19-to-56Gb/s PAM-4 Wireline Transceiver with a Configurable ADC in 16nm FinFET
- 7.4 A 55nm Time-Domain Mixed-Signal Neuromorphic Accelerator with Stochastic Synapses and Embedded Reinforcement Learning for Autonomous Micro-Robots
- 7.7 A PUF Scheme Using Competing Oxide Rupture with Bit Error Rate Approaching Zero
- 8.1 A 960pW Co-Integrated-Antenna Wireless Energy Harvester for WiFi Backchannel Wireless Powering
- 8.2 A 70W and 90% GaN-Based Class-E Wireless-Power-Transfer System with Automatic-Matching-Point-Search Control for Zero-Voltage Switching and Zero-Voltage-Derivative Switching
- 8.3 A Reconfigurable Cross-Connected Wireless-Power Transceiver for Bidirectional Device-to-Device Charging with 78.1% Total Efficiency
- 8.8 A 30nA Quiescent 80nW-to-14mW Power-Range Shock-Optimized SECE-Based Piezoelectric Harvesting Interface with 420% Harvested-Energy Improvement
- 9.1 A Multimode 76-to-81GHz Automotive Radar Transceiver with Autonomous Monitoring
- 9.2 A 253mW/Channel 4TX/4RX Pulsed Chirping Phased-Array Radar TRX in 65nm CMOS for X-Band Synthetic-Aperture Radar Imaging
- 9.6 A 120Gb/s 16QAM CMOS Millimeter-Wave Wireless Transceiver
- 10.1 Chopped Rate-to-Digital FM Gyroscope with 40ppm Scale Factor Accuracy and 1.2dph Bias

EE3: Industry Showcase

Organizers: **Alison Burdett**, *Sensium Healthcare, Abingdon, Oxfordshire, United Kingdom*
Eugenio Cantatore, *Eindhoven University of Technology, Eindhoven, The Netherlands*
Kush Gulati, *Omni Design Tech., Milpitas, CA*
Yan Li, *Western Digital, Milpitas, CA*

This year at ISSCC, on the 65th anniversary of the conference, a new event called the Industry Showcase will be introduced for the first time. Following the recognized role of ISSCC as the foremost global forum for advances in solid-state circuits and systems-on-chip (SoCs), the goal of this event will be to highlight the role of silicon in the creation of novel products. It will feature short presentations as well as interactive demonstrations where attendees can have a hands-on experience with each featured innovation. The featured presentations were chosen through a nomination and voting process by members of the Industry Showcase Committee, and represent an exciting introduction to the next generation of applications and products enabled by the sustained evolution of solid-state integrated circuits.

Amongst those participating will be:

- Infineon (60 GHz gesture-recognition radar)
- Google (Tensor Processing Unit)
- Qualcomm (Structured-light 3D depth sensing camera)
- Sony (Xperia touch smart projector)
- Elliptic Labs (Ultrasound gesture recognition)
- Nvidia (Deep learning)
- Ultrahaptics (Ultrasound touchless interfaces)
- Novelda (single-chip UWB sensing)
- Chronocam (Bio-inspired image sensors)

COMMITTEE MEMBERS

Shuichi Nagai
 Long Yan
 Abbas Komijani
 Roberto Nonis
 Alan Wong
 David McLaurin
 John Maneatis
 Calvin Chao
 Tim Piessens
 Vadim Ivanov
 Jan Westra
 Yung-Shiang Shu
 Stephane LeTual
 Yogesh Ramadass

Panasonic, Osaka, Japan
 Samsung, Hwaesong-si, Korea
 Apple, Cupertino, CA
 Infineon, Villach, Austria
 EnSilica, Abingdon, UK
 Analog Devices, Raleigh, NC
 TrueCircuits, Los Altos, CA
 TSMC, Hsinchu City, Taiwan
 icSense, Leuven, Belgium
 Texas Instruments, Tucson, AZ
 Broadcom, Bunnik, The Netherlands
 MediaTek, Hsinchu City, Taiwan
 STmicroelectronics, Crolles, France
 TI, San Jose, CA

EE4: Figures-of-Merit on Trial

Organizers: **Kostas Doris**, *NXP, Eindhoven, The Netherlands*
Stefano Stanzione, *imec-NL, Eindhoven, The Netherlands*
Paul Ferguson, *Analog Devices, Wilmington, MA*

Moderator: **Gabriele Manganaro**, *Analog Devices, Wilmington, MA*

Mixed-signal/RF circuits are characterized by a wide variety of performance parameters and diverse functionality. A figure of merit (FOM) provides a unique, simple and objective metric that allows normalizing and comparing circuits and systems of the same class. On the other hand, does the minimalistic simplicity of any single metric sacrifice more than it offers? Doesn't engineering practice intrinsically require designing and judging a far more complex reality than the monochromatic reductionism that an FOM can provide? For instance, in the case of analog-to-digital converters, the ability to drive the ADC's input, to clock it, to integrate it or interface it with other processing units, to supply power to it, are just a few real-life examples of factors that can make or break a converter architecture and the signal chain embedding it. These factors are not considered in any FOM, with potentially catastrophic consequences.

Enough already with the cult of FOMs? Open the doors to a new age of purely human subjective calls? You, the audience, be the judge.

This panel will probe the weaknesses and strengths of popular analog FOMs in an entertaining and educational way: To this end, the room will become a tribunal with the moderator as judge. For each FOM on trial, two panelists will officiate, one becoming the defending advocate of the FOM, and the other the prosecutor, while the audience will become the jury, that will decide which of the two contestants will win.

Panelists

Filip Tavernier, *KU Leuven, Leuven, Belgium*

Bob Dobkin, *Analog Devices, Milpitas, CA*

Anton de Graauw, *NXP Semiconductors, Eindhoven, The Netherlands*

Jason T. Stauth, *Thayer School of Engineering at Dartmouth Hanover, NH*

Lawrence Loh, *MediaTek, San Jose, CA*

Pietro Andreani, *Lund University, Lund, Sweden*

Neuromorphic, Clocking and Security Circuits

Session Chair: *Youngmin Shin*, Samsung, Hwasung, Korea

Associate Chair: *Phillip Restle*, IBM T. J. Watson Research Center,
Yorktown Heights, NY

8:30 AM

- 7.1 A 0.0056mm² All-Digital MDLL Using Edge Re-Extraction, Dual-Ring VCOs and a 0.3mW Block-Sharing Frequency Tracking Loop Achieving 292fs_{rms} Jitter and -249dB FOM**

S. Yang¹, J. Yin¹, P-I. Mak¹, R. P. Martins^{1,2}, ¹University of Macau, Macau, China

²Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

9:00 AM

- 7.2 A 0.02mm² Fully Synthesizable Period-Jitter Sensor Using Stochastic TDC Without Reference Clock and Calibration in 10nm CMOS Technology**

K. Choo, H. Kim, W. Kim, J. Kim, T. Kim, H. Ko, Samsung Electronics, Hwaseong, Korea

9:30 AM

- 7.3 A 0.3-to-1.2V Frequency-Scalable Fractional-N ADPLL with a Speculative Dual-Referenced Interpolating TDC**

M. Lee¹, S. Kim², H. Cho¹, J. Koo¹, K-H. Cho², J-H. Cho², B. Kim¹, H-J. Park¹, J-Y. Sim¹

¹Pohang University of Science and Technology, Pohang, Korea

²Samsung Electronics, Hwaseong, Korea

Break 10:00 AM

10:15 AM

- DS1 7.4 A 55nm Time-Domain Mixed-Signal Neuromorphic Accelerator with Stochastic Synapses and Embedded Reinforcement Learning for Autonomous Micro-Robots**

A. Amravati, S. B. Nasir, S. Thangadurai, I. Yoon, A. Raychowdhury

Georgia Institute of Technology, Atlanta, GA

10:45 AM

- 7.5 An Enhanced-Security Buck DC-DC Converter with True-Random-Number-Based Pseudo Hysteresis Controller for Internet-of-Everything (IoE) Devices**

W-H. Yang¹, L-C. Chu¹, S-H. Yang¹, Y-J. Lai¹, S-Q. Chen¹, K-H. Chen¹, Y-H. Lin², S-R. Lin², T-Y. Tsa², ¹National Chiao Tung University, Hsinchu, Taiwan

²Realtek Semiconductor, Hsinchu, Taiwan

11:15 AM

- 7.6 A Secure Camouflaged Logic Family Using Post-Manufacturing Programming with a 3.6GHz Adder Prototype in 65nm CMOS at 1V Nominal V_{DD}**

N. E. C. Akkaya, B. Erbagci, K. Mai, Carnegie Mellon University, Pittsburgh, PA

11:30 AM

- DS1 7.7 A PUF Scheme Using Competing Oxide Rupture with Bit Error Rate Approaching Zero**

M-Y. Wu, T-H. Yang, L-C. Chen, C-C. Lin, H-C. Hu, F-Y. Su, C-M. Wang, J-H. Huang,

H-M. Chen, C-H. Lu, E-S. Yang, R-J. Shen, eMemory, Hsinchu, Taiwan

11:45 AM

- 7.8 A 445F² Leakage-Based Physically Unclonable Function with Lossless Stabilization Through Remapping for IoT Security**

J. Lee, D. Lee, Y. Lee, Y. Lee, Sungkyunkwan University, Suwon, Korea

Conclusion 12:15 PM

Wireless Power and Harvesting

Session Chair: *Yuan Gao, IME, A*STAR, Singapore*Associate Chair: *Zhiliang Hong, Fudan University, Shanghai, China*

8:30 AM

- DS1** 8.1 **A 960pW Co-Integrated-Antenna Wireless Energy Harvester for WiFi Backchannel Wireless Powering**

*K. R. Sadagopan¹, J. Kang¹, Y. Ramadass², A. Natarajan¹*¹Oregon State University, Corvallis, OR; ²Texas Instruments, Santa Clara, CA

9:00 AM

- DS1** 8.2 **A 70W and 90% GaN-Based Class-E Wireless-Power-Transfer System with Automatic-Matching-Point-Search Control for Zero-Voltage Switching and Zero-Voltage-Derivative Switching**

*C-H. Yeh¹, Y-T. Lin¹, C-C. Kuo¹, C-J. Huang¹, C-Y. Xie¹, S-F. Lu¹, W-H. Yang¹, K-H. Chen¹, K-C. Liu¹, Y-H. Lin²*¹National Chiao Tung University, Hsinchu, Taiwan; ²Realtek Semiconductor, Hsinchu, Taiwan

9:30 AM

- DS1** 8.3 **A Reconfigurable Cross-Connected Wireless-Power Transceiver for Bidirectional Device-to-Device Charging with 78.1% Total Efficiency**

F. Mao¹, Y. Lu¹, S-P. U^{1,2}, R. P. Martins^{1,3}, ¹University of Macau, Macau, China²Synopsys Macau, Macau, China; ³Instituto Superior Técnico/Universidade de Lisboa, Lisbon, Portugal

9:45 AM

- 8.4 **A 13.56MHz Wireless Power and Data Transfer Receiver Achieving 75.4% Effective-Power-Conversion Efficiency with 0.1% ASK Modulation Depth and 9.2mW Output Power**

*Y. Wang¹, D. Ye¹, L. Lyu¹, Y. Xiang¹, H. Min¹, C-J. R. Shi^{1,2}*¹Fudan University, Shanghai, China; ²University of Washington, Seattle, WA

Break 10:00 AM

10:15 AM

- 8.5 **MISIMO: A Multi-Input Single-Inductor Multi-Output Energy Harvester Employing Event-Driven MPPT Control to Achieve 89% Peak Efficiency and a 60,000x Dynamic Range in 28nm FDSOI**

S. S. Amin, P. P. Mercier, University of California, San Diego, La Jolla, CA

10:45 AM

- 8.6 **A 4.5-to-16 μ W Integrated Triboelectric Energy-Harvesting System Based on High-Voltage Dual-Input Buck Converter with MPPT and 70V Maximum Input Voltage**

I. Park, J. Maeng, D. Lim, M. Shim, J. Jeong, C. Kim, Korea University, Seoul, Korea

11:00 AM

- 8.7 **A Piezoelectric Energy-Harvesting Interface Circuit with Fully Autonomous Conjugate Impedance Matching, 156% Extended Bandwidth, and 0.38 μ W Power Consumption**

*Y. Cai¹, Y. Manoli^{1,2}*¹University of Freiburg - IMTEK, Freiburg, Germany; ²Hahn-Schickard, Villingen-Schwenningen, Germany

11:15 AM

- DS1** 8.8 **A 30nA Quiescent 80nW-to-14mW Power-Range Shock-Optimized SECE-Based Piezoelectric Harvesting Interface with 420% Harvested-Energy Improvement**

*A. Quelen¹, A. Morel¹, P. Gasnier¹, R. Grézaud¹, S. Monfray², G. Pillonnet¹*¹CEA-LETI-MINATEC, Grenoble, France²STMicroelectronics, Crolles, France

11:45 AM

- 8.9 **A Fully Integrated Split-Electrode-Synchronized-Switch Harvesting-on-Capacitors (SE-SSHC) Rectifier for Piezoelectric Energy Harvesting with Between 358% and 821% Power-Extraction Enhancement**

S. Du, A. A. Seshia, University of Cambridge, Cambridge, United Kingdom

12:00 PM

- 8.10 **A 13.56MHz Time-Interleaved Resonant-Voltage-Mode Wireless-Power Receiver with Isolated Resonator and Quasi-Resonant Boost Converter for Implantable Systems**

*S-U. Shin¹, M. Choi¹, S-T. Koh¹, Y. Yang¹, S. Jung², Y-H. Sohn¹, S-H. Park¹, Y. Ju¹, Y. Jo¹, Y. Huh¹, S. Choi¹, S. J. Kim², G-H. Cho¹*¹KAIST, Daejeon, Korea; ²Samsung Advanced Institute of Technology, Suwon, Korea

Conclusion 12:15 PM

Wireless Transceivers and Techniques

Session Chair: *Alan Wong*, *EnSilica*, *Abingdon*, *United Kingdom*

Associate Chair: *Xin He*, *NXP*, *Eindhoven*, *The Netherlands*

8:30 AM

9.1 **A Multimode 76-to-81GHz Automotive Radar Transceiver with Autonomous Monitoring**

DS1

B. P. Ginsburg¹, K. Subburaj², S. Samala¹, K. Ramasubramanian², J. Singh², S. Bhatara², S. Murali², D. Breen¹, M. Moallem¹, K. Dandu¹, S. Jalan^{2,3}, N. Nayak¹, R. Sachdev², I. Prathapan², K. Bhatia¹, T. Davis¹, E. Seok¹, H. Parthasarathy², R. Chatterjee², V. Srinivasan¹, V. Giannini^{1,4}, A. Kumar², R. Kulak¹, S. Ram², P. Gupta², Z. Parkar², S. Bhardwaj², R. Y.C.², R. K.A.², A. Shrimal², V. Rentala¹,
¹Texas Instruments, Dallas, TX; ²Texas Instruments, Bangalore, India
³Intel, Bangalore, India; ⁴Uhnder, Austin, TX

9:00 AM

9.2 **A 253mW/Channel 4TX/4RX Pulsed Chirping Phased-Array Radar TRX in 65nm CMOS for X-Band Synthetic-Aperture Radar Imaging**

DS1

L. Lou¹, K. Tang¹, B. Chen¹, T. Guo¹, Y. Wang², W. Wang¹, Z. Fang¹, Z. Liu¹, Y. Zheng¹
¹Nanyang Technological University, Singapore
²Singapore University of Technology and Design, Singapore

9:30 AM

9.3 **A Highly Reconfigurable 65nm CMOS RF-to-Bits Transceiver for Full-Band Multicarrier TDD/FDD 2G/3G/4G/5G Macro Basestations**

D. J. McLaurin¹, K. G. Gard¹, R. P. Schubert², M. J. Manglan³, H. Zhu⁴, D. Alldred⁵, Z. Li⁶, S. R. Bal¹, J. Fan¹, O. E. Gysel¹, C. M. Mayer², T. Montalvo¹, ¹Analog Devices, Raleigh, NC
²Analog Devices, Norwood, MA; ³Analog Devices, Greensboro, NC
⁴Analog Devices, Wilmington, MA; ⁵Analog Devices, Toronto, Canada

Break 10:00 AM

10:15 AM

9.4 **A 40Gb/s 6pJ/b RX Baseband in 28nm CMOS for 60GHz Polarization MIMO**

S. Kang¹, C. Thakkar¹, N. Narevsky², K. Dasgupta¹, S. Daneshgar¹, J. Jaussi¹, B. Casper¹
¹Intel, Hillsboro, OR; ²University of California, Berkeley, CA

10:45 AM

9.5 **A 27.8Gb/s 11.5pJ/b 60GHz Transceiver in 28nm CMOS with Polarization MIMO**

S. Daneshgar, K. Dasgupta, C. Thakkar, A. Chakrabarti, S. Yamada, D. Choudhury, J. Jaussi, B. Casper, Intel, Hillsboro, OR

11:15 AM

9.6 **A 120Gb/s 16QAM CMOS Millimeter-Wave Wireless Transceiver**

DS1

K. K. Tokgoz¹, S. Maki¹, J. Pang¹, N. Nagashima¹, I. Abdo¹, S. Kawai¹, T. Fujimura¹, Y. Kawano², T. Suzuki², T. Iwa², K. Okada¹, A. Matsuzawa¹
¹Tokyo Institute of Technology, Tokyo, Japan; ²Fujitsu Laboratories, Atsugi, Japan

11:30 AM

9.7 **A Broadband and Deep-TX Self-Interference Cancellation Technique for Full-Duplex and Frequency-Domain-Duplex Transceiver Applications**

K-D. Chu, M. Katanbaf, T. Zhang, C. Su, J. C. Rudell, University of Washington, Seattle, WA

11:45 AM

9.8 **A 1.4-to-2.7GHz High-Efficiency RF Transmitter with an Automatic 3F_{LO}-Suppression Tracking-Notch-Filter Mixer Supporting HPUE in 14nm FinFET CMOS**

Q. Liu, D. Kwon, Q. Bui, J. Choi, J. Lee, S. Baek, S. Heo, T. Byunghak Cho
 Samsung Electronics, Suwon, Korea

12:00 PM

9.9 **A High-Efficiency 28GHz Outphasing PA with 23dBm Output Power Using a Triaxial Balun Combiner**

B. Rabet¹, J. Buckwalter², ¹University of California, San Diego, La Jolla, CA
²University of California, Santa Barbara, Santa Barbara, CA

Conclusion 12:15 PM

Sensor Systems

Session Chair: *Michael Kraft, KU Leuven, Leuven, Belgium*
 Associate Chair: *Masayuki Miyamoto, Wacom, Tokyo, Japan*

8:30 AM

10.1 Chopped Rate-to-Digital FM Gyroscope with 40ppm Scale Factor Accuracy and 1.2dph Bias

DS1

B. Eminoglu, B. E. Boser, University of California, Berkeley, CA

9:00 AM

10.2 Personal Inertial Navigation System Employing MEMS Wearable Ground Reaction Sensor Array and Interface ASIC Achieving a Position Accuracy of 5.5m Over 3km Walking Distance Without GPS

DS2

Q. Guo¹, W. Deng², O. Bebek³, C. Cavusoglu⁴, C. Mastrangelo¹, D. Young¹

¹University of Utah, Salt Lake City, UT; ²University of California, Berkeley, CA

³Ozyegin University, Istanbul, Turkey; ⁴Case Western Reserve University, Cleveland, OH

9:15 AM

10.3 Multi-Way Interactive Capacitive Touch System with Palm Rejection of Active Stylus for 86" Touch Screen Panels

DS2

J-S. An¹, S-H. Han², K-B. Park¹, J. E. Kim³, J-H. Ye⁴, S-H. Lee¹, J-Y. Jeong¹, J. S. Kim¹, K-H. Baek³, K-S. Chung¹, S-K. Hong¹, O-K. Kwon¹, ¹Hanyang University, Seoul, Korea

²Leading UI, Anyang, Korea; ³Chung-Ang University, Seoul, Korea; ⁴MiraeTNS, Chungju, Korea

9:30 AM

10.4 A Noise-Immune Stylus Analog Front-End Using Adjustable Frequency Modulation and Linear-Interpolating Data Reconstruction for Both Electrically Coupled Resonance and Active Styluses

K-H. Lee¹, S-P. Nam¹, J-H. Lee¹, M. Choi¹, H-J. Ko¹, S-H. Byun¹, J-C. Lee¹, Y-H. Lee¹, Y-C. Rhee¹, Y-K. Choi¹, B-H. Kang², C-B. Park², S. Park², T. Kim²

¹Samsung Electronics, Hwaseong, Korea; ²Samsung Electronics, Suwon, Korea

Break 10:00 AM

10:15 AM

10.5 A 0.91mW/Element Pitch-Matched Front-End ASIC with Integrated Subarray Beamforming ADC for Miniature 3D Ultrasound Probes

C. Chen¹, Z. Chen¹, D. Bera², E. Noothout¹, Z-Y. Chang¹, M. Tan¹, H. J. Vos^{1,2}, J. G. Bosch², M. D. Verweij^{1,2}, N. de Jong^{1,2}, M. A. Pertijs¹, ¹Delft University of Technology, Delft, The Netherlands

²Erasmus MC, Rotterdam, The Netherlands

10:45 AM

10.6 Single-Chip Reduced-Wire Active Catheter System with Programmable Transmit Beamforming and Receive Time-Division Multiplexing for Intracardiac Echocardiography

G. Jung¹, M. W. Rashid¹, T. M. Carpenter², C. Tekes¹, D. M. J. Cowell², S. Freear², F. L. Degertekin¹, M. Ghovanloo¹

¹Georgia Institute of Technology, Atlanta, GA; ²University of Leeds, Leeds, United Kingdom

11:15 AM

10.7 A 0.3ppm Dual-Resonance Transformer-Based Drift-Cancelling Reference-Free Magnetic Sensor for Biosensing Applications

C. Sideris, P. Porsandeh Khial, B. Ling, A. Hajimiri

California Institute of Technology, Pasadena, CA

11:45 AM

10.8 A 100mK-NETD 100ms-Startup-Time 80×60 Micro-Bolometer CMOS Thermal Imager Integrated with a 0.234mm² 1.89μV_{rms} Noise 12b Biasing DAC

K-D. Kim¹, S. Park¹, K-S. Yoon¹, G-G. Kang¹, H-K. Han¹, J-S. Choi¹, M-W. Ko¹, J-H. Cho¹, S. Lim¹, H-M. Lee², H-S. Kim³, K. Lee¹, G-H. Cho¹

¹KAIST, Daejeon, Korea; ²Korea University, Seoul, Korea; ³Dankook University, Cheonan, Korea

Conclusion 12:15 PM

SRAM**Session Chair:** *Jonathan Chang*, TSMC, Hsinchu, Taiwan**Associate Chair:** *Chun Shiah*, Etron, Hsinchu, Taiwan**8:30 AM****11.1 A 23.6Mb/mm² SRAM in 10nm FinFET Technology with Pulsed PMOS TVC and Stepped-WL for Low-Voltage Applications***Z. Guo, D. Kim, S. Nalam, J. Wiedemer, X. Wang, E. Karl*

Intel, Hillsboro, OR

9:00 AM**11.2 A 7nm FinFET SRAM Using EUV Lithography with Dual Write-Driver-Assist Circuitry for Low-Voltage Applications***T. Song, J. Jung, W. Rim, H. Kim, Y. Kim, C. Park, J. Do, S. Park, S. Cho, H. Jung, B. Kwon, H-S. Choi, J. Choi, J. S. Yoon*

Samsung Electronics, Hwaseong, Korea

9:30 AM**11.3 A 5GHz 7nm L1 Cache Memory Compiler for High-Speed Computing and Mobile Applications***M. Clinton¹, R. Singh¹, M. Tsai¹, S. Zhang¹, B. Sheffield¹, J. Chang²*¹TSMC, Austin, TX²TSMC, Hsinchu, Taiwan**Break 10:00 AM**

DRAM

Session Chair: *Seung-Jun Bae, Samsung, Hwasung, Korea*

Associate Chair: *Wolfgang Spirkel, Micron Semiconductor, Munich, Germany*

10:15 AM

12.1 A 16Gb 18Gb/s/pin GDDR6 DRAM with Per-Bit Trainable Single-Ended DFE and PLL-Less Clocking

Y-J. Kim, H-J. Kwon, S-Y. Doo, Y-J. Eom, Y-S. Kim, M-S. Ahn, Y-H. Kim, S-H. Jung, S-G. Do, C-Y. Lee, J-S. Kim, D-S. Kang, K-B. Park, J-B. Shin, J-H. Lee, S-H. Oh, S-Y. Lee, J-H. Yu, J-S. Kwon, K-H. Yu, C-H. Jeon, S-S. Kim, M-W. Won, G-H. Cho, H-S. Park, H-K. Kim, J-W. Lee, S-H. Cho, K-W. Park, J-K. Park, Y-J. Lee, Y. Kim, Y-H. Seo, B-R. Cho, C-H. Shin, C-Y. Lee, Y. Lee, Y-G. Song, S-Y. Bang, Y. Park, S-K. Choi, B-C. Kim, G-H. Han, S-J. Bae, H-J. Kwon, J-H. Choi, Y-S. Sohn, K-I. Park, S-J. Jang

Samsung Electronics, Hwaseong, Korea

10:45 AM

12.2 A 16Gb LPDDR4X SDRAM with an NBTI-Tolerant Circuit Solution, an SWD PMOS GIDL Reduction Technique, an Adaptive Gear-Down Scheme and a Metastable-Free DQS Aligner in a 10nm Class DRAM Process

K. C. Chun, Y-G. Chu, J-S. Heo, T-S. Kim, S. Kim, H-K. Yang, M-J. Kim, C-K. Lee, J. Kim, H. Yoon, C-H. Shin, S. Cha, H-J. Kim, Y-S. Kim, K. Kim, Y-J. Kim, W. Choi, D-S. Yim, I. Moon, Y-J. Kim, J. Lee, Y. Choi, Y. Kwon, S-W. Choi, J-W. Kim, Y-S. Park, W. Kang, J. Chung, S. Kim, Y. Ryu, S-J. Cho, H. Shin, H. Jung, S. Kwon, K. Kang, J. Lee, Y. Song, Y-J. Kim, E-A. Kim, K-S. Ha, K-H. Kim, S-H. Hyun, S. Ko, J-H. Choi, Y-S. Sohn, K-I. Park, S-J. Jang

Samsung Electronics, Hwaseong, Korea

11:15 AM

12.3 A 1.2V 64Gb 341GB/s HBM2 Stacked DRAM with Spiral Point-to-Point TSV Structure and Improved Bank Group Data Control

J. H. Cho, J. Kim, W. Y. Lee, D. U. Lee, T. K. Kim, H. B. Park, C. Jeong, M-J. Park, S. G. Baek, S. Choi, B. K. Yoon, Y. J. Choi, K. Y. Lee, D. Shim, J. Oh, J. Kim, S-H. Lee

SK hynix, Gyeonggi, Korea

11:45 AM

12.4 A 16Gb/s/pin 8Gb GDDR6 DRAM with Bandwidth Extension Techniques for High-Speed Applications

K-D. Hwang, B. Kim, S-Y. Byeon, K-Y. Kim, D-H. Kwon, H-B. Lee, G-I. Lee, S-S. Yoon, J-Y. Cha, S-Y. Jang, S-H. Lee, Y-S. Joo, G-S. Lee, S-S. Xi, S-B. Lim, K-H. Chu, J-H. Cho, J. Chun, J. Oh, J. Kim, S-H. Lee

SK hynix, Gyeonggi, Korea

12:00 PM

12.5 A 16Gb 1.2V 3.2Gb/s/pin DDR4 SDRAM with Improved Power Distribution and Repair Strategy

S. Shim, S. Kim, J. Bae, K. Ko, E. Lee, K. Kim, K. Kim, S. Lee, J. Hyun, I. Koh, J. Park, M. Kim, S. Shin, D. Lee, Y. Lee, S. Hyun, W. Choi, D. Im, D. Lee, J. Jang, S. Lee, J. Chun, J. Oh, J. Kim, S-H. Lee

SK hynix, Icheon, Korea

Conclusion 12:15 PM

Machine Learning and Signal Processing

Session Chair: *Dejan Markovic*, University of California, Los Angeles, Los Angeles, CA

Associate Chair: *Masato Motomura*, Hokkaido University, Sapporo, Japan

1:30 PM

13.1 A Shift Towards Edge Machine-Learning Processing

O. Temam, Google, Paris, France

2:00 PM

13.2 QUEST: A 7.49TOPS Multi-Purpose Log-Quantized DNN Inference Engine Stacked on 96MB 3D SRAM Using Inductive-Coupling Technology in 40nm CMOS

K. Ueyoshi¹, K. Ando¹, K. Hirose¹, S. Takamaeda-Yamazaki¹, M. Nakamura², T. Adachi², J. Kadomoto³, T. Miyata³, M. Hamada³, T. Kuroda³, M. Motomura¹

¹Hokkaido University, Sapporo, Japan

²Ultra Memory, Hachioji, Japan

³Keio University, Yokohama, Japan

2:30 PM

13.3 UNPU: A 50.6TOPS/W Unified Deep Neural Network Accelerator with 1b-DS2 to-16b Fully-Variable Weight Bit-Precision

J. Lee, C. Kim, S. Kang, D. Shin, S. Kim, H-J. Yoo, KAIST, Daejeon, Korea

Break 3:00 PM

3:15 PM

13.4 A 9.02mW CNN-Stereo-Based Real-Time 3D Hand-Gesture Recognition DS2 Processor for Smart Mobile Devices

S. Choi, J. Lee, K. Lee, H-J. Yoo, KAIST, Daejeon, Korea

3:45 PM

13.5 An Always-On 3.8 μ J/86% CIFAR-10 Mixed-Signal Binary CNN Processor with All Memory on Chip in 28nm CMOS

D. Bankman¹, L. Yang¹, B. Moons², M. Verhelst², B. Murmann¹

¹Stanford University, Stanford, CA

²KU Leuven, Leuven, Belgium

4:15 PM

13.6 A 1.8Gb/s 70.6pJ/b 128 \times 16 Link-Adaptive Near-Optimal Massive MIMO Detector in 28nm UTBB-FDSOI

W. Tang¹, H. Prabhu², L. Liu², V. Öwall², Z. Zhang¹

¹University of Michigan, Ann Arbor, MI

²Lund University, Lund, Sweden

4:45 PM

13.7 A 232-to-1996KS/s Robust Compressive-Sensing Reconstruction Engine for Real-Time Physiological Signals Monitoring

T-S. Chen, H-C. Kuo, A-Y. Wu, National Taiwan University, Taipei, Taiwan

Conclusion 5:15 PM

High-Resolution ADCs

Session Chair: **Matt Straayer**, Maxim Integrated Products, Chelmsford, MA
 Associate Chair: **Seung-Tak Ryu**, KAIST, Daejeon, Korea

1:30 PM

14.1 A 50MHz-BW Continuous-Time $\Delta\Sigma$ ADC with Dynamic Error Correction Achieving 79.8dB SNDR and 95.2dB SFDR

T. He¹, M. Ashburn², S. Ho², Y. Zhang¹, G. Temes¹

¹Oregon State University, Corvallis, OR

²MediaTek, Woburn, MA

2:00 PM

14.2 A 15.2-ENOB Continuous-Time $\Delta\Sigma$ ADC for a 7.3 μ W 200mV_{pp}-Linear-Input-Range Neural Recording Front-End

H. Chandrakumar, D. Marković

University of California, Los Angeles, Los Angeles, CA

2:30 PM

14.3 A 13-ENOB 2nd-Order Noise-Shaping SAR ADC Realizing Optimized NTF Zeros Using an Error-Feedback Structure

S. Li, B. Qiao, M. Gandara, N. Sun

University of Texas, Austin, TX

Break 3:00 PM

3:15 PM

14.4 A 1.1mW 200kS/s Incremental $\Delta\Sigma$ ADC with a DR of 91.5dB Using Integrator Slicing for Dynamic Power Reduction

P. Vogelmann, M. Haas, M. Ortmanns

University of Ulm, Ulm, Germany

3:45 PM

14.5 A 280 μ W Dynamic-Zoom ADC with 120dB DR and 118dB SNDR in 1kHz BW

S. Karmakar¹, B. Gönen¹, F. Sebastiano¹, R. Van Veldhoven², K. A. A. Makinwa¹

¹Delft University of Technology, Delft, The Netherlands

²NXP Semiconductors, Eindhoven, The Netherlands

4:15 PM

14.6 A 0.4V 13b 270kS/s SAR-ISDM ADC with an Opamp-Less Time-Domain Integrator

S-E. Hsieh, C-C. Hsieh

National Tsing Hua University, Hsinchu, Taiwan

4:45 PM

14.7 A Signal-Independent Background-Calibrating 20b 1MS/s SAR ADC with **DS2** 0.3ppm INL

H. Li¹, M. Maddox¹, M. C. W. Coln¹, W. Buckley², D. Hummerston³, N. Naeem¹

¹Analog Devices, Wilmington, MA

²Analog Devices, Cork, Ireland

³Analog Devices, Newbury, United Kingdom

Conclusion 5:15 PM

RF PLLs

Session Chair: *Jiayoon Ru*, Broadcom, Irvine, CA

Associate Chair: *Jaehyook Choi*, Ulsan National Institute of Science Technology, Ulsan, Korea

1:30 PM

15.1 A 0.98mW Fractional-N ADPLL Using 10b Isolated Constant-Slope DTC with FOM of -246dB for IoT Applications in 65nm CMOS

H. Liu, D. Tang, Z. Sun, W. Deng, H. C. Ngo, K. Okada, A. Matsuzawa
Tokyo Institute of Technology, Tokyo, Japan

2:00 PM

15.2 A 23GHz Low-Phase-Noise Digital Bang-Bang PLL for Fast Triangular and Saw-Tooth Chirp Modulation

D. Cherniak^{1,2}, L. Grimaldi², L. Bertulessi², C. Samori², R. Nonis¹, S. Levantino²
¹Infineon Technologies, Villach, Austria; ²Politecnico di Milano, Milan, Italy

2:30 PM

15.3 A 36.3-to-38.2GHz -216dBc/Hz² 40nm CMOS Fractional-N FMCW Chirp Synthesizer PLL with a Continuous-Time Bandpass Delta-Sigma Time-to-Digital Converter

D. Weyer¹, M. B. Dayanik², S. Jang¹, M. P. Flynn¹
¹University of Michigan, Ann Arbor, MI; ²Broadcom, Irvine, CA

Break 3:00 PM

3:15 PM

15.4 A Low-Phase-Noise Digital Bang-Bang PLL with Fast Lock Over a Wide Lock Range

L. Bertulessi, L. Grimaldi, D. Cherniak, C. Samori, S. Levantino
Politecnico di Milano, Milan, Italy

3:45 PM

15.5 A Digital Frequency Synthesizer with Dither-Assisted Pulling Mitigation for Simultaneous DCO and Reference Path Coupling

C-R. Ho, M-W. Chen, University of Southern California, Los Angeles, CA

4:15 PM

15.6 A 0.01mm² 4.6-to-5.6GHz Sub-Sampling Type-I Frequency Synthesizer with -254dB FOM

A. Sharkia, S. Mirabbasi, S. Shekhar, University of British Columbia, Vancouver, Canada

4:30 PM

15.7 A Dividerless Reference-Sampling RF PLL with -253.5dB Jitter FOM and <-67dBc Reference Spurs

J. Sharma, H. Krishnaswamy, Columbia University, New York, NY

4:45 PM

15.8 An 82-to-108GHz -181dB-FOM_T ADPLL Employing a DCO with Split-Transformer and Dual-Path Switched-Capacitor Ladder and a Clock-Skew-Sampling Delta-Sigma TDC

Z. Huang, H. C. Luong, HKUST, Hong Kong, China

Conclusion 5:15 PM

Advanced Optical and Wireline Techniques

Session Chair: **Azita Emami**, California Institute of Technology, Pasadena, CA

Associate Chair: **Andrew Joy**, Cavium, Northampton, United Kingdom

1:30 PM

16.1 Optical Interconnects in Computing and Switching Systems: the Anatomy of a 20Tb/s Switch Card

A. Krishnamoorthy, Axalume, San Diego, CA

2:00 PM

16.2 A 28Gb/s Transceiver with Chirp-Managed EDC for DML Systems

K. Kwon, J. Yoon, H. Choi, Y. Jeon, J. Yang, B. Kim, S. Kwon, M. Kim, S. Jeon, H. Won, H-M. Bae
KAIST, Daejeon, Korea

2:30 PM

16.3 A 56Gb/s Burst-Mode NRZ Optical Receiver with 6.8ns Power-On and CDR-Lock Time for Adaptive Optical Links in 14nm FinFET CMOS

I. Ozkaya^{1,2}, A. Cevrero¹, P. A. Francese¹, C. Menolfi¹, M. Braendli¹, T. Morfi¹, D. Kuchta³, L. Kull¹, M. Kossel¹, D. Luu¹, M. Meghelli³, Y. Leblebic², T. Toiff¹

¹IBM Research, Ruschlikon, Switzerland; ²EPFL, Lausanne, Switzerland

³IBM Research, Yorktown Heights, NY

2:45 PM

16.4 A 0.5-to-0.9V, 3-to-16Gb/s, 1.6-to-3.1pJ/b Wireline Transceiver Equalizing 27dB Loss at 10Gb/s with Clock-Domain Encoding Using Integrated Pulse-Width Modulation (iPWM) in 65nm CMOS

A. Ramachandran, T. Anand, Oregon State University, Corvallis, OR

Break 3:00 PM

3:15 PM

16.5 A 20Gb/s Transceiver with Framed-Pulsewidth Modulation in 40nm CMOS

S. Jeon¹, W. Kwon¹, T. Yoon², J-H. Yoon¹, K. Kwon¹, J. Yang¹, H-M. Bae¹

¹KAIST, Daejeon, Korea; ²Samsung Electronics, Hwaseong, Korea

3:45 PM

16.6 A 7.8Gb/s/pin 1.96pJ/b Compact Single-Ended TRX and CDR with Phase-Difference Modulation for Highly Reflective Memory Interfaces

S. Lee, J. Seo, K. Lim, J. Ko, J-Y. Sim, H-J. Park, B. Kim

Pohang University of Science and Technology, Pohang, Korea

4:15 PM

16.7 A 126mW 56Gb/s NRZ Wireline Transceiver for Synchronous Short-Reach Applications in 16nm FinFET

M. Erett¹, D. Carey¹, J. Hudner¹, R. Casey¹, K. Geary¹, P. Neto¹, M. Raj², S. McLeod³, H. Zhang², A. Roldan², H. Zhao⁴, P-C. Chiang⁴, H. Zhao⁴, K. Tari⁴, Y. Frans², K. Chang²

¹Xilinx, Cork, Ireland; ²Xilinx, San Jose, CA; ³Acacia Communications, San Jose, CA

⁴Xilinx, Singapore

4:45 PM

16.8 A 1.17pJ/b 25Gb/s/pin Ground-Referenced Single-Ended Serial Link for **DS2** Off- and On-Package Communication in 16nm CMOS Using a Process- and Temperature-Adaptive Voltage Regulator

J. M. Wilson¹, W. J. Turner¹, J. W. Poulton¹, B. Zimmer², X. Chen², S. S. Kudva², S. Song², S. G. Tell¹, N. Nedovic², W. Zhao^{1,4}, S. R. Sudhakaran², C. T. Gray¹, W. J. Dally²

¹Nvidia, Durham, NC; ²Nvidia, Santa Clara, CA; ³Broadcom, Irvine, CA

⁴now with Broadcom, Irvine, CA

5:00 PM

16.9 A 20Gb/s 79.5mW 127GHz CMOS Transceiver with Digitally Pre-Distorted PAM-4 Modulation for Contactless Communications

Y. Kim^{1,2}, B. Hu², Y. Du², A. Tang^{1,2}, H-N. Chen³, C. Jou³, J. Cong², T. Itoh², M-C. F. Chang^{2,4}

¹Jet Propulsion Laboratory, Pasadena, CA; ²University of California, Los Angeles, Los Angeles, CA

³TSMC, Hsinchu, Taiwan; ⁴National Chiao Tung University, Hsinchu, Taiwan

Conclusion 5:15 PM

Technologies for Health and Society

Session Chair: *Patrick Mercier*, University of California, San Diego, La Jolla, CA
 Associate Chair: *Long Yan*, Samsung Electronics, Hwaseongsi, Korea

1:30 PM

17.1 Food and Agriculture Cloud Services with Sensor Networks

K. Watanabe¹, R. Sakuma²

¹Fujitsu Kyushu System Services, Fukuoka, Japan; ²Fujitsu America, Sunnyvale, CA

2:00 PM

17.2 4-Camera VGA-Resolution Capsule Endoscope with 80Mb/s Body-Channel Communication Transceiver and Sub-cm Range Capsule Localization

J. Jang¹, J. Lee¹, K-R. Lee¹, J. Lee¹, M. Kim¹, Y. Lee¹, J. Bae², H-J. Yoo¹

¹KAIST, Daejeon, Korea; ²Kangwon National University, Chuncheon, Korea

2:30 PM

17.3 A 0.3V Biofuel-Cell-Powered Glucose/Lactate Biosensing System Employing a 180nW 64dB SNR Passive $\Delta\Sigma$ ADC and a 920MHz Wireless Transmitter

A. Fazli Yeknami, X. Wang, S. Imani, A. Nikoofard, I. Jeerapan, J. Wang, P. P. Mercier

University of California, San Diego, La Jolla, CA

Break 3:00 PM

3:15 PM

17.4 A 0.28m Ω -Sensitivity 105dB-Dynamic-Range Electrochemical Impedance Spectroscopy SoC for Electrochemical Gas Detection

G. Qu¹, H. Wang¹, Y. Zhao¹, J. O'Donnell², C. Lyden³, Y. Liu¹, J. Ding⁴, D. Dempsey², L. Chen¹, D. Bourke², S. Gu¹, J. Gao¹, L. Lu¹, L. Wang¹, X. Li¹, H. Li¹, C. Chu¹, L. Yang¹

¹Analog Devices, Beijing, China; ²Analog Devices, Limerick, Ireland

³Analog Devices, Cork, Ireland; ⁴Analog Devices, Shanghai, China

⁵Analog Devices, Wilmington, MA

3:45 PM

17.5 50nW 5kHz-BW Opamp-Less $\Delta\Sigma$ Impedance Analyzer for Brain Neurochemistry Monitoring

M. El Ansary¹, N. Soltani¹, H. Kassiri¹, R. Machado¹, S. Dufou^{1,2}, P. L. Carlen^{1,2}, M. Thompson¹, R. Genov¹

¹University of Toronto, Toronto, Canada; ²Toronto Western Hospital, Toronto, Canada

4:00 PM

17.6 A 200Mb/s Inductively Coupled Wireless Transcranial Transceiver **DS2** Achieving 5e-11 BER and 1.5pJ/b Transmit Energy Efficiency

W. Li¹, Y. Duan², J. M. Rabaey¹, University of California, Berkeley, CA; ²Inphi, Santa Clara, CA

4:15 PM

17.7 A 330 $\mu\text{m}\times 90\mu\text{m}$ Opto-Electronically Integrated Wireless System-on-Chip **DS2** for Recording of Neural Activities

S. Lee, A. J. Cortese, P. Trexel, E. R. Agger, P. L. McEuen, A. C. Molnar

Cornell University, Ithaca, NY

4:30 PM

17.8 A 665 μW Silicon Photomultiplier-Based NIRS/EEG/EIT Monitoring ASIC for Wearable Functional Brain Imaging

J. Xu¹, M. Konijnenburg¹, B. Lukita¹, S. Song², H. Ha¹, R. van Wegberg¹, E. Sheikhi¹, M. Mazzillo³, G. Fallica³, W. De Raedt⁴, C. Van Hoof^{2,4}, N. Van Helleputte²

¹imec - Holst Centre, Eindhoven, The Netherlands; ²imec, Leuven, Belgium

³STMicroelectronics, Catania, Italy; ⁴KU Leuven, Leuven, Belgium

4:45 PM

17.9 A Recursive-Memory Brain-State Classifier with 32-Channel Track-and-Zoom $\Delta^2\Sigma$ ADCs and Charge-Balanced Programmable Waveform Neurostimulators

G. O'Leary¹, M. R. Pazhouhandeh¹, M. Chang¹, D. Groppe², T. A. Valiante³, N. Verma⁴, R. Genov¹

¹University of Toronto, Toronto, Canada; ²Krembil Neuroscience Center, Toronto, Canada

³Toronto Western Hospital, Toronto, Canada; ⁴Princeton University, Princeton, NJ

Conclusion 5:15 PM

Demonstration Session 2, Tuesday, February 13th, 5:00-7:00 PM

This year, the Demonstration Session extending in selected regular papers, both Academic and Industrial, will take place on Monday February 12th, and Tuesday February 13th, from 5 pm until 7 pm in the Golden Gate Hall. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2018, as noted by the symbol **DS2**

- 10.2 **Personal Inertial Navigation System Employing MEMS Wearable Ground Reaction Sensor Array and Interface ASIC Achieving a Position Accuracy of 5.5m Over 3km Walking Distance Without GPS**
- 10.3 **Multi-Way Interactive Capacitive Touch System with Palm Rejection of Active Stylus for 86" Touch Screen Panels**
- 13.3 **UNPU: A 50.6TOPS/W Unified Deep Neural Network Accelerator with 1b-to-16b Fully-Variable Weight Bit-Precision**
- 13.4 **A 9.02mW CNN-Stereo-Based Real-Time 3D Hand-Gesture Recognition Processor for Smart Mobile Devices**
- 14.7 **A Signal-Independent Background-Calibrating 20b 1MS/s SAR ADC with 0.3ppm INL**
- 16.8 **A 1.17pJ/b 25Gb/s/pin Ground-Referenced Single-Ended Serial Link for Off- and On-Package Communication in 16nm CMOS Using a Process- and Temperature-Adaptive Voltage Regulator**
- 17.6 **A 200Mb/s Inductively Coupled Wireless Transcranial Transceiver Achieving 5e-11 BER and 1.5pJ/b Transmit Energy Efficiency**
- 17.7 **A 330 μ m \times 90 μ m Opto-Electronically Integrated Wireless System-on-Chip for Recording of Neural Activities**
- 18.1 **Droop Mitigation using Critical-Path Sensors and an On-Chip Distributed Power Supply Estimation Engine in the z14TM Enterprise Processor**
- 19.6 **A 2.5nJ Duty-Cycled Bridge-to-Digital Converter Integrated in a 13mm³ Pressure-Sensing System**
- 19.7 **A 21.8b Sub-100 μ Hz 1/f Corner 2.4 μ V-Offset Programmable-Gain Read-Out IC for Bridge Measurement Systems**
- 20.2 **A Flash Memory Controller for 15 μ s Ultra-Low-Latency SSD Using High-Speed 3D NAND Flash with 3 μ s Read Time**
- 21.1 **Mixed-Signal Programmable Non-Linear Interface for Resource-Efficient Multi-Sensor Analytics**
- 21.4 **A 10Gb/s Si-Photonic Transceiver with 150 μ W 120 μ s-Lock-Time Digitally Supervised Analog Microring Wavelength Stabilization for 1Tb/s/mm² Die-to-Die Optical Networks**
- 21.5 **A 286F²/Cell Distributed Bulk-Current Sensor and Secure Flush Code Eraser Against Laser Fault Injection Attack**
- 26.1 **A 0.55-to-0.9GHz 2.7dB NF Full-Duplex Hybrid-Coupler Circulator with 56MHz 40dB TX SI Suppression**
- 26.10 **A 128-pixel 0.56THz Sensing Array for Real-Time Near-Field Imaging in 0.13 μ m SiGe BiCMOS**
- 28.3 **A 0.8V 0.8mm² Bluetooth 5/BLE Digital-Intensive Transceiver with a 2.3mW Phase-Tracking RX Utilizing a Hybrid Loop Filter for Interference Resilience in 40nm CMOS**
- 28.7 **A 14.5mm² 8nW -59.7dBm-Sensitivity Ultrasonic Wake-Up Receiver for Power-, Area-, and Interference-Constrained Applications**
- 28.8 **A 5.8GHz Power-Harvesting 116 μ m \times 116 μ m "Dielet" Near-Field Radio with On-Chip Coil Antenna**
- 29.4 **A 0.13 μ m CMOS SoC for Simultaneous Multichannel Optogenetics and Electrophysiological Brain Recording**
- 29.5 **A mm-Sized Free-Floating Wirelessly Powered Implantable Optical Stimulating System-on-a-Chip**
- 29.6 **A 92dB Dynamic Range Sub- μ V_{rms}-Noise 0.8 μ W/ch Neural-Recording ADC Array with Predictive Digital Autoranging**
- 29.7 **A 110dB-CMRR 100dB-PSRR Multi-Channel Neural-Recording Amplifier System Using Differentially Regulated Rejection Ratio Enhancement in 0.18 μ m CMOS**
- 31.1 **Conv-RAM: An Energy-Efficient SRAM with Embedded Convolution Computation for Low-Power CNN-Based Machine Learning Applications**
- 31.2 **A 42pJ/Decision 3.12TOPS/W Robust In-Memory Machine Learning Classifier with On-Chip Training**
- 31.3 **Brain-Inspired Computing Exploiting Carbon Nanotube FETs and Resistive RAM: Hyperdimensional Computing Case Study**

ISSCC 2018 • SUNDAY FEBRUARY 11TH

Tutorials

8:30 AM	T1: Low-Jitter PLLs for Wireless Transceivers	T2: Nonvolatile Circuits for Memory, Logic, and Artificial Intelligence	T3: Basics of Quantum Computing
10:30 AM	T4: Error-Correcting Codes in 5G/NVM Applications	T5: Hybrid Design of Analog-to-Digital Converters	T6: Single-Photon Detection in CMOS
1:30 PM	T7: Basics of Adaptive and Resilient Circuits	T8: Fundamentals of Switched-Mode Power Converter Design	
3:30 PM	T9: Digital RF Transmitters	T10: ADC-Based Serial Links: Design and Analysis	

Forums

8:00 AM	F1: Intelligent Energy-Efficient Systems at the edge of IoT	F2: FinFETs & FDSOI – A Mixed-Signal Circuit Designer's Perspective
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Events Below in Bold Box are Included with your Conference Registration

Evening Events

7:30 PM	EE1: Student Research Preview: Short Presentations with Poster Session	8:00 PM	EE2: Workshop on Circuits for Social Good
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ISSCC 2018 • MONDAY FEBRUARY 12TH • PAPER SESSIONS

8:30 AM	Session 1: Plenary Session				
1:30 PM	Session 2: Processors	Session 3: Analog Techniques	Session 4: mm-Wave Radios for 5G and Beyond	Session 5: Image Sensors	Session 6: Ultra-High-Speed Wireline
12noon to 7:00 PM – Book Displays • 5:00 PM to 7:00 PM – Demonstration Session • 5:15 PM – Author Interviews • Social Hour					
Evening Events					
8:00 PM	EE3: Industry Showcase			EE4: Figures-of-Merit on Trial	

ISSCC 2018 • TUESDAY FEBRUARY 13TH • PAPER SESSIONS

8:30 AM	Session 7: Neuromorphic, Clocking and Security Circuits	Session 8: Wireless Power and Harvesting	Session 9: Wireless Transceivers and Techniques	Session 10: Sensor Systems	Session 11: SRAM
1:30 PM	Session 13: Machine Learning and Signal Processing	Session 14: High-Resolution ADCs	Session 15: RF PLLs	Session 16: Advanced Optical and Wireline Techniques	Session 17: Technologies for Health and Society
10:00 AM to 7:00 PM – Book Displays • 5:00 PM to 7:00 PM – Demonstration Session • 5:15 PM – Author Interviews • Social Hour					
Evening Events					
8:00 PM	EE5: Lessons Learned – Great Circuits That Didn't Work (Oops, If Only I Had Known!)			EE6: Can Artificial Intelligence Replace My Job? – The Dawn of a New IC Industry with AI	

ISSCC 2018 • WEDNESDAY FEBRUARY 14TH • PAPER SESSIONS

8:30 AM	Session 18: Adaptive Circuits and Digital Regulators	Session 19: Sensors and Interfaces	Session 20: Flash-Memory Solutions	Session 22: Gigahertz Data Converters	Session 24: GaN Drivers and Converters
1:30 PM	Session 26: RF Techniques for Communication and Sensing	Session 27: Power-Converter Techniques	Session 21: Extending Silicon and its Applications	Session 23: LO Generation	Session 25: Clock Generation for High-Speed Links
			Session 28: Wireless Connectivity	Session 29: Advanced Biomedical Systems	Session 30: Emerging Memories
					Session 31: Computation in Memory for Machine Learning
10:00 AM to 3:00 PM – Book Displays • 5:15 PM – Author Interviews					

ISSCC 2018 • THURSDAY FEBRUARY 15TH

8:00 AM	Short Course: Hardware Approaches to Machine Learning and Inference	F3: Circuits and Architectures for Wireless Sensing, Radar and Imaging	F4: Circuit and System Techniques for mm-wave Multi-Antenna Systems	F5: Advanced Optical Communication: From Devices, Circuits and Architectures, to Algorithms	F6: Advances in Energy Efficient Analog Design
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EE5: Lessons Learned – Great Circuits That Didn't Work – (Oops, If Only I Had Known!)

Organizers: **Phillip Restle**, *IBM T. J. Watson Research Center, Yorktown Heights, NY*
Kostas Doris, *NXP, Eindhoven, The Netherlands*
Vivek De, *Intel, Hillsboro, Oregon*
Paul Ferguson, *Analog Devices, Wilmington, MA*

Moderator: **Tom Lee**, *Stanford University, Stanford, CA*

Working on your first (or last) IC can be exciting, stressful, rewarding, and embarrassing. Whatever the lesson learned, be assured that it was experienced by pioneers before you. Failures (mistakes or just bad ideas!) can be valuable learning experiences, but are rarely revealed. Tonight, we provide an opportunity for recognized experts to share their past mistakes and failures, and disclose lessons learned. After the panelists have confessed, the audience can also contribute "learning experiences" (in less than a minute). Inevitably, this collection of revelations will be motivating: inspiring to the young and inexperienced; and virtuous for gurus in sharing a universal truth – first-time perfection is rare!

Panelists

Bram Nauta, *University of Twente, Enschede, The Netherlands*
Nicky Lu, *Etron Technology, Hsinchu, Taiwan*
Shanthi Pavan, *Institute of Technology, Madras, Chennai, India*
David J. Allstot, *University of California, Berkeley, CA*
Barrie Gilbert, *Analog Devices NW Labs, Beaverton, OR*
Jon Strange, *MediaTek Wireless, West Malling, United Kingdom*

EE6: Can Artificial Intelligence Replace My Job? The Dawn of a New IC Industry with AI

Organizers: **Jaeha Kim**, *Seoul National University, Seoul, Korea*
Ki-Tae Park, *Samsung Electronics, Gyeonggi-do, Korea*

Moderator: **Paul D. Franzon**, *North Carolina State University, Raleigh, NC*

The emergence of artificial intelligence (AI) capable of human tasks and more and better, is approaching fast. Shortly, most businesses, including the IC industry, will choose AI over humans, if AI can deliver the same results with lower risks and costs. Consequently, many questions arise for us: what will be the respective roles of AI and humans in developing ICs? How will AI shape the IC industry? What is the right career choice for young people in the field? This panel will showcase diverse experts who will share their vision on this daunting new development in our business.

Panelists

Bill Dally, *NVIDIA, Santa Clara, CA*
Georges Gielen, *Katholieke Universiteit Leuven, Leuven, Belgium*
Dario Gil, *IBM Research, Yorktown Heights, NY*
Antun Domic, *Synopsys, Mountain View, CA*
Seung Hoon Tong, *Samsung Electronics, Gyeonggi-do, Korea*
Hsien-Hsin Sean Lee, *TSMC, Hsinchu, Taiwan*

Adaptive Circuits and Digital Regulators

Session Chair: *Dennis Sylvester*, University of Michigan, Ann Arbor, MIAssociate Chair: *Koji Hirairi*, Sony LSI Design, Kanagawa, Japan

8:30 AM

18.1 Droop Mitigation using Critical-Path Sensors and an On-Chip Distributed DS2 Power Supply Estimation Engine in the z14™ Enterprise Processor*C. Vezyrtzis¹, T. Strach², P. I-J. Chuang¹, P. Lobo³, R. Rizzolo⁴, T. Webe⁵, P. Owczarczyk⁴, A. Buyuktosunoglu¹, R. Bertran¹, D. Hui⁴, S. M. Eickhoff⁴, M. Floyd⁶, G. Salem⁶, S. Carey⁴, S. G. Tsapepas⁴, P. J. Restle¹*¹IBM Research, Yorktown Heights, NY; ²IBM STG, Boeblingen, Germany³IBM STG, Bangalore, India; ⁴IBM STG, Poughkeepsie, NY; ⁵IBM STG, Austin, TX⁶IBM STG, Essex Junction, VT

9:00 AM

18.2 A Combined All-Digital PLL-Buck Slack Regulation System with Autonomous CCM/DCM Transition Control and 82% Average Voltage-Margin Reduction in a 0.6-to-1.0V Cortex-M0 Processor*X. Sun, S. Kim, F. U. Rahman, V. R. Pamula, X. Li, N. John, V. S. Sathe*

University of Washington, Seattle, WA

9:30 AM

18.3 A 2.5 μ W 0.0067mm² Automatic Back-Biasing Compensation Unit Achieving 50% Leakage Reduction in FDSOI 28nm over 0.35-to-1V V_{DD} Range*A. Quelen¹, G. Pillonnet¹, P. Flatresse², E. Beigné¹*¹CEA-LETI-MINATEC, Grenoble, France; ²STMicroelectronics, Crolles, France

9:45 AM

18.4 A 0.4V 430nA Quiescent Current NMOS Digital LDO with NAND-Based Analog-Assisted Loop in 28nm CMOS*X. Ma^{1,2}, Y. Lu¹, R. P. Martins^{1,3}, Q. Li²*, ¹University of Macau, Macau, China²University of Electronic Science and Technology of China, Chengdu, China³Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

Break 10:00 AM

10:15 AM

18.5 A Fully Integrated 40pF Output Capacitor Beat-Frequency-Quantizer-Based Digital LDO with Built-In Adaptive Sampling and Active Voltage Positioning*S. Kundu¹, M. Liu¹, R. Wong², S-J. Wen², C. H. Kim¹*¹University of Minnesota, Minneapolis, MN; ²Cisco Systems, San Jose, CA

10:45 AM

18.6 A 500mA Analog-Assisted Digital-LDO-Based On-Chip Distributed Power Delivery Grid with Cooperative Regulation and IR-Drop Reduction in 65nm CMOS*Y. Lu¹, F. Yang², F. Chen¹, P. K. T. Mok¹*, ¹HKUST, Hong Kong, China; ²Qualcomm, Singapore

11:15 AM

18.7 A Sub-1.55mV-Accuracy 36.9ps-FOM Digital-Low-Dropout Regulator Employing Switched-Capacitor Resistance*L. G. Salem, P. P. Mercier*, University of California, San Diego, La Jolla, CA

11:45 AM

18.8 A High-Efficiency and Fast-Transient Digital-Low-Dropout Regulator with the Burst Mode Corresponding to the Power-Saving Modes of DC-DC Switching Converters*J-H. Lin¹, Y-S. Ma¹, C-M. Huang¹, L-C. Lin¹, C-H. Cheng¹, K-H. Chen¹, Y-H. Lin², S-R. Lin², T-Y. Tsa²*¹National Chiao Tung University, Hsinchu, Taiwan; ²Realtek Semiconductor, Hsinchu, Taiwan

Conclusion 12:15 PM

Sensors and Interfaces

Session Chair: *Man-Kay Law*, University of Macau, Macau, China
 Associate Chair: *Taeik Kim*, Samsung Electronics, Hwaseong, Korea

8:30 AM

19.1 An 8b Subthreshold Hybrid Thermal Sensor with $\pm 1.07^\circ\text{C}$ Inaccuracy and Single-Element Remote-Sensing Technique in 22nm FinFET

C-Y. Lu¹, S. Ravikumar¹, A. D. Sali¹, M. Eberlein², H-J. Lee¹

¹Intel, Hillsboro, OR; ²Intel, Neubiberg, Germany

9:00 AM

19.2 A 0.25mm² Resistor-Based Temperature Sensor with an Inaccuracy of 0.12°C (3 σ) from -55°C to 125°C and a Resolution FOM of 32fJ-K²

S. Pan, K. A. A. Makinwa, Delft University of Technology, Delft, The Netherlands

9:30 AM

19.3 A 0.53pJ-K² 7000 μm^2 Resistor-Based Temperature Sensor with an Inaccuracy of $\pm 0.35^\circ\text{C}$ (3 σ) in 65nm CMOS

W. Choi¹, Y-T. Lee¹, S. Kim², S. Lee², J. Jang², J. Chun², K. A. A. Makinwa³, Y. Chae¹

¹Yonsei University, Seoul, Korea; ²SK hynix, Icheon, Korea

³Delft University of Technology, Delft, The Netherlands

Break 10:00 AM

10:15 AM

19.4 A $\pm 4\text{A}$ High-Side Current Sensor with 25V Input CM Range and 0.9% Gain Error from -40°C to 85°C Using an Analog Temperature Compensation Technique

L. Xu, J. H. Huijsing, K. A. A. Makinwa, Delft University of Technology, Delft, The Netherlands

10:45 AM

19.5 A Current-Measurement Front-End with 160dB Dynamic Range and 7ppm INL

C-L. Hsu, D. A. Hall, University of California, San Diego, La Jolla, CA

11:15 AM

19.6 A 2.5nJ Duty-Cycled Bridge-to-Digital Converter Integrated in a 13mm³ DS2 Pressure-Sensing System

S. Oh¹, Y. Shi¹, G. Kim^{1,2}, Y. Kim^{1,2}, T. Kang¹, S. Jeong^{1,2}, D. Sylvester¹, D. Blaauw¹

¹University of Michigan, Ann Arbor, MI; ²CubeWorks, Ann Arbor, MI

11:45 AM

19.7 A 21.8b Sub-100 μHz 1/f Corner 2.4 μV -Offset Programmable-Gain Read-DS2 Out IC for Bridge Measurement Systems

J. Jun, C. Rhee, M. Kim, J. Kang, S. Kim, Seoul National University, Seoul, Korea

12:00 PM

19.8 A Phase-Domain Readout Circuit for a CMOS-Compatible Thermal-Conductivity-Based Carbon Dioxide Sensor

Z. Cai^{1,2}, R. van Veldhoven², H. Suy³, G. de Graaf¹, K. A. A. Makinwa¹, M. Pertijs¹

¹Delft University of Technology, Delft, The Netherlands

²NXP Semiconductors, Eindhoven, The Netherlands

³ams AG, Eindhoven, The Netherlands

Conclusion 12:15 PM

Flash-Memory Solutions

Session Chair: *Ki-Tae Park*, Samsung, Hwaseong, KoreaAssociate Chair: *Yan Li*, Western Digital, Milpitas, CA

8:30 AM

20.1 A 512Gb 3b/Cell 3D Flash Memory on a 96-Word-Line-Layer Technology

H. Maejima¹, K. Kanda¹, S. Fujimura¹, T. Takagiwa¹, S. Ozawa¹, J. Sato¹, Y. Shindo¹, M. Sato¹, N. Kanagawa¹, J. Musha¹, S. Inoue¹, K. Sakurai¹, N. Morozumi¹, R. Fukuda¹, Y. Shimizu¹, T. Hashimoto¹, X. Li¹, Y. Shimizu¹, K. Abe¹, T. Yasufuku¹, T. Minamoto¹, H. Yoshihara¹, T. Yamashita¹, K. Satou², T. Sugimoto¹, F. Kono¹, M. Abe¹, T. Hashiguchi¹, M. Kojima¹, Y. Suematsu², T. Shimizu¹, A. Imamoto¹, N. Kobayashi¹, M. Miakashi¹, K. Yamaguchi¹, S. Bushnaq¹, H. Haibi¹, M. Ogawa¹, Y. Ochi¹, K. Kubota², T. Waku², D. He¹, W. Wang¹, H. Minagawa¹, T. Nishiuchi¹, H. Nguyen³, K-H. Kim³, K. Cheah³, Y. Koh³, F. Lu³, V. Ramachandra³, S. Rajendra³, S. Choi³, K. Payak³, N. Raghunathan³, S. Georgakis³, H. Sugawara³, S. Lee³, T. Futatsuyama¹, K. Hosono¹, N. Shibata¹, T. Hisada¹, T. Kaneko¹, H. Nakamura¹

¹Toshiba Memory, Yokohama, Japan²Toshiba Memory Systems, Yokohama, Japan³SanDisk, Milpitas, CA

9:00 AM

20.2 A Flash Memory Controller for 15 μ s Ultra-Low-Latency SSD Using High-DS2 Speed 3D NAND Flash with 3 μ s Read Time

W. Cheong, C. Yoon, S. Woo, K. Han, D. Kim, C. Lee, Y. Choi, S. Kim, D. Kang, G. Yu, J. Kim, J. Park, K-W. Song, K-T. Park, S. Cho, H. Oh, D. D. Lee, J-H. Choi, J. Jeong

Samsung Electronics, Hwaseong, Korea

9:30 AM

20.3 A 1Tb 4b/Cell 64-Stacked-WL 3D NAND Flash Memory with 12MB/s Program Throughput

S. Lee, C. Kim, M. Kim, S-M. Joe, J. Jang, S. Kim, K. Lee, J. Kim, J. Park, H-J. Lee, M. Kim, S. Lee, S. Lee, J. Bang, D. Shin, H. Jang, D. Lee, N. Kim, J. Jo, J. Park, S. Park, Y. Rho, Y. Park, H-J. Kim, C. A. Lee, C. Yu, Y. Min, M. Kim, K. Kim, S. Moon, H. Kim, Y. Choi, Y. Ryu, J. Choi, M. Lee, J. Kim, G. S. Choo, J-D. Lim,

D-S. Byeon, K. Song, K-T. Park, K-H. Kyung

Samsung Electronics, Hwaseong, Korea

Break 10:00 AM

Extending Silicon and its ApplicationsSession Chair: *Jan Genoe*, IMEC, Leuven, BelgiumAssociate Chair: *Frederic Giancesello*, STMicroelectronics, Crolles, France

10:15 AM

21.1 Mixed-Signal Programmable Non-Linear Interface for Resource-Efficient DS2 Multi-Sensor Analytics*K. Badami, J-C. Pena Ramos, S. Lauwereins, M. Verhelst*
KU Leuven, Leuven, Belgium

10:45 AM

21.2 A 1 μ W Voice Activity Detector Using Analog Feature Extraction and Digital Deep Neural Network*M. Yang, C-H. Yeh, Y. Zhou, J. P. Cerqueira, A. A. Lazar, M. Seok*
Columbia University, New York, NY

11:00 AM

21.3 32GHz Resonant-Fin Transistors in 14nm FinFET Technology*B. Bahr¹, Y. He², Z. Krivokapic³, S. Banna³, D. Weinstein²*¹Massachusetts Institute of Technology, now at Kilby Labs - Texas Instruments, Dallas, TX²Purdue University, West Lafayette, IN³GLOBALFOUNDRIES, Santa Clara, CA

11:15 AM

21.4 A 10Gb/s Si-Photonic Transceiver with 150 μ W 120 μ s-Lock-Time Digitally DS2 Supervised Analog Microring Wavelength Stabilization for 1Tb/s/mm² Die-to-Die Optical Networks*Y. Thonnart¹, M. Zid¹, J. L. Gonzalez-Jimenez¹, G. Waltener¹, R. Polster¹, O. Dubray¹, F. Lepin¹, S. Bernabé¹, S. Menez¹, G. Parès¹, O. Castany¹, L. Boutafa¹, P. Grosse¹, B. Charbonnier¹, C. Baudo²*¹CEA-LETI-MINATEC, Grenoble, France²STMicroelectronics, Crolles, France

11:45 AM

21.5 A 286F²/Cell Distributed Bulk-Current Sensor and Secure Flush Code DS2 Eraser Against Laser Fault Injection Attack*K. Matsuda¹, T. Fujii², N. Shoji², T. Sugawara², K. Sakiyama², Y-I. Hayashi³, M. Nagata¹, N. Miura¹*¹Kobe University, Kobe, Japan²University of Electro-Communication, Chofu, Japan³Nara Advanced Institute of Science and Technology, Ikoma, Japan

12:00 PM

21.6 An 8-Channel 13GHz ESR-on-a-Chip Injection-locked VCO-array achieving 200 μ M-Concentration Sensitivity*A. Chu^{1,3}, B. Schlecker^{1,3}, K. Lips², M. Ortmanns¹, J. Anders^{1,3}*¹University of Ulm, Ulm, Germany²Helmholtz-Zentrum Berlin für Materialien und Energie, Berlin, Germany³University of Stuttgart, Stuttgart, Germany

Conclusion 12:15 PM

Gigahertz Data Converters

Session Chair: *Kostas Doris*, NXP, Eindhoven, The Netherlands
Associate Chair: *Jan Westra*, Broadcom, Bunnik, The Netherlands

8:30 AM

22.1 A 24-to-72GS/s 8b Time-Interleaved SAR ADC with 2.0-to-3.3pJ/conversion and >30dB SNDR at Nyquist in 14nm CMOS FinFET

L. Kull¹, D. Luu^{1,2}, C. Menolfi¹, M. Braendli¹, P. A. Francese¹, T. Morf¹, M. Kossel¹, A. Cevrero¹, I. Ozkaya^{1,3}, T. Toifl¹

¹IBM Zurich Research Laboratory, Rueschlikon, Switzerland

²ETH Zurich, Zurich, Switzerland

³EPFL, Lausanne, Switzerland

9:00 AM

22.2 A 16b 6GS/s Nyquist DAC with IMD <-90dBc up to 1.9GHz in 16nm CMOS

C-H. Lin, K. L. J. Wong, T-Y. Kim, G. R. Xie, D. Major, G. Unruh, S. R. Dommaraju, H. Eberhart, A. Venes

Broadcom, Irvine, CA

9:30 AM

22.3 A 16b 12GS/s Single/Dual-Rate DAC with Successive Bandpass Delta-Sigma Modulator Achieving <-67dBc IM3 Within DC-to-6GHz Tunable Passbands

S. Su, M. S-W. Chen

University of Southern California, Los Angeles, CA

Break 10:00 AM

LO Generation

Session Chair: *Hyunchol Shin*, Kwangwoon University, Seoul, Korea

Associate Chair: *Andrea Bevilacqua*, University of Padova, Padova, Italy

10:15 AM

23.1 A -31dBc Integrated-Phase-Noise 29GHz Fractional-N Frequency Synthesizer Supporting Multiple Frequency Bands for Backward-Compatible 5G Using a Frequency Doubler and Injection-Locked Frequency Multipliers

H. Yoon¹, J. Kim¹, S. Park¹, Y. Lim¹, Y. Lee¹, J. Bang¹, K. Lim², J. Choi¹

¹Ulsan National Institute of Science and Technology, Ulsan, Korea

²FCI, Seongnam, Korea

10:45 AM

23.2 A >40dB IRR, 44% Fractional-Bandwidth Ultra-Wideband mm-Wave Quadrature LO Generator for 5G Networks in 55nm CMOS

F. Piri¹, M. Bassi^{1,2}, N. Lacaïta¹, A. Mazzanti¹, F. Svelto¹

¹University of Pavia, Pavia, Italy; ²now with Infineon Technologies, Villach, Austria

11:00 AM

23.3 A 22.8-to-43.2GHz Tuning-Less Injection-Locked Frequency Tripler Using Injection-Current Boosting with 76.4% Locking Range for Multiband 5G Applications

J. Zhang, H. Liu, C. Zhao, K. Kang

University of Electronic Science and Technology of China, Chengdu, China

11:15 AM

23.4 A 301.7-to-331.8GHz Source with Entirely On-Chip Feedback Loop for Frequency Stabilization in 0.13 μ m BiCMOS

C. Jiang^{1,2}, M. Aseeri³, A. Cathelin⁴, E. Afshari^{1,2}

¹University of Michigan, Ann Arbor, MI; ²Cornell University, Ithaca, NY

³King Abdulaziz City for Science and Technology, Riyadh, Saudi Arabia

⁴STMicroelectronics, Crolles, France

11:30 AM

23.5 An Inverse-Class-F CMOS VCO with Intrinsic-High-Q 1st- and 2nd-Harmonic Resonances for 1/f²-to-1/f³ Phase-Noise Suppression Achieving 196.2dBc/Hz FOM

C-C. Lim^{1,2}, J. Yin¹, P-I. Mak¹, H. Ramiah², R. P. Martins^{1,3}

¹University of Macau, Macau, China; ²University of Malaya, Kuala Lumpur, Malaysia

³Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

11:45 AM

23.6 A Quad-Core 15GHz BiCMOS VCO with -124dBc/Hz Phase Noise at 1MHz Offset, -189dBc/Hz FOM, and Robust to Multimode Concurrent Oscillations

F. Padovan¹, F. Quadrelli^{1,2}, M. Bassi¹, M. Tiebout¹, A. Bevilacqua²

¹Infineon Technologies, Villach, Austria; ²University of Padova, Padova, Italy

12:00 PM

23.7 A 7.4-to-14GHz PLL with 54fs_{rms} Jitter in 16nm FinFET for Integrated RF-Data-Converter SoCs

D. Turker¹, A. Bekele¹, P. Upadhyaya¹, B. Verbruggen², Y. Cao¹, S. Ma¹, C. Erdmann²,

B. Farley², Y. Frans¹, K. Chang¹, ¹Xilinx, San Jose, CA; ²Xilinx, Dublin, Ireland

Conclusion 12:15 PM

GaN Drivers and Converters

Session Chair: *Yogesh Ramadass*, Texas Instruments, San Jose, CA
Associate Chair: *Gerard Villar Pique*, NXP Semiconductors, Eindhoven,
The Netherlands

8:30 AM

24.1 A 2MHz 150-to-400V Input Isolated DC-DC Bus Converter with Monolithic Slope-Sensing ZVS Detection Achieving 13ns Turn-On Delay and 1.6W Power Saving*L. Cong^{1,2}, H. Lee¹*¹University of Texas at Dallas, Richardson, TX²Texas Instruments, Santa Clara, CA

9:00 AM

24.2 A Fully Integrated Three-Level 11.6nC Gate Driver Supporting GaN Gate Injection Transistors*A. Seidel¹, B. Wicht^{1,2}*¹Reutlingen University, Reutlingen, Germany²Leibniz University Hannover, Hannover, Germany

9:30 AM

24.3 A 3-to-40V V_{IN} 10-to-50MHz 12W Isolated GaN Driver with Self-Excited t_{dead} Minimizer Achieving 0.2ns/0.3ns t_{dead} , 7.9% Minimum Duty Ratio and 50V/ns CMTI*X. Ke, D. B. Ma*

University of Texas at Dallas, Richardson, TX

Break 10:00 AM

Clock Generation for High-Speed Links**Session Chair: Roberto Nonis**, Infineon, Villach, Austria**Associate Chair: Pavan Hanumolu**, University of Illinois, Urbana-Champaign, Urbana, IL

10:15 AM

25.1 A 4-to-16GHz Inverter-Based Injection-Locked Quadrature Clock Generator with Phase Interpolators for Multi-Standard I/Os in 7nm FinFET*S. Chen, L. Zhou, I. Zhuang, J. Im, D. Melek, J. Namkoong, M. Raj, J. Shin, Y. Frans, K. Chang*
Xilinx, San Jose, CA

10:45 AM

25.2 A 5GHz 370fs_{rms} 6.5mW Clock Multiplier Using a Crystal-Oscillator Frequency Quadrupler in 65nm CMOS*K. M. Megawer, A. Elkholy, D. Coombs, M. G. Ahmed, A. Elmallah, P. K. Hanumolu*
University of Illinois, Urbana, IL

11:15 AM

25.3 A Fractional-N Digital PLL with Background-Dither-Noise-Cancellation Loop Achieving <-62.5dBc Worst-Case Near-Carrier Fractional Spurs in 65nm CMOS*C-R. Ho, M-W. Chen*

University of Southern California, Los Angeles, CA

11:30 AM

25.4 A -242dB FOM and -75dBc-Reference-Spur Ring-DCO-Based All-Digital PLL Using a Fast Phase-Error Correction Technique and a Low-Power Optimal-Threshold TDC*T. Seong, Y. Lee, S. Yoo, J. Choi*

Ulsan National Institute of Science and Technology, Ulsan, Korea

Conclusion 11:45 AM

RF Techniques for Communication and SensingSession Chair: *Giuseppe Gramegna, Huawei, Golfe Juan, France*Associate Chair: *Hua Wang, Georgia Institute of Technology, Atlanta, GA*

1:30 PM

26.1 A 0.55-to-0.9GHz 2.7dB NF Full-Duplex Hybrid-Coupler Circulator with DS2 56MHz 40dB TX SI Suppression*S. Jain, A. Agrawal, M. Johnson, A. Natarajan, Oregon State University, Corvallis, OR*

2:00 PM

26.2 A 62-to-68GHz Linear 6Gb/s 64QAM CMOS Doherty Radiator with 27.5%/20.1% PAE at Peak/6dB-Back-off Output Power Leveraging High-Efficiency Multi-Feed Antenna-Based Active Load Modulation*H. T. Nguyen, T. Chi, S. Li, H. Wang, Georgia Institute of Technology, Atlanta, GA*

2:30 PM

26.3 A 69-to-79GHz CMOS Multiport PA/Radiator with +35.7dBm CW EIRP and Integrated PLL*B. Abiri, A. Hajimiri, California Institute of Technology, Pasadena, CA*

2:45 PM

26.4 A 28GHz 41%-PAE Linear CMOS Power Amplifier Using a Transformer-Based AM-PM Distortion-Correction Technique for 5G Phased Arrays*S. N. Ali¹, P. Agarwal², J. Baylon¹, S. Gopal¹, L. Renaud¹, D. Heo¹*¹Washington State University, Pullman, WA; ²MaxLinear, San Diego, CA

Break 3:00 PM

3:15 PM

26.5 A Compact Dual-Band Digital Doherty Power Amplifier Using Parallel-Combining Transformer for Cellular NB-IoT Applications*Y. Yin, L. Xiong, Y. Zhu, B. Chen, H. Min, H. Xu, Fudan University, Shanghai, China*

3:30 PM

26.6 A Continuous-Mode Harmonically Tuned 19-to-29.5GHz Ultra-Linear PA Supporting 18Gb/s at 18.4% Modulation PAE and 43.5% Peak PAE*T-W. Li, M-Y. Huang, H. Wang, Georgia Institute of Technology, Atlanta, GA*

4:00 PM

26.7 A Coupled-RTWO-Based Subharmonic Receiver Front-End for 5G E-Band Backhaul Links in 28nm Bulk CMOS*M. Vigilante, P. Reynaert, KU Leuven, Heverlee, Belgium*

4:15 PM

26.8 A 12mW 70-to-100GHz Mixer-First Receiver Front-End for mm-Wave Massive-MIMO Arrays in 28nm CMOS*L. Iotti, G. LaCaille, A. M. Niknejad, University of California, Berkeley, CA*

4:30 PM

26.9 A 13th-Order CMOS Reconfigurable RF BPF with Adjustable Transmission Zeros for SAW-Less SDR Receivers*P. Song, H. Hashemi, University of Southern California, Los Angeles, CA*

4:45 PM

26.10 A 128-pixel 0.56THz Sensing Array for Real-Time Near-Field Imaging in 0.13 μ m SiGe BiCMOS DS2*P. Hillger¹, R. Jain¹, J. Grzyb¹, L. Mavarani¹, B. Heinemann², G. Mac Grogan³, P. Mounaix⁴, T. Zimmer⁵, U. Pfeiffer¹, ¹University of Wuppertal, Wuppertal, Germany*²IHP, Frankfurt (Oder), Germany; ³Institut Bergonié, Bordeaux, France⁴CNRS, Talence, France; ⁵University of Bordeaux, Talence, France

Conclusion 5:15 PM

Power-Converter Techniques

Session Chair: *Makoto Takamiya, University of Tokyo, Tokyo, Japan*

Associate Chair: *Yen Hsun Hsu, Mediatek, Hsinchu, Taiwan*

1:30 PM

- 27.1 A 0.22-to-2.4V-Input Fine-Grained Fully Integrated Rational Buck-Boost SC DC-DC Converter Using Algorithmic Voltage-Feed-In (AVFI) Topology Achieving 84.1% Peak Efficiency at 13.2mW/mm²**

Y. Jiang¹, M-K. Law¹, P-I. Mak¹, R. P. Martins^{1,2}, ¹University of Macau, Macau, China

²Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

2:00 PM

- 27.2 A 10MHz Time-Domain-Controlled Current-Mode Buck Converter with 8.5% to 93% Switching Duty Cycle**

J-G. Kang, M-G. Jeong, J. Park, C. Yoo, Hanyang University, Seoul, Korea

2:30 PM

- 27.3 An 86% Efficiency SIMO DC-DC Converter with One Boost, One Buck, and a Floating Output Voltage for Car-Radio**

A. Salimath¹, E. Bonizzoni¹, E. Botti², G. Gonano², P. Cacciagrano², D. L. Brambilla², T. Barbieri², F. Maloberti¹, ¹University of Pavia, Pavia, Italy; ²STMicroelectronics, Cornaredo, Italy

Break 3:00 PM

3:15 PM

- 27.4 A 97% High-Efficiency 6 μ s Fast-Recovery-Time Buck-Based Step-Up/Down Converter with Embedded 1/2 and 3/2 Charge-Pumps for Li-Ion Battery Management**

M-W. Ko¹, K-D. Kim¹, Y-J. Woo², S-U. Shin¹, H-K. Han¹, Y. Huh¹, G-G. Kang¹, J-H. Cho¹, S-J. Lim¹, S-H. Park¹, H-M. Lee³, G-H. Cho¹

¹KAIST, Daejeon, Korea; ²Siliconworks, Daejeon, Korea; ³Korea University, Seoul, Korea

3:30 PM

- 27.5 A 95.2% Efficiency Dual-Path DC-DC Step-Up Converter with Continuous Output Current Delivery and Low Voltage Ripple**

S-U. Shin¹, Y. Huh¹, Y. Ju¹, S. Choi¹, C. Shin¹, Y-J. Woo¹, M. Choi¹, S-H. Park¹, Y-H. Sohn¹, M-W. Ko¹, Y. Jo¹, H. Han¹, H-M. Lee², S-W. Hong³, W. Qu⁴, G-H. Cho¹, ¹KAIST, Daejeon, Korea

²Korea University, Seoul, Korea; ³Sookmyung Women's University, Seoul, Korea

⁴Zhejiang University, Hangzhou, China

3:45 PM

- 27.6 An 87.1% Efficiency RF-PA Envelope-Tracking Modulator for 80MHz LTE-Advanced Transmitter and 31dBm PA Output Power for HPUE in 0.153 μ m CMOS**

C-Y. Ho, S-M. Lin, C-H. Meng, H-P. Hong, S-H. Yan, T-H. Kuo, C-S. Peng, C-H. Hsiao, H-H. Chen, D-W. Sung, C-W. Kuan, MediaTek, Hsinchu, Taiwan

4:15 PM

- 27.7 A 2TX Supply Modulator for Envelope-Tracking Power Amplifier Supporting Intra- and Inter-Band Uplink Carrier Aggregation and Power Class-2 High-Power User Equipment**

T. Nomiyama¹, Y. Your², Y. Choo¹, D. Kim¹, J. Han¹, J. Jung¹, J. Baek¹, S. Lee¹, E. Park¹, J. Choi¹, J-S. Paek¹, J. Lee¹, T. B. Cho¹, I. Kang¹

¹Samsung Electronics, Hwaseong, Korea; ²Samsung Semiconductor, San Jose, CA

4:45 PM

- 27.8 94% Power-Recycle and Near-Zero Driving-Dead-Zone N-Type Low-Dropout Regulator with 20mV Undershoot at Short-Period Load Transient of Flash Memory in Smart Phone**

W-C. Chen, T-C. Huang, C-C. Chiu, C-W. Chang, K-C. Hsu, MediaTek, Hsinchu, Taiwan

5:00 PM

- 27.9 An On-Chip Resonant-Gate-Drive Switched-Capacitor Converter for Near-Threshold Computing Achieving 70.2% Efficiency at 0.92A/mm² Current Density and 0.4V Output**

M. Abdelfattah¹, M. Swilam¹, B. Dupaix², S. Smith¹, A. Fayed¹, W. Khalil¹

¹Ohio State University, Columbus, OH; ²Air Force Research Laboratory, Wright-Patterson AFB, OH

Conclusion 5:15 PM

Wireless Connectivity

Session Chair: *Howard Luong*, Hong Kong University of Science and Technology, Hong Kong, China

Associate Chair: *Kyoo Hyun Lim*, FCI, Seongnam, Korea

1:30 PM

28.1 An 802.11ax 4x4 Spectrum-Efficient WLAN AP Transceiver SoC Supporting 1024QAM with Frequency-Dependent IQ Calibration and Integrated Interference Analyzer

S. Kawai¹, H. Aoyama², R. Ito³, Y. Shimizu³, M. Ashida³, A. Mak³, T. Takeuchi³, H. Kobayashi³, G. Urakawa³, H. Hoshino³, S. Saigusa³, K. Koyama⁴, M. Morita², R. Nihei², D. Goto², M. Nagata³, K. Nakata³, K. Ikeuchi¹, K. Yoshioka¹, R. Tachibana³, M. Ara², C-K. Teh², A. Suzuki², H. Yoshida², Y. Hagiwara³, T. Kato², I. Seto¹, T. Horiguchi³, K. Ban¹, K. Takahashi³, H. Kajihara³, T. Yamagishi³, Y. Fujimura³, K. Horiuchi³, K. Nonin¹, K. Kurose³, H. Yamada³, K. Taniguchi¹, M. Sekiya¹, T. Tomizawa³, D. Taki³, M. Ikuta³, T. Suzuki³, Y. Ando³, D. Yashima¹, T. Kaihotsu¹, H. Mori¹, K. Nakanishi¹, T. Kumagaya¹, Y. Uekawa², T. Aoki¹, K. Onizuka¹, T. Mitomo¹

¹Toshiba, Kawasaki, Japan; ²Toshiba Electronic Devices & Storage, Kawasaki, Japan

³Toshiba Memory, Kawasaki, Japan; ⁴Toshiba Microelectronics, Kawasaki, Japan

2:00 PM

28.2 An ADPLL-Centric Bluetooth Low-Energy Transceiver with 2.3mW Interference-Tolerant Hybrid-Loop Receiver and 2.9mW Single-Point Polar Transmitter in 65nm CMOS

H. Liu, Z. Sun, D. Tang, H. Huang, T. Kaneko, W. Deng, R. Wu, K. Okada, A. Matsuzawa
Tokyo Institute of Technology, Tokyo, Japan

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28.3 A 0.8V 0.8mm² Bluetooth 5/BLE Digital-Intensive Transceiver with a **DS2** 2.3mW Phase-Tracking RX Utilizing a Hybrid Loop Filter for Interference Resilience in 40nm CMOS

M. Ding¹, X. Wang¹, P. Zhang¹, Y. He¹, S. Traferro¹, K. Shibata², M. Song¹, H. Korpela¹, K. Ueda², Y-H. Liu¹, C. Bachmann¹, K. Philips¹

¹imec - Holst Centre, Eindhoven, The Netherlands; ²Renesas Electronics, Tokyo, Japan

Break 3:00 PM

3:15 PM

28.4 A 0.45V Sub-mW All-Digital PLL in 16nm FinFET for Bluetooth Low-Energy (BLE) Modulation and Instantaneous Channel Hopping Using 32.768kHz Reference

M-S. Yuan¹, C-C. Li¹, C-C. Liao¹, Y-T. Lin¹, C-H. Chang¹, R. B. Staszewski²

¹TSMC, Hsinchu, Taiwan; ²University College Dublin, Dublin 4, Ireland

3:45 PM

28.5 A 0.2V Energy-Harvesting BLE Transmitter with a Micropower Manager Achieving 25% System Efficiency at 0dBm Output and 5.2nW Sleep Power in 28nm CMOS

J. Yin¹, S. Yang¹, H. Yi¹, W-H. Yu¹, P-I. Mak¹, R. P. Martins^{1,2}, ¹University of Macau, Macau, China

²Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

4:15 PM

28.6 A -76dBm 7.4nW Wakeup Radio with Automatic Offset Compensation

J. Moody, P. Bassirian, A. Roy, N. Liu, S. Pancrazio, N. S. Barker, B. H. Calhoun, S. M. Bowers
University of Virginia, Charlottesville, VA

4:30 PM

28.7 A 14.5mm² 8nW -59.7dBm-Sensitivity Ultrasonic Wake-Up Receiver for **DS2** Power-, Area-, and Interference-Constrained Applications

A. S. Rekhi, A. Arbabian, Stanford University, Stanford, CA

4:45 PM

28.8 A 5.8GHz Power-Harvesting 116µm×116µm "Dielet" Near-Field Radio with **DS2** On-Chip Coil Antenna

B. Zhao, N-C. Kuo, B. Liu, Y-A. Li, L. Iotti, A. M. Niknejad
University of California, Berkeley, Berkeley, CA

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Advanced Biomedical Systems

Session Chair: *Pedram Mohseni*, Case Western Reserve University, Cleveland, OH

Associate Chair: *Nick Van Helleputte*, imec, Heverlee, Belgium

1:30 PM

29.1 Creating Neural "Co-Processors" to Explore Treatments for Neurological Disorders

S. Stanslaski, J. Herron, E. Fehrmann, R. Corey, H. Orser, T. Adamski, T. Denison, Medtronic Neurological Technology, Fridley, MN

2:00 PM

29.2 A Fully Immersible Deep-Brain Neural Probe with Modular Architecture and a Delta-Sigma ADC Integrated Under Each Electrode for Parallel Readout of 144 Recording Sites

D. De Dorigo¹, C. Moranz¹, H. Graf¹, M. Marx¹, B. Shui¹, M. Kuhl¹, Y. Manoli^{1,2}

¹University of Freiburg - IMTEK, Freiburg, Germany

²Hahn-Schickard, Villingen-Schwenningen, Germany

2:30 PM

29.3 A 16384-Electrode 1024-Channel Multimodal CMOS MEA for High-Throughput Intracellular Action Potential Measurements and Impedance Spectroscopy in Drug-Screening Applications

C. Mora Lopez¹, H. S. Chun¹, L. Bert², S. Wang¹, J. Putzeys¹, C. Van Den Bulcke^{1,3}, J-W. Weijers¹, A. Firrincieli¹, V. Reumers¹, D. Braeken¹, N. Van Helleputte¹

¹imec, Heverlee, Belgium; ²Chrysalite, Tervuren, Belgium; ³KU Leuven, Leuven, Belgium

Break 3:00 PM

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29.4 A 0.13 μ m CMOS SoC for Simultaneous Multichannel Optogenetics and **DS2** Electrophysiological Brain Recording

G. Gagnon-Turcotte, C. Ethier, Y. De Koninck, B. Gosselin

Laval University, Quebec City, QC, Canada

3:45 PM

29.5 A mm-Sized Free-Floating Wirelessly Powered Implantable Optical **DS2** Stimulating System-on-a-Chip

Y. Jia¹, S. A. Mirbozorgi¹, B. Lee¹, W. Khan², F. Mad², A. Weber², W. L², M. Ghovanloo¹

¹Georgia Institute of Technology, Atlanta, GA; ²Michigan State University, East Lansing, MI

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29.6 A 92dB Dynamic Range Sub- μ V_{rms}-Noise 0.8 μ W/ch Neural-Recording ADC **DS2** Array with Predictive Digital Autoranging

C. Kim, S. Joshi, H. Courellis, J. Wang, C. Miller, G. Cauwenberghs

University of California, San Diego, La Jolla, CA

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29.7 A 110dB-CMRR 100dB-PSRR Multi-Channel Neural-Recording Amplifier **DS2** System Using Differentially Regulated Rejection Ratio Enhancement in 0.18 μ m CMOS

S. Lee¹, A. K. George¹, T. Lee², J-U. Chu³, S. Han⁴, J-H. Kim⁵, M. Je², J. Lee¹

¹Daegu Gyeongbuk Institute of Science and Technology, Daegu, Korea

²KAIST, Daejeon, Korea; ³Korea Institute of Machinery and Materials, Daegu, Korea

⁴Korea Institute of Science and Technology, Seoul, Korea

⁵Seoul National University of Science and Technology, Seoul, Korea

5:00 PM

29.8 A 43.4 μ W Photoplethysmogram-Based Heart-Rate Sensor Using Heart-Beat-Locked Loop

D-H. Jang, S. Cho, KAIST, Daejeon, Korea

Conclusion 5:15 PM

Emerging Memories

Session Chair: *Shinichiro Shiratake*, Toshiba Memory, Yokohama, Japan
Associate Chair: *Edoardo Charbon*, EPFL, Neuchatel, Switzerland

1:30 PM

30.1 An N40 256K×44 Embedded RRAM Macro with SL-Precharge SA and Low-Voltage Current Limiter to Improve Read and Write Performance

C-C. Chou, Z-J. Lin, P-L. Tseng, C-F. Li, C-Y. Chang, W-C. Chen, Y-D. Chih, T-Y. J. Chang
TSMC, Hsinchu, Taiwan

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30.2 A 1Mb 28nm STT-MRAM with 2.8ns Read Access Time at 1.2V VDD Using Single-Cap Offset-Cancelled Sense Amplifier and In-situ Self-Write-Termination

Q. Dong^{1,2}, Z. Wang¹, J. Lim¹, Y. Zhang¹, Y-C. Shih³, Y-D. Chih³, J. Chang³, D. Blaauw¹, D. Sylvester¹

¹University of Michigan, Ann Arbor, MI

²TSMC, San Jose, CA

³TSMC, Hsinchu, Taiwan

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30.3 A 28nm 32Kb Embedded 2T2MTJ STT-MRAM Macro with 1.3ns Read-Access Time for Fast and Reliable Read Applications

T-H. Yang^{1,2}, K-X. Li¹, Y-N. Chiang¹, W-Y. Lin¹, H-T. Lin¹, M-F. Chang¹

¹National Tsing Hua University, Hsinchu, Taiwan

²TSMC, Hsinchu, Taiwan

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30.4 A 20ns-Write 45ns-Read and 10¹⁴-Cycle Endurance Memory Module Composed of 60nm Crystalline Oxide Semiconductor Transistors

S. Maeda¹, S. Ohshita¹, K. Furutani¹, Y. Yakubo¹, T. Ishizu¹, T. Atsumi¹, Y. Ando¹, D. Matsubayashi¹, K. Kato¹, T. Okuda¹, M. Fujita², S. Yamazaki¹

¹Semiconductor Energy Laboratory, Atsugi, Japan

²University of Tokyo, Tokyo, Japan

Break 3:00 PM

Computation in Memory for Machine Learning

Session Chair: *Naveen Verma*, Princeton University, Princeton, NJ

Associate Chair: *Fatih Hamzaoglu*, Intel, Hillsboro, OR

3:15 PM

31.1 Conv-RAM: An Energy-Efficient SRAM with Embedded Convolution DS2 Computation for Low-Power CNN-Based Machine Learning Applications

A. Biswas, A. P. Chandrakasan

Massachusetts Institute of Technology, Cambridge, MA

3:45 PM

31.2 A 42pJ/Decision 3.12TOPS/W Robust In-Memory Machine Learning DS2 Classifier with On-Chip Training

S. K. Gonugondla, M. Kang, N. Shanbhag

University of Illinois, Urbana-Champaign, IL

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31.3 Brain-Inspired Computing Exploiting Carbon Nanotube FETs and DS2 Resistive RAM: Hyperdimensional Computing Case Study

T. F. Wu¹, H. Li¹, P.-C. Huang², A. Rahim², J. M. Rabaey², P. Wong¹, M. M. Shulaker³, S. Mitra¹

¹Stanford University, Stanford, CA

²University of California, Berkeley, Berkeley, CA

³Massachusetts Institute of Technology, Cambridge, MA

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31.4 A 65nm 1Mb Nonvolatile Computing-in-Memory ReRAM Macro with Sub-16ns Multiply-and-Accumulate for Binary DNN AI Edge Processors

W.-H. Chen, K.-X. Li, W.-Y. Lin, K.-H. Hsu, P.-Y. Li, C.-H. Yang, C.-X. Xue, E.-Y. Yang, Y.-K. Chen, Y.-S. Chang, T.-H. Hsu, Y.-C. King, C.-J. Lin, R.-S. Liu, C.-C. Hsieh, K.-T. Tang, M.-F. Chang

National Tsing Hua University, Hsinchu, Taiwan

5:00 PM

31.5 A 65nm 4Kb Algorithm-Dependent Computing-in-Memory SRAM Unit- Macro with 2.3ns and 55.8TOPS/W Fully Parallel Product-Sum Operation for Binary DNN Edge Processors

W.-S. Khwa^{1,2}, J.-J. Chen¹, J.-F. Li¹, X. Si³, E.-Y. Yang¹, X. Sun⁴, R. Liu⁴, P.-Y. Chen⁴, Q. Li³, S. Yu⁴, M.-F. Chang¹

¹National Tsing Hua University, Hsinchu, Taiwan

²TSMC, Hsinchu, Taiwan

³University of Electronic Science and Technology of China, Sichuan, China

⁴Arizona State University, Tempe, AZ

Conclusion 5:15 PM

Short Course: Hardware Approaches to Machine Learning and Inference

Time:	Topic:
8:00 AM	Breakfast
8:20 AM	Introduction by Chair, Daniel Friedman <i>IBM Thomas J. Watson Research Center, Yorktown Heights, NY</i>
8:30 AM	Introduction to Machine Learning and Inference Gu-Yeon Wei , <i>Harvard University, Cambridge, MA</i>
10:00 AM	Break
10:30 AM	Algorithm and Implementation Co-Design for Learning and Inference Marian Verhelst , <i>KU Leuven, Heverlee, Belgium</i>
12:15 PM	Lunch
1:20 PM	Efficient Edge Solutions for Deep Learning Applications Vivienne Sze , <i>Massachusetts Institute of Technology, Cambridge, MA</i>
2:50 PM	Break
3:20 PM	Efficient Alternatives and Extensions to Deep-Learning-Based Solutions Naveen Verma , <i>Princeton University, Princeton, NJ</i>
4:50 PM	Conclusion

Introduction

Advances in artificial intelligence are already changing how computing systems interact with users and interact with their environments, with further dramatic changes on the horizon. In this context, machine learning and inference operations have become a critically important computational workload, and the importance of this workload will continue to increase. Today, GPU-, CPU-, and FPGA-based engines dominate the compute landscape for learning and for inference, but the exploration of alternative, enhanced, or complementary compute capability in this problem space is an active and growing research area. In this short course, we will provide a framework for understanding some of the computational challenges in machine learning and inference and discuss emerging technical approaches aimed at meeting those challenges.

The first presentation in the course will provide an overview of machine learning and inference. It will start with a discussion of deep learning and machine learning, then will proceed to describe neural network approaches, model structures and layer types, and will use specific examples to clarify concepts. In the next talk, algorithm and implementation co-optimization for learning and inference will be discussed, including exploration of how applications can be used to drive design choices. In the third presentation, data flow approaches and energy considerations will be discussed in the context of machine learning and inference problems, including the application of the presented design principles to a specific accelerator implementation. Finally, the last presentation will discuss a different but related class of problems, such as continuous learning with limited data, and hardware approaches suited to solving such problems. Broadly, the four presentations will provide machine learning context, associated computation- and application-driven considerations, and a discussion of emerging approaches for machine learning and inference hardware implementation, the latter supported by specific illustrative design examples.

8:30 AM SC1: Introduction to Machine Learning and Inference*Gu-Yeon Wei, Harvard University, Cambridge, MA*

Machine learning, and in particular deep learning, has received a great deal of attention in recent years as it has disrupted many fields of electrical engineering and computer science. The success of deep-learning techniques comes from their ability to solve notoriously difficult classification and regression problems. Much of deep learning's recent successes can be attributed to a virtuous cycle of advances in computing hardware, the availability of huge amounts of labeled data, and development of deeper models. This talk introduces the broad and dynamic field of deep learning for hardware designers. We begin with a brief history and review key innovations that have led to the powerful deep-learning techniques we see today. We will review the different types of learning widely used today with a focus on neural network models for inference applied across a variety of domains. The primary objective of this talk is to help and motivate chip designers to engage in this exciting opportunity and further push the impact of deep learning via hardware-level innovations.

Gu-Yeon Wei is Gordon McKay Professor of Electrical Engineering and Computer Science in the Paulson School of Engineering and Applied Sciences (SEAS) at Harvard University and currently serves as Area Chair for Electrical Engineering. He received his BS, MS, and PhD degrees in Electrical Engineering from Stanford University. His research interests span multiple layers of a computing system: mixed-signal integrated circuits, computer architecture, and design tools for efficient hardware. His research efforts focus on identifying synergistic opportunities across these layers to develop energy-efficient solutions for a broad range of systems from flapping-wing microrobots to machine learning hardware for IoT devices to large-scale servers.

10:30 AM SC2: Algorithm and Implementation Co-Design for Learning and Inference*Marian Verhelst, KU Leuven, Heverlee, Belgium*

As deep learning comes with significant computational complexity, only relatively recently has this technology become feasible on power-hungry server platforms. In the past few years, we have seen a trend from server-based processing towards embedded processing of the computation for deep learning networks. It is crucial to understand that this evolution is not enabled by either novel architectures or novel deep learning algorithms alone. The breakthroughs clearly come from a close co-optimization between algorithms and implementation architectures. In this presentation, we will review a wide range of recent techniques to a) make the learning algorithms implementation-aware and b) make the hardware implementations algorithm-aware.

Marian Verhelst is assistant professor at MICAS – KU Leuven, Belgium. Her research focuses on embedded machine learning, low-power sensing, and processing for the internet of things. Marian is member of the Young Academy of Belgium, the ISSCC and DATE executive committees, and is an associate editor of JSSC.

1:20 PM SC3: Efficient Edge Solutions for Deep Learning Applications*Vivienne Sze, Massachusetts Institute of Technology, Cambridge, MA*

Visual object detection and recognition are needed for a wide range of applications including robotics/drones, self-driving cars, smart Internet of Things, and portable/wearable electronics. For many of these applications, local embedded processing is preferred due to privacy or latency concerns. This talk will describe methods to enable energy-efficient processing of deep convolutional neural networks (CNN), as such networks form the cornerstone of many deep-learning algorithms. While CNNs deliver record-breaking accuracy for many computer vision tasks, they require significant compute resources due to the size of the networks (e.g., hundreds of megabytes for filter weights storage and 30k-600k operations per input pixel). We will give a short overview of the key concepts in CNNs, discuss the computational challenges CNNs present, particularly in the embedded space, and highlight various opportunities where hardware designers can help to address these challenges.

Vivienne Sze is an Associate Professor at MIT in the Electrical Engineering and Computer Science Department. Her research interests include energy-aware signal processing algorithms, and low-power circuit and system design for multimedia applications such as computer vision, autonomous navigation, machine learning and video compression. Prior to joining MIT, she was a Member of Technical Staff in the R&D Center at TI, where she developed algorithms and hardware for the latest video coding standard H.265/HEVC. She is a co-editor of the book entitled, “High Efficiency Video Coding (HEVC): Algorithms and Architectures” (Springer, 2014).

Dr. Sze received the B.A.Sc. degree from the University of Toronto in 2004, and the S.M. and Ph.D. degree from MIT in 2006 and 2010, respectively. In 2011, she was awarded the Jin-Au Kong Outstanding Doctoral Thesis Prize in electrical engineering at MIT for her thesis on “Parallel Algorithms and Architectures for Low Power Video Decoding”. She is a recipient of the 2017 Qualcomm Faculty Award, 2016 Google Faculty Research Award, 2016 AFOSR Young Investigator Award, 2016 3M Non-tenured Faculty Award, 2014 DARPA Young Faculty Award, 2007 DAC/ISSCC Student Design Contest Award and a co-recipient of the 2016 MICRO Top Picks Award and 2008 A-SSCC Outstanding Design Award.

More information about our research in the Energy-Efficient Multimedia Systems group can be found at: <http://www.rle.mit.edu/eems/>

3:20 PM SC4: **Efficient Alternatives and Extensions to Deep-Learning-Based Solutions**

Naveen Verma, Princeton University, Princeton, NJ

Deep-learning systems have had profound impacts in a broad range of applications. However, it is important to remember that these represent only one class of machine learning. In this segment of the short course, we start by probing what the critical attributes are of deep learning, and what challenges in modeling and inference they solve. We then go on to consider the limitations of deep learning in emerging applications involving on-line learning (e.g. reinforcement learning with embedded sensors) – namely the need for a large number of training instances and the need for very low energy. This motivates alternatives or extensions to deep learning, which make use of other forms of learning to enhance training and energy efficiency. Given the need for very low energy in many applications, we explore how the statistical-learning can enable new hardware architectures, substantially overcoming the tradeoffs limiting conventional architectures for sensing and computation. Finally, having examined how algorithmic techniques can enhance systems, we look at how systems, and emerging technologies for sensing, can enhance algorithms. As an illustration, we consider how object-associated sensing, as enabled by IoT devices, has the potential to provide semantic structure, leading to features that can enhance the generalization of learning with simpler and easier-to-train models.

Naveen Verma received the B.A.Sc. degree in Electrical and Computer Engineering from the University of British Columbia, Vancouver, Canada in 2003, and the M.S. and Ph.D. degrees in Electrical Engineering from the Massachusetts Institute of Technology in 2005 and 2009 respectively. Since July 2009 he has been with the department of Electrical Engineering at Princeton University, where he is currently an Associate Professor. His research focuses on advanced sensing systems, including low-voltage digital logic and SRAMs, low-noise analog instrumentation and data-conversion, large-area sensing systems based on flexible electronics, and low-energy algorithms for embedded inference, especially for medical applications. Prof. Verma is a Distinguished Lecturer of the IEEE Solid-State Circuits Society, and serves on the technical program committees for ISSCC, VLSI Symp., DATE, and the IEEE Signal-Processing Society (DISPS). Prof. Verma is a recipient or co-recipient of the 2006 DAC/ISSCC Student Design Contest Award, the 2008 ISSCC Jack Kilby Paper Award, the 2012 Alfred Rheinlein Junior Faculty Award, the 2013 NSF CAREER Award, the 2013 Intel Early Career Award, the 2013 Walter C. Johnson Prize for Teaching Excellence, the 2013 VLSI Symp. Best Student Paper Award, the 2014 AFOSR Young Investigator Award, the 2015 Princeton Engineering Council Excellence in Teaching Award, and the 2015 IEEE Trans. CPMT Best Paper Award.

F3: Circuits and Architectures for Wireless Sensing, Radar and Imaging

Organizer: Brian Ginsburg, Texas Instruments, Dallas, TX

Committee: Payam Lajevardi, Robert Bosch LLC, Palo Alto, CA
 Andrea Mazzanti, Università di Pavia, Pavia, Italy
 Hayato Wakabayashi, Sony, San Jose, CA
 Yuu Watanabe, Waseda University, Kanagawa, Japan
 Alan Wong, EnSilica, Abingdon, United Kingdom

Remote sensing has become an increasingly important area of development in the last few years. Various kinds of signals are used: electromagnetic waves at RF and mm-wave frequencies, infrared and visible light, and acoustic waves. These sensors also require sophisticated signal conditioning and signal processing to extract relevant information from background clutter. This forum gives an overview of circuits, sensors and entire systems that are based on these technologies.

Forum Agenda

Time:	Topic:
8:00 AM	Breakfast
8:30 AM	Introduction by Chair
8:35 AM	Integrated Circuits for Next-Generation Miniature Ultrasound Probes <i>Michiel Pertijs, Delft University of Technology, Delft, The Netherlands</i>
9:25 AM	Emerging Electromagnetic-Acoustic Sensing and Imaging Beyond Radar and Ultrasound <i>Yuanjin Zheng, Nanyang Technological University, Singapore, Singapore</i>
10:15 AM	Break
10:35 AM	Systems and Algorithms For Millimeter-Resolution Imaging: From mm-Wave Radar to Multi-Physics RF-Ultrasound Approaches <i>Amin Arbabian, Stanford University, Stanford, CA</i>
11:25 AM	Portable Continuous-Wave Radar for Non-Contact Sensing and Localization <i>Changzhi Li, Texas Tech University, Lubbock, TX</i>
12:15 PM	Lunch
1:20 PM	Radar Circuits and Systems for Vital Signs Monitoring <i>Jorgen Andreas Michaelsen, Novelda, Oslo, Norway</i>
2:10 PM	Challenges and Opportunities in Automotive Radar Systems <i>Karthik Ramasubramanian, Texas Instruments, Bangalore, India</i>
3:00 PM	Break
3:20 PM	What's the Best Technology and Architecture for your Time of Flight System? <i>David Stoppa, ams AG, Rueschlikon, Switzerland</i>
4:10 PM	Optical Phased Array LiDAR <i>Michael Watts, Analog Photonics, Boston, MA</i>
5:00 PM	Conclusion

F4: Circuit and System Techniques for mm-Wave Multi-Antenna Systems

Organizer: Pierre Busson, ST Microelectronics, Crolles, France

Committee: Howard Luong, Hong Kong University of Science and Technology, Hong Kong, China

Chih-Ming Hung, MediaTek, Hsin-Chu, Taiwan

Harish Krishnaswamy, Columbia University, New York, NY

Theodore Georgantas, Broadcom, Athens, Greece

Patrick P. Mercier, University of California San Diego, La Jolla, CA

The 5th generation wireless system (5G) is proposed as the next major revolution of mobile wireless technologies. Carrier frequencies in the mm-wave bands and MIMO/multi-antenna systems are expected to be extensively employed to achieve significantly enhanced data rate, spectral/spatial diversity/efficiency and minimized system latency. The design of commercial high-performance radio transceivers at mm-wave represents a major technical challenge. This forum is focused on current state-of-the-art and future directions of multi-antenna systems in the mm-wave bands, from both system architecture and circuit design perspectives. Key system integration aspects such as antenna design, packaging and built-in self-test will also be covered.

Forum Agenda

<u>Time:</u>	<u>Topic:</u>
8:00 AM	Breakfast
8:10 AM	Introduction by Chair
8:15 AM	Broadband Architectures and Multiport Antennas co-design for Frequency, Pattern and Spatial Diversity in mm-Wave MIMO Arrays <i>Kaushik Sengupta, Princeton University, Princeton, NJ</i>
9:00 AM	Multi-Beam Phased Arrays for 5G Systems <i>Kazuaki Kunihiro, NEC, Kawasaki, Japan</i>
9:45 AM	Phased Arrays and 5G: The End of the Marconi Era is Near <i>Gabriel Rebeiz, UCSD, San Diego, CA</i>
10:30 AM	Break
10:45 AM	CMOS PA Design at mm-Wave Frequencies <i>Patrick Reynaert, KU Leuven, Leuven, Belgium</i>
11:30 AM	Advances in mm-Wave Phased Arrays for Beamforming in 5G Systems <i>Alberto Valdes-Garcia, IBM T. J. Watson Research Center, Yorktown Heights, NY</i>
12:15 PM	Lunch
1:30 PM	Power Amplifiers in Advanced Antenna Systems <i>Ulf Gustavsson, Ericsson, Göteborg, Sweden</i>
2:15 PM	Integration of mm-Wave Antennas Using Organic Packaging Technologies up to 240GHz <i>Cyril Luxey, University of Nice, Valbonne, France</i>
3:00 PM	Break
3:15 PM	New Wave SiP for mm-Wave <i>CP Hung, Advanced Semiconductor Engineering Group, Kaohsiung, Taiwan</i>
4:00 PM	Non-Invasive Calibration and Built-In Self Test (BIST) for Phased-Array Systems <i>Jose Luis Gonzalez, CEA-LETI-MINATEC, Grenoble, France</i>
4:45 PM	Conclusion

F5: Advanced Optical Communication: From Devices, Circuits, and Architectures to Algorithms

Organizer: Bo Zhang, *Broadcom, Irvine, CA*
Committee: Frederic Giancesello, *STMicroelectronics, Crolles, France*
 Simone Erba, *STMicroelectronics, Pavia, Italy*
 Mounir Meghelli, *IBM Thomas J Watson Research Center,
Yorktown Heights, NY*
 Azita Emami, *California Institute of Technology, Pasadena, CA*
 Takayuki Shibasaki, *Fujitsu Laboratories, Kawasaki, Japan*

Since the invention of optical fiber in the 1970's, optical communication has been changing the landscape of telecommunication and data communication worldwide with its ultra-broad bandwidth and long haul transmission capabilities. It connects people around the world through submarine inter-continent optical cables, is the backbone of metro area networks, and is essential for data center network connectivity. Today, cost effective 100Gb/s optical links on a single fiber, using either III-V based optical devices or silicon photonics, are readily available for few meters to few kilometers connectivity solutions inside the data center and between data centers, while next generation links are poised to reach 400Gb/s. In this forum, the current state-of-the-art of optical communications will be reviewed, including advances in long-haul transport, progress in silicon photonics covering transceivers, packaging, assembly and test, progress in high order modulation schemes and signal processing, description of 56Gb/s and beyond electrical serial interfaces, and closing with a presentation on optical backplane technology.

Forum Agenda

<u>Time:</u>	<u>Topic:</u>
8:00 AM	Breakfast
8:20 AM	Introduction
8:30 AM	Scalable Optical Transport Network with Capacity over One Petabit per Second <i>Yutaka Miyamoto, NTT, Yokosuka, Japan</i>
9:20 AM	Insights Into Silicon Photonics Electro-Optical Transceiver Front-Ends <i>Enrico Temporiti, STMicroelectronics, Pavia, Italy</i>
10:10 AM	Break
10:35 AM	New Paradigm Shift to PAM4 Signaling at 100/400G for Cloud Data Centers <i>Frank Chang, Inphi, Thousand Oaks, CA</i>
11:25 AM	Mixed-Signal Electrical Transceivers for 56Gb/s and Beyond <i>Elad Alon, University of California at Berkeley, Berkeley, CA</i>
12:15 PM	Lunch
1:20 PM	ADC/DAC/DSP-Based Transceivers for 400Gb and Beyond: Opportunities and Challenges from Kilometres to Hundreds of Kilometres Reach <i>Ian Dedic, Acacia Communication, Wooburn Green, U.K.</i>
2:10 PM	Advanced Modulation and Signal Processing Empowering Optical Communication <i>David P. Johnson, Ciena, Ottawa, Canada</i>
3:00 PM	Break
3:20 PM	Leveraging Semiconductor Technologies for Packaging, Assembly and Test of Advanced Silicon Photonics <i>Peter De Dobbelaere, Luxtera, Carlsbad, CA</i>
4:10 PM	Optical Backplane Technology Using Fiber Wiring Sheet and Connectors <i>Masahiro Aoyagi, AIST, Tsukuba, Japan</i>
5:00 PM	Closing Remarks

F6: Advances in Energy Efficient Analog Design**Organizer:** Axel Thomsen, Cirrus Logic Inc., Austin, TX**Committee:** **Bernhard Wicht**, Leibniz Universität Hannover, Hannover, Germany
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Analog Design covers a wide range of applications. In this forum we focus on trends in analog design that are driven by hot applications. The desire for better wireless sensor nodes has driven advances in nano-power design and modeling, for infrastructure, power, and data-conversion circuits. Burst mode operation for oscillators, and better power efficiency for sensor interface circuits are also desired. This forum starts with an overview of limits to power efficiency and then dives into various design challenges that have been met by novel solutions.

Forum Agenda

Time:	Topic:
8:00 AM	Breakfast
8:00 AM	Introduction by Chair
8:30 AM	General Overview of Power Consumption Fundamental Limits in Analog Circuits <i>Yannis Tsvidis, Columbia University, New York, NY</i>
9:20 AM	Energy Efficient Nyquist-Rate ADCs <i>Klaas Bult, Analog Design Consult B.V., Bosch en Duin, The Netherlands</i>
10:10 AM	Break
10:35 AM	Energy-Efficient Amplifiers <i>Gyu-Hyeong Cho, KAIST, Daejeon, Korea</i>
11:25 AM	High-Frequency Multiphase Hysteretic Switching Regulators for High Current Slew Rate SoCs <i>D. Brian Ma, University of Texas, Dallas, TX</i>
12:15 PM	Lunch
1:20 PM	Nano-Watt References and Oscillators <i>Jae-Yoon Sim, Pohang University of Science and Technology, Pohang, Korea</i>
2:10 PM	Nano-Watt SAR ADC Design <i>Chih Cheng Hsieh, National Tsing Hua University, Hsinchu, Taiwan</i>
3:00 PM	Break
3:20 PM	Nanopower DC-DC Converters: From Harvesting Interface to Power-Supply Applications <i>Gaël Pillonnet, CEA-LETI-MINATEC, Grenoble, France</i>
4:10 PM	Energy-Efficient Clock Generation for IoT Applications <i>Ming Ding, imec - Holst Centre, Eindhoven, The Netherlands</i>
5:00 PM	Closing remarks by Chair

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Saturday,	February 10	4:00 pm to 7:00 pm
Sunday,	February 11	6:30 am to 8:30 pm
Monday,	February 12	6:30 am to 3:00 pm
Tuesday,	February 13	8:00 am to 3:00 pm
Wednesday,	February 14	8:00 am to 3:00 pm
Thursday,	February 15	7:00 am to 2:00 pm

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Deadlines: The deadline for registering at the Early Registration rates is 11:59 pm Pacific Time **Sunday January 7, 2018**. After January 7th, and on or before 11:59 pm Pacific Time **Sunday January 21, 2018**, registrations will be processed **at the Late Registration rates**. **After January 21st, you must register at the on-site rates.** You are urged to register early to obtain the lowest rates and ensure your participation in all aspects of ISSCC.

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Technical Sessions: Registration includes admission to all technical and evening sessions starting Sunday evening and continuing throughout Monday, Tuesday and Wednesday. ISSCC does not offer partial conference registrations.

Technical Book Display: Several technical publishers will have collections of professional books and textbooks for sale during the Conference. The Book Display will be open on Monday from Noon to 7:00 pm; on Tuesday from 10:00 am to 7:00 pm; and on Wednesday from 10:00 am to 3:00 pm.

Demonstration Sessions: Hardware demonstrations will support selected papers on Monday and Tuesday evenings.

Author Interviews: Author Interviews will be held Monday, Tuesday and Wednesday evenings. Authors from each day’s papers will be available to discuss their work.

Social Hour: Social Hour refreshments will be available starting at 5:15 pm.

University Events: Several universities are planning social events during the Conference. Check the University Events display at the conference for the list of universities, locations and times of these events.

ISSCC Travel Umbrella: A compact travel umbrella will be given to all Conference registrants.

Publications: Conference registration includes:

-The **Digest of Technical Papers** in hard copy and by download. The Digest book will be distributed beginning on Sunday at 10:00 am.

-**Papers Visuals:** The visuals from all papers presented will be available by download.

-**Demonstration Session Guidebook:** A descriptive guide to the Demonstration Session will be available by download.

-**Note:** Instructions will be provided for access to all downloads. Downloads will be available both during the Conference and for a limited time afterwards.

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Educational Events: Many educational events are available at ISSCC for an additional fee. There are ten 90-minute Tutorials and two all-day Forums on Sunday. There are four additional all-day Forums on Thursday as well as an all-day Short Course. All events include a course handout in color. The Forums and Short Course include breakfast, lunch and break refreshments. The Tutorials include break refreshments. See the schedule for details of the topics and times. **New:** A “Thursday All-Access Pass” is available that provides access to all Thursday educational events and a copy of each course handout. Pick just the speakers you want to hear!

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ISSCC 2018 Publications: The following ISSCC 2018 publications can be purchased in advance or on site:

2018 ISSCC Download USB: All of the downloads included in conference registration (**mailed in March**).

2018 Tutorials USB: All of the 90 minute Tutorials (**mailed in May**).

2018 Short Course USB: “Hardware Approaches to Machine Learning and Inference” (**mailed in May**).

The Short Course and Tutorial USBs contain audio and written English transcripts synchronized with the presentation visuals. In addition, the USBs contain a pdf file of the presentations and pdf files of key reference material.

Earlier ISSCC Publications: Selected publications from earlier conferences can be purchased. There are several ways to purchase this material:

-Items listed on the registration form can be purchased with registration and picked up at the conference.

-Visit the ISSCC Publications Desk. This desk is located in the registration area and has the same hours as conference registration. With payment by cash, check or credit card, you can purchase materials at this desk. See the posted list at the Conference for titles and prices.

-Visit the ISSCC website at www.isscc.org and click on the link “About/Shop ISSCC/Shop Now” where you can order online or download an order form to mail, email or fax. For a small shipping fee, this material will be sent to you immediately and you will not have to wait until you attend the Conference to get it.

HOW TO MAKE HOTEL RESERVATIONS

Online: ISSCC participants are urged to make their hotel reservations at the San Francisco Marriott Marquis online. Go to the conference website and click on the Hotel Reservation link.

Conference room rates are \$272 for a single/double, \$297 for a triple and \$322 for a quad (per night plus tax). In addition, ISSCC attendees booked in the ISSCC group receive **in-room Internet access for free**. All online reservations require the use of a credit card. Online reservations are confirmed immediately. You should print the page containing your confirmation number and reservation details and bring it with you when you travel to ISSCC.

Telephone: Call 877-622-3056 (US) or 415-896-1600 and ask for “Reservations.” When making your reservation, identify the group as ISSCC 2018 to get the group rate.

Hotel Deadline: Reservations must be received at the San Francisco Marriott Marquis no later than 5 pm Pacific Time January 21, 2018 to obtain the special ISSCC rates. A limited number of rooms are available at these rates. **Once this limit is reached or after January 21st, the group rates may no longer be available and reservations will be filled at the best available rate.** Changes: Before the hotel deadline, your reservation can be changed by calling the telephone numbers above. After the hotel deadline, call the Marriott Marquis at 415-896-1600 (ask for “Reservations”). Have your hotel confirmation number ready.

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REFERENCE INFORMATION

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Conference Website:	www.isscc.org
ISSCC Email:	ISSCC@ieee.org
Registration questions:	ISSCCinfo@yesevents.com
Hotel Information:	San Francisco Marriott Marquis 780 Mission Street San Francisco, CA 94103 Phone: 415-896-1600
Press Information:	Kenneth C. Smith University of Toronto Email: lcfujino@aol.com Phone: 416-418-3034
Registration:	YesEvents 1700 Reisterstown Road #236 Baltimore, MD 21208 Email: issccinfo@yesevents.com Phone: 410-559-2200 or 800-937-8728 Fax: 410-559-2217

Hotel Transportation: Visit the ISSCC website "Registration/Transportation from Airport" page for helpful travel information and links. You can get a map and driving directions from the hotel website at www.marriott.com/hotels/travel/sfodt-san-francisco-marriott-marquis/

Next ISSCC Dates and Location:

ISSCC 2019 will be held on February 17-21, 2019
at the San Francisco Marriott Marquis Hotel.

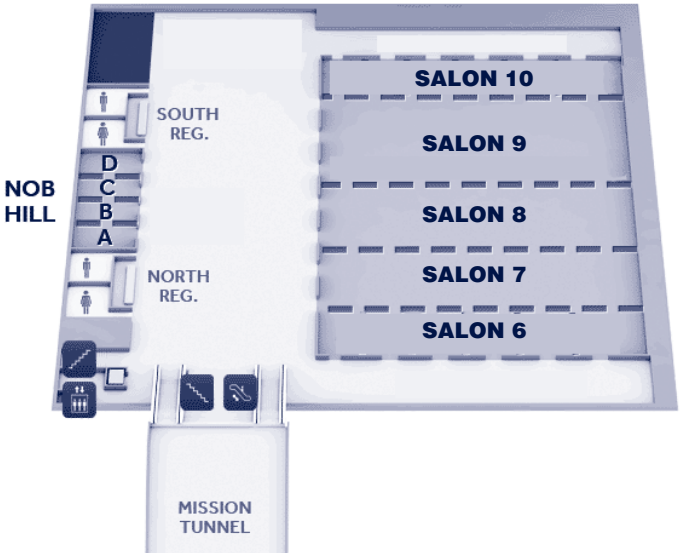
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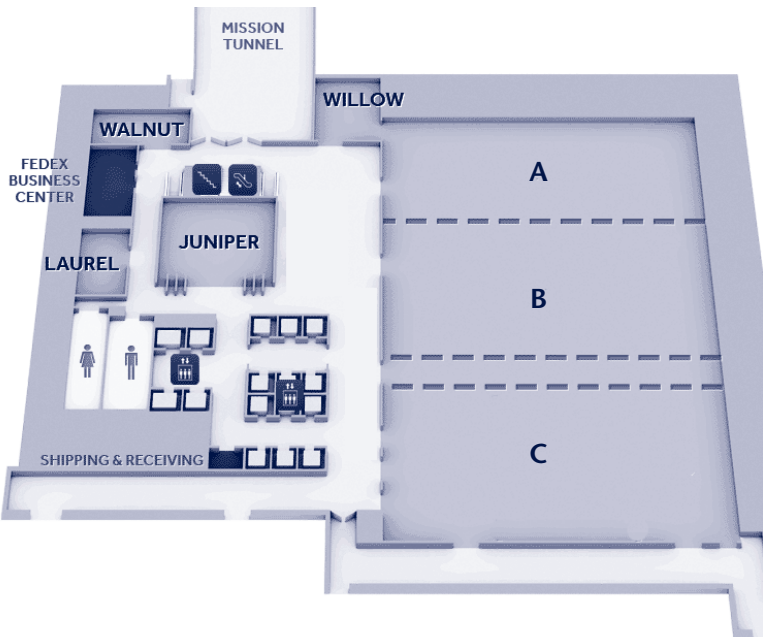
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CONFERENCE SPACE LAYOUT

LOWER B2 LEVEL - YERBA BUENA BALLROOM



B2 LEVEL - GOLDEN GATE HALL





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