2022 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

FEBRUARY 19, 20, 21, 22, 23, 24, 25, 26

ALL VIRTUAL

CONFERENCE THEME:
Intelligent Silicon for a Sustainable World

DRAFT 1 - 19 - 2022
ISSCC VISION STATEMENT
The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and application to maintain technical currency, and to network with leading experts.

ISSCC 2022 ON-DEMAND CONTENT / RELEASE

<table>
<thead>
<tr>
<th>ISSCC On-Demand Content</th>
<th>Release Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>TUTORIALS</td>
<td>Friday, February 11, 5PM PST</td>
</tr>
<tr>
<td>FORUMS, SHORT COURSE</td>
<td>Friday, February 18, 5PM PST</td>
</tr>
<tr>
<td>TECHNICAL PAPERS</td>
<td>Friday, February 18, 5PM PST</td>
</tr>
<tr>
<td>PLENARY TALKS</td>
<td>Monday, February 21, 7AM PST</td>
</tr>
</tbody>
</table>

Recorded content available until March 31, 2022

CONFERENCE TECHNICAL HIGHLIGHTS
This year, ISSCC 2022 will be available only virtually.

See next page for Conference schedule details.
## ISSCC 2022 Timetable

### ISSCC 2022 • Sunday February 20th

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
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<tbody>
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<td>8:30 AM</td>
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### ISSCC 2022 • Monday February 21st

<table>
<thead>
<tr>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td>8:30 AM</td>
<td>Paper Sessions</td>
<td>Session 2: Processors</td>
<td>Session 3: Analog Techniques &amp; Sensor Interfaces</td>
</tr>
<tr>
<td>8:00 AM</td>
<td></td>
<td>9:00 AM</td>
<td>8:30 AM</td>
</tr>
</tbody>
</table>

### ISSCC 2022 • Tuesday February 22nd

<table>
<thead>
<tr>
<th>Time</th>
<th>Plenary II</th>
<th>7:00 AM – 1.3: The Art of Scaling: Distributed and Connected to Sustain the Golden Age of Computation</th>
<th>7:45 AM – 1.4: The Future of the High-Performance Semiconductor Industry and Design</th>
</tr>
</thead>
<tbody>
<tr>
<td>8:30 AM</td>
<td>Paper Sessions</td>
<td>Session 2: Processors</td>
<td>Session 3: Analog Techniques &amp; Sensor Interfaces</td>
</tr>
<tr>
<td>8:00 AM</td>
<td></td>
<td>9:00 AM</td>
<td>8:30 AM</td>
</tr>
</tbody>
</table>

### ISSCC 2022 • Wednesday February 23rd

<table>
<thead>
<tr>
<th>Time</th>
<th>Highlighted Industry Chips &amp; Demonstration Sessions</th>
<th>7:00 AM – Session 21: Highlighted Chip Releases: Digital/ML</th>
<th>7:00 AM – Demonstration Session 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>8:00 AM</td>
<td></td>
<td>8:30 AM</td>
<td>8:45 AM</td>
</tr>
</tbody>
</table>

### ISSCC 2022 • Thursday February 24th

<table>
<thead>
<tr>
<th>Time</th>
<th>Special Events</th>
<th>7:00 AM – SE3: Semiconductor Supply Chain</th>
<th>7:00 AM – SE4: The Bright and Dark Side of Artificial Intelligence (AI)</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:00 AM</td>
<td>Paper Sessions</td>
<td>Session 29: ML Chips for Emerging Applications</td>
<td>Session 30: Power Management Techniques</td>
</tr>
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<td>8:30 AM</td>
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<td>8:30 AM</td>
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</tbody>
</table>

### ISSCC 2022 • Friday February 25th

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
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</thead>
<tbody>
<tr>
<td>7:00 AM</td>
<td></td>
<td>F1: Compute-in-X (CiX): Overcoming the Data Bottleneck in AI Processing</td>
<td>F2: Chip Design for Low-Power, Robust, and Secure IoT Devices</td>
<td>F3: The Path to 6G: Architectures, Circuits, Technologies for Sub-Terahertz Communications, Sensing and Imaging</td>
</tr>
<tr>
<td>8:30 AM</td>
<td>Special Events</td>
<td>8:30 AM – SE5: Shifting Tides of Innovation – Where is Cutting-Edge Research Happening Today?</td>
<td>8:30 AM – SE6: Next Trillion Dollar Market</td>
<td></td>
</tr>
</tbody>
</table>

### ISSCC 2022 • Saturday February 26th

<table>
<thead>
<tr>
<th></th>
<th></th>
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<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>7:00 AM</td>
<td>SRP and WIC Mentoring Sessions</td>
<td>7:00 AM – SRP and WIC Mentoring Sessions</td>
<td>7:00 AM – SRP and WIC Mentoring Sessions</td>
<td>7:00 AM – SRP and WIC Mentoring Sessions</td>
<td>7:00 AM – SRP and WIC Mentoring Sessions</td>
</tr>
</tbody>
</table>

---
# TABLE OF CONTENTS

**Tutorials** ................................................................................................................................. 4-8

**SPECIAL EVENTS**

SE1  Student Research Preview: Short Presentations with Poster Session ................................. .9
SE2  Next Generation Circuit Designer 2022 Workshop ................................................................. 10-11

**PAPER SESSIONS**

<table>
<thead>
<tr>
<th>Session</th>
<th>Topic</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Plenary I</td>
<td>12</td>
</tr>
<tr>
<td>2</td>
<td>Processors</td>
<td>13</td>
</tr>
<tr>
<td>3</td>
<td>Analog Techniques &amp; Sensor Interfaces</td>
<td>14</td>
</tr>
<tr>
<td>4</td>
<td>mm-Wave and Sub-THz ICs for Communication and Sensing</td>
<td>15</td>
</tr>
<tr>
<td>5</td>
<td>Image, Range Sensors and Displays</td>
<td>16</td>
</tr>
<tr>
<td>6</td>
<td>Ultra-High-Speed Wireline</td>
<td>17</td>
</tr>
<tr>
<td>7</td>
<td>NAND Flash Memory</td>
<td>18</td>
</tr>
<tr>
<td>8</td>
<td>Plenary II</td>
<td>19</td>
</tr>
<tr>
<td>9</td>
<td>Advanced RF Building Blocks</td>
<td>20</td>
</tr>
<tr>
<td>10</td>
<td>High-Quality GHz-to-THz Frequency Generation and Radiation</td>
<td>21</td>
</tr>
<tr>
<td>11</td>
<td>Nyquist and Incremental ADCs</td>
<td>22</td>
</tr>
<tr>
<td>12</td>
<td>Compute-in-Memory and SRAM</td>
<td>23</td>
</tr>
<tr>
<td>13</td>
<td>Monolithic System for Robot and Bio Applications</td>
<td>24</td>
</tr>
<tr>
<td>14</td>
<td>Digital Techniques for Clocking, Variation Tolerance and Power Management</td>
<td>25</td>
</tr>
<tr>
<td>15</td>
<td>GaN, High-Voltage and Wireless Power</td>
<td>26</td>
</tr>
</tbody>
</table>

**INVITED PAPERS**

21  Highlighted Chip Releases: Digital/ML............................................................................. 27

Demonstration Session 1

26  Highlighted Chip Releases: Systems and Quantum Computing .................................................. 29

Demonstration Session 2

**PAPER SESSIONS**

<table>
<thead>
<tr>
<th>Session</th>
<th>Topic</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>ML Processors</td>
<td>31</td>
</tr>
<tr>
<td>16</td>
<td>Emerging Domain-Specific Digital Circuits and Systems</td>
<td>32</td>
</tr>
<tr>
<td>17</td>
<td>Advanced Wireline Links and Techniques</td>
<td>33</td>
</tr>
<tr>
<td>18</td>
<td>DC-DC Converters</td>
<td>34</td>
</tr>
<tr>
<td>19</td>
<td>Power Amplifiers and Building Blocks</td>
<td>35</td>
</tr>
<tr>
<td>20</td>
<td>Body and Brain Interfaces</td>
<td>36</td>
</tr>
<tr>
<td>21</td>
<td>Cryo-Circuits and Ultra-Low-Power Intelligent IoT</td>
<td>37</td>
</tr>
<tr>
<td>22</td>
<td>Frequency Synthesizers</td>
<td>38</td>
</tr>
<tr>
<td>23</td>
<td>Low-Power and UWB Radios for Communication and Ranging</td>
<td>39</td>
</tr>
<tr>
<td>24</td>
<td>Noise-Shaping ADCs</td>
<td>40</td>
</tr>
</tbody>
</table>

**SPECIAL EVENTS**

SE3  Semiconductor Supply Chain............................................................................................. 41
SE4  The Bright and Dark Side of Artificial Intelligence (AI) .............................................. 41

**PAPER SESSIONS**

<table>
<thead>
<tr>
<th>Session</th>
<th>Topic</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>27</td>
<td>mm-Wave &amp; Sub-6GHz Receivers and Transceivers for 5G Radios</td>
<td>42</td>
</tr>
<tr>
<td>28</td>
<td>DRAM and Interface</td>
<td>43</td>
</tr>
<tr>
<td>29</td>
<td>ML Chips for Emerging Applications</td>
<td>44</td>
</tr>
<tr>
<td>30</td>
<td>Power Management Techniques</td>
<td>45</td>
</tr>
<tr>
<td>31</td>
<td>Audio Amplifiers</td>
<td>46</td>
</tr>
<tr>
<td>32</td>
<td>Ultrasound and Beamforming Applications</td>
<td>47</td>
</tr>
<tr>
<td>33</td>
<td>Domain-Specific Processors</td>
<td>48</td>
</tr>
<tr>
<td>34</td>
<td>Hardware Security</td>
<td>49</td>
</tr>
</tbody>
</table>

**FORUMS**

F1  Compute-in-X (CiX): Overcoming the Data Bottleneck in AI Processing .......................... 50
F2  Chip Design for Low-Power, Robust, and Secure IoT Devices ........................................ 51
F3  The Path to 6G: Architectures, Circuits, Technologies for .......................................... 52
F4  Sub-THz Communications, Sensing, and Imaging                                           | 52   |

**SPECIAL EVENTS**

SE5  Shifting Tides of Innovation – Where is Cutting-Edge Research Happening Today? ........ 53
SE6  Next Trillion-Dollar Market............................................................................................... 53

**FORUMS**

F4  Paving the Way to 200Gb/s Transceivers ......................................................................... 54
F5  How to Improve AI Efficiency Further: New Devices, Architectures and Algorithms ........ 55
F6  Computer Systems Under Attack – Paying the Performance Price for Protection  ............ 56

**SHORT COURSE**

SC  High Speed/High Performance Data Converters: ................................................................. 57-59
Metrics, Architectures, and Emerging Topics

Committees .................................................................................................................................... 60-67

Conference Information ............................................................................................................... 68
There are a total of 12 tutorials this year on 12 different topics. Each tutorial, selected through a competitive process within each subcommittee of the ISSCC, presents the basic concepts and working principles of a single topic. These tutorials are intended for non-experts, graduate students and practicing engineers who wish to explore and understand a new topic.

Naveen Verma  
ISSCC Tutorials Chair

The presentations and the videos of all 12 tutorials (90 minutes each) will be available online, on-demand, as of:

**Friday, Feb. 11, 2022, 5:00pm, PST**

**Live Q&A sessions for the tutorials will be available on:**

**Sunday Feb. 20, 2022, 7:00am - 9:00am PST**

20 minute live session = 5 minute summary + 10 minute Q&A + 5 minute break

The Q&A sessions will be recorded and made available after their live sessions.

**Live Q&A - February 20, 7:00am PST**

**T6: Wireless Power Transfer and Management for Medical Applications**  
**Mehdi Kiani, The Pennsylvania State University, University Park, PA**

Wireless technologies play an important role in advanced biomedical systems. Implantable medical devices (IMDs) are a rapidly growing category of bio-systems, where the use of wireless technology is a necessity. This tutorial will present several system- and circuit-level techniques towards the development of novel wireless power-transfer systems with different modalities. Also, novel integrated power-management circuits with voltage and current mode operation will be reviewed.

Mehdi Kiani received his M.S. and Ph.D. degrees in Electrical and Computer Engineering from the Georgia Institute of Technology in 2012 and 2013, respectively. He joined the faculty of the School of Electrical Engineering and Computer Science at the Pennsylvania State University in August 2014 where he is currently an Associate Professor. His research interests are in the multidisciplinary areas of analog, mixed-signal, and power-management integrated circuits, wireless implantable medical devices, neural interfaces, and assistive technologies. He was a recipient of the 2020 NSF CAREER Award. He is currently an Associate Editor of the IEEE Transactions on Biomedical Circuits and Systems and IEEE Transactions on Biomedical Engineering.

**Live Q&A - February 20, 7:20am PST**

**T5: Fundamentals of Process Monitors for Signoff-Oriented Circuit Design**  
**Eric Jia-Wei Fang, MediaTek, Hsinchu City, Taiwan**

In advanced technology nodes, the process technology requires more than a year to reach maturity. To avoid costly iterations between design and foundry, thus impeding time-to-market, the final validation of circuit timing and power, known as chip signoff, should leverage on-chip process monitors to speed-up process learning. This tutorial introduces the relationship between process and signoff in terms of speed/leakage, voltage, temperature and aging. Then, the tutorial covers the different types of digital circuits, with a focus on the corresponding challenges, to monitor this relationship. Since signoff requires a statistical methodology, silicon big-data collection and analysis are described to provide feedback to the foundry and designers.

Eric J.-W. Fang received the B.S. degree in electrical engineering from National Cheng Kung University, Taiwan in 2003, and the M.S. and Ph.D. degrees in electronics engineering from National Taiwan University, Taiwan in 2005 and 2009, respectively. He was a Visiting Scholar with the University of Illinois at Urbana-Champaign, Champaign, USA between 2008 and 2009. He is currently a senior department manager with MediaTek, Inc. and has served as an International Technical Program Committee member for IEEE ISSCC since 2021. His current research interests include digital sensor design with machine-learning technology, digital timing and IR signoff, and chip-package-board co-design. He has published more than 15 technical papers and holds 10 granted US patents.
High-performance systems are challenged by the stringent computational, reliability and availability requirements of emerging cloud-native applications. Unfortunately, efficiency gains through scaling alone have slowed, even as susceptibility to variation-induced system failures have increased, thus necessitating further innovations in energy efficient and reliable processor and system design. This tutorial addresses the following key aspects: how do sources of variations impact design margins and system reliability?; how do self-monitoring systems use sensors to measure ambient environment?; how is environment adaptation actuated in high-volume production systems using a combination of power-delivery and clocking techniques?; what design and analysis techniques can mitigate transient soft errors and hard errors due to transistor aging and interconnect failures?

Shidhartha Das received the M.Sc. and Ph.D. degrees from the University of Michigan, Ann Arbor, MI, USA, in 2003 and 2009, respectively. He is currently a Distinguished Engineer with Arm Ltd., Cambridge, UK where he conducts research in high-performance CPU design, focusing on circuit/micro-architectural techniques for power delivery and variation mitigation. In the past, he has contributed to multiple areas of technology development, including mixed-signal architectures for machine-learning acceleration and emerging non-volatile memories, for which he received the Arm Inventor of the Year award in 2016. He has 58 granted US patents and several more that are pending. He has received multiple best paper awards and his research has been featured in IEEE Spectrum. He serves as the Guest Editor for the IEEE Journal of Solid-State Circuits and Associate Editor for the IEEE Solid-State Circuits Letters.

The noise-shaping (NS) successive-approximation register (SAR) has become a dominant emerging ADC architecture in a short time. Combining the benefits of SAR and noise shaping, NS-SAR ADCs take full advantage of advanced CMOS processes and continue to break records for energy and area efficiency. Along with increasing data rate, NS-SAR ADCs are getting attractive in various applications. This tutorial begins by explaining the basics of the NS SAR. It explores different noise-shaping techniques and introduces approaches for higher-order noise-shaping and high signal-bandwidth designs.

Yun-Shiang Shu (S’05–M’10–SM’19) received the B.S. and M.S. degrees in Electrical Engineering from National Taiwan University, Taiwan, in 1997 and 1999, respectively, and the Ph.D. degree in electrical and computer engineering from University of California at San Diego, CA in 2008. He is currently a Deputy Technical Director at MediaTek Inc., Hsinchu, Taiwan, where he leads the development of biosensors for wearable devices. His published works in ISSCC, VLSI, and JSSC range from flash, pipeline, SAR, to delta-sigma ADCs for communication and sensor interface applications, with a focus on signal processing techniques to compensate for analog circuit imperfections. Dr. Shu was a TPC member of the IEEE Symposium on VLSI Circuits and currently serves as an ITPC member and Far-East Regional Chair for IEEE ISSCC 2022.

Advances in CMOS processes and the spread of GaN FETs are pushing the switching frequency of DC-DC converters beyond 10MHz. Such increase in the switching frequency of the converters results in reducing the size of passive components and increasing the system power density. Starting from the fundamentals of DC-DC buck converters, this tutorial will cover topics including loss analysis and control schemes at high frequencies typically above a few MHz. State-of-the-art design techniques to reduce the switching loss and to drive GaN FETs are also introduced. Finally, topics including recent progress in high-frequency magnetic components and their integration will be covered.
Kousuke Miyaji received the B.S., M.S., and Ph.D. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan, in 2003, 2005, and 2008, respectively. He is currently an Associate Professor in the Department of Electrical and Computer Engineering at Shinshu University. His current research interests include high-frequency DC-DC converters, efficient power-management systems, wireless power transfer systems, and 3D-integration of power magnetic components. Dr. Miyaji has been serving as a TPC member of the International Solid-State Circuits Conference (ISSCC) since 2021.

**Live Q&A - February 20, 8:40am PST**

**T1: Analog Circuit Design in Bipolar-CMOS-DMOS (BCD) Technologies**

Marc Berkhout, *Goodix Technology, Nijmegen, The Netherlands*

Bipolar-CMOS-DMOS (BCD) technologies enable applications of high industrial interest, whereby high-voltage and high-power circuits are combined with high-density digital logic on a single die, as in (audio) power amplifiers and switch-mode power supplies (SMPS). This tutorial addresses challenges of BCD design that are not usually encountered when designing in standard CMOS, e.g. crossing (multiple) voltage domains, parasitic bipolar activity with inductive loads, large operating supply voltage ranges and electrostatic discharge (ESD). The tutorial looks into the structure of BCD technologies and devices, as well as typical circuits, such as power switches, gate drivers, level shifters and bootstraps.

Marc Berkhout received the M.Sc. and the Ph.D. degrees in EE from the University of Twente, The Netherlands, in 1992 and 1996. From 1996 to 2019, he was with Philips/NXP Semiconductors, Nijmegen, The Netherlands. He is currently a fellow with Goodix Technologies, Nijmegen. His main interests are class-D amplifiers and integrated power electronics. Dr. Berkhout was a TPC member of the European Solid-State Circuits Conference (ESSCIRC) from 2008 to 2018 and the International Solid-State Circuits Conference (ISSCC) from 2013 to 2016, and since 2021. He received the ESSCIRC 2002 Best Paper Award and was a plenary invited speaker at the ESSCIRC 2008.

**Live Q&A - February 20, 7:00am PST**

**T12: Advances in Digital vs. Analog AI Accelerators**

Jae-sun Seo, *Arizona State University, Tempe, AZ*

For state-of-the-art AI accelerators, there have been large advances in both all-digital and analog/mixed-signal circuit-based designs. This tutorial presents a practical overview and comparison of recent digital and analog AI accelerators. It will first introduce recent AI algorithms for computer vision and speech applications, which have been targeted for many AI hardware designs. Next, it will present a survey of (i) all-digital AI accelerators, including designs with new dataflow, low precision, and sparsity, and (ii) analog/mixed-signal AI accelerators featuring switch-capacitor circuits and in-memory computing with analog-to-digital converters. The tutorial discusses the key trade-offs of both design approaches including circuit/architecture design, algorithm-mapping flexibility, hardware accuracy and energy efficiency.

Jae-sun Seo received the Ph.D. degree from the University of Michigan in 2010. From 2010 to 2013, he was with IBM T. J. Watson Research Center. In 2014, he joined ASU in the School of Electrical, Computer and Energy Engineering, where he is now an Associate Professor. He was a visiting faculty at Intel Circuits Research Lab in 2015. His research interests include efficient hardware design of machine learning and neuromorphic algorithms. He has authored/co-authored >130 papers and holds >10 issued U.S. patents. He is a recipient of an IBM Outstanding Technical Achievement Award (2012), an NSF CAREER Award (2017), and an Intel Outstanding Researcher Award (2021). He currently serves as an International Technical Program Committee member for ISSCC and an Associate Editor for IEEE Open Journal of the Solid-State Circuits Society (OJ-SSCS).
This tutorial presents basic equalization techniques for high-speed serial interfaces. A simple channel transfer function model will be discussed to explain various channel behaviors. Basic transmitter and receiver equalization techniques such as feed-forward equalization (FFE), continuous-time linear equalization (CTLE), and decision-feedback equalization (DFE) will be covered. Modulation techniques such as non-return-to-zero (NRZ), duo-binary, and pulse-amplitude modulation 4 (PAM-4) will be discussed. Various implementations and design challenges of equalization circuits will be discussed and compared. Various methods of equalization adaptation algorithms will be covered.

Byungsub Kim received the B.S. degree in electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, South Korea, in 2000, and the M.S. and Ph.D. degrees in electrical engineering and computer science from the Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, in 2004 and 2010, respectively. He was an Analog Design Engineer with Intel Corporation, Hillsboro, OR, USA, from 2010 to 2011. In 2012, he joined the Faculty of Department of Electrical Engineering, POSTECH, where he is currently an Associate Professor. Dr. Kim received several honorable awards. He was a recipient of the IEEE Journal of Solid-State Circuits Best Paper Award in 2009. He was a co-recipient of the Beatrice Winner Award for Editorial Excellence at the 2009 IEEE International Solid-State Circuits Conference. He has been serving as a Technical Program Committee Member of IEEE International Solid-State Circuits Conference since 2018.

Millimeter(mm)-Wave phased arrays are becoming a differentiating technology in modern wireless communication and imaging systems. This tutorial will cover key aspects of silicon-based mm-wave phased-array IC design and package integration. It will begin with an overview of the theory and intuition behind phased arrays; it will then discuss different silicon-based phased-array architectures and key phased-array building blocks, including phase shifters, variable-gain amplifiers, combiners, and splitters. Finally, this tutorial will discuss the integration of phased-array ICs with antennas in phased-array antenna modules.

Bodhisatwa Sadhu received the B.E. degree in electrical and electronics engineering from Birla Institute of Technology and Science (BITS) – Pilani, India in 2007, and the Ph.D. degree in Electrical Engineering from the University of Minnesota, Minneapolis, in 2012. He is currently a Research Scientist at IBM T. J. Watson Research Center, NY, and an Adjunct Assistant Professor at Columbia University, NY. At IBM, he led the design of the world’s first reported silicon-based 5G phased array IC. He has authored/co-authored 50+ papers, a book, and several book chapters, and holds 50+ issued U.S. patents. He is the recipient of multiple awards including the 2017 ISSCC Lewis Winner Award for Outstanding Paper and the 2017 JSSC Best Paper Award. He is an MTT-S Distinguished Microwave Lecturer, and serves on the steering committee of IEEE RFIC Symposium, and the ITPC of IEEE ISSCC.
Sriram Vangal received the B.E. degree from Bangalore University, India, in 1993, the M.S. degree from the University of Nebraska, Lincoln, USA in 1995, and the Ph.D. degree from Linköping University, Sweden in 2007 – all in Electrical Engineering. He joined Intel Corporation in 1995 and has played a lead role in multi-core CPU development and ultra-low power silicon research. Sriram is a Principal Engineer with Intel Labs researching sustainable net-zero energy computing. Sriram has received two Intel Achievement Awards for his work, is an IEEE senior member and has published over 35 conference and journal papers, has authored three book chapters, and has over 30 issued patents.

Live Q&A - February 20, 8:20am PST
T8: Fundamentals of Mixed-Mode RF Transceivers
Jeff Walling, Virginia Tech, Blacksburg, VA

RF systems that directly interface between digital bits and RF front-ends are rapidly gaining interest as the number of transceivers in mobile systems is increasing. This tutorial will review the concepts of direct digital-to-RF conversion and focus on the analysis and design of digital transceiver building blocks, such as switched capacitor RF-DACs, current-mode RF-DACs, and directly quantized receiver circuits. The tutorial will focus on the practical implementation of these circuit blocks using theoretical predictions.

Jeff Walling received his PhD degree from the University of Washington in 2008 and has been actively engaged in research and product design in the wireless industry for 20 years. While a student and intern at Intel Research, he was an early pioneer in digital friendly and mixed-mode transceiver systems and has continued to lead innovation in the field, particularly with the introduction of the switched-capacitor power amplifier. He has published >70 journal and conference papers and has twice won outstanding department teaching awards at Rutgers University and the University of Utah. He was in the corporate R&D group at Qualcomm and the AI solutions sector at Skyworks. Since the Fall of 2021, he is an Associate Professor in the ECE department at Virginia Tech. His research is focused on efficient radio architectures from RF-to-THz for next generation communication networks.

Live Q&A - February 20, 8:40am PST
T7: HBM DRAM and 3D Stacked Memory
Dong Uk Lee, SK hynix, Icheon-si, Korea

The proliferation of machine-learning workloads has accelerated the demand for higher memory bandwidth in modern systems. HBM DRAM was developed to break through the system-performance limit caused by memory bandwidth. With advanced packaging technology, HBM has been the only scalable DRAM bandwidth solution of the past 10 years, starting from 128GB/s and now extending beyond 800GB/s. This tutorial will cover HBM, HBM2, and HBM3 architectures; it will also cover historical trends and state-of-the-art for DRAM. Electrical interfaces and PDN for 2.5D system-in-package (SiP) structures will be reviewed, along with heterogeneous memory structures, including TSV interfaces. This tutorial will also cover the various design methods such as known-good-stack verification, self-repair, MBIST and RAS features, to deal with the new package structures. Finally, advanced 3D memory architectures including future trends of HBM, will be introduced.

Dong Uk Lee is Principal Engineer of SK hynix. He was the Lead Engineer of the industry’s first HBM DRAM development and standardization from 2011 to 2013. He received the B.S. and M.S. degrees in electronics from Hanyang University, Seoul, Korea, in 1996 and 2001. He joined Hynix in 2001, and has developed 16 commodity DRAMs, including graphics DRAM, computing DRAM, HBM, HBM2E and HBM3. He holds 70 US patents. He is the author of 8 ISSCC and 2 JSSC, from 2006 to 2020. He presented an invited paper at CICC 2015, and he was a forum presenter at ISSCC 2016. Mr. Lee received the Medal of Honor for outstanding contribution to the semiconductor industry from the Government of Korea in 2021. Since 2017, he has been serving as a member of the ISSCC Technical Program Committee.
The Student Research Preview (SRP) will highlight selected student research projects in progress. The SRP consists of 90 second presentations followed by a Poster Session, by graduate students from around the world, which have been selected on the basis of a short submission concerning their on-going research. Selection is based on the technical quality and innovation of the work. This year, the SRP will be presented in two theme sections: Digital and Machine-Learning; Analog and Radio.

The Student Research Preview will include a Distinguished Lecture by Prof. Kofi Makinwa, Delft University of Technology. SRP is open to all ISSCC registrants.

**SRP Session (8:30 AM – 10:30 AM)**

- **8:30 AM:** Introductory Remarks
- **8:35 AM:** Awards
  - Silk Road Award
  - SSCS Pre-Doctoral Fellowship Award
  - ISSCC Student Travel Grant
- **8:45 AM:** Distinguished Speaker Talk
  (pre-recorded)
  - “First Time Right!” by Prof. Kofi Makinwa, Delft University of Technology
- **9:00 AM - 9:30 AM:** 90 Second Presentations
  (pre-recorded)
- **9:30 AM - 10:30 AM:** Posters
  (Gathertown)

**SRP Organizing Committee**

- **Co-Chair:** Jerald Yoo
  - National University of Singapore, Singapore
- **Co-Chair:** Mondira Pant
  - Intel, MA
- **Advisor:** Anantha Chandrakasan
  - MIT
- **Advisor:** Kevin Zhang
  - TSMC
- **Advisor:** Jan Van der Spiegel
  - University of Pennsylvania
- **Media/Publications:** Laura Fujino
  - University of Toronto
- **A/V:** Trudy Stetzler
  - Halliburton, Houston, TX

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- Masoud Babaie, Delft University of Technology, Netherlands
- Utsav Banerjee, Indian Institute of Science, India
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- Po-Hung Chen, National Chiao Tung University, Taiwan
- Zeynep Deniz, IBM, NY
- Hao Gao, Eindhoven University of Technology, Netherlands
- Minkyu Je, KAIST, Korea
- Matthias Kuhl, Hamburg University of Technology, Germany
- Seulki Lee, IMEC-NL, Netherlands
- Yoonmyung Lee, SungKyunKwan University, Korea
- Shih-Chii Liu, University of Zurich/ETH Zurich, Switzerland
- Carolina Mora Lopez, imec, Belgium
- Noriyuki Miura, Osaka University, Japan
- Phillip Nadeau, Analog Devices, MA
- Mondira Pant, Intel, MA
- Negar Reiskarimian, MIT, MA
- Jae-sun Seo, Arizona State University, AZ
- Atsushi Shirane, Tokyo Institute of Technology, Japan
- Mahsa Shoaran, EPFL, Switzerland
- Yildiz Sinangil, Apple, CA
- Mahmut Sinangil, TSMC, CA
- Filip Tavernier, KU Leuven, Belgium
- Chia-Hsiang Yang, National Taiwan University, Taiwan
- Lita Yang, Microsoft, CA
- Rabia Tugce Yazicigil, Boston University, MA
- Jerald Yoo, National University of Singapore, Singapore
- Milin Zhang, Tsinghua University, China
SE2:
Morning Session: Next Generation Circuit Designer 2022 Workshop

Chair: Yildiz Sinangil, Apple, Cupertino, CA
Co-Chair: Sophia Shao, UC Berkeley, Berkeley, CA
Co-Chair: Alice Wang, Everactive, Plano, TX

Workshop Committee:
Abira Alvater, IEEE-SSCS, Piscataway, NJ
Aya G. Amer, MIT, Cambridge, MA
Zeynep Deniz, IBM Research, Yorktown Heights, NY
Najme Ebrahimi, University of Florida, Gainesville, FL
Dina Reda El-Damak, University of Science and Technology at Zewail City, Egypt
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Q. Jane Gu, University of California Davis, CA
Ulkuhan Guler, Worcester Polytechnic Institute, Worcester, MA
Yaoyao Jia, University of Austin, Austin, TX
Awani Khodkumbhe, University of California, Berkeley, CA
Rabia Tugce Yazicigil, Boston University, Boston, MA
Alicia Klinefelter, NVIDIA, Durham, NC
Deeksha Lal, Anokiwave, Billerica, MA
Jiamin Li, National University of Singapore, Singapore
Farhana Sheikh, Intel, Hillsboro, OR
Trudy Stetzler, Halliburton, Houston, TX
Vivienne Sze, MIT, Cambridge, MA
Kathy Wilcox, AMD, Boxborough, MA

Advisory Board:
Anantha Chandrakasan, MIT, Cambridge, MA

The IEEE SSCS Women in Circuits together with ISSCC will be co-sponsoring the first “Next Generation Circuit Designer 2022” for young professionals and students. This is a virtual educational workshop for a diverse set of graduate and undergraduate students, and young professionals who have graduated with B.S. within the last two years, who are interested in learning how to excel at academic and industry careers in computer science and computer and electrical engineering.

The panel on “Our Path to Circuit Design”, with panelists from diverse regions, backgrounds and career levels, will touch upon topics such as:

- networking and mentoring,
- choosing or changing a career path, a research topic, or an advisor,
- time management, work-life balance, and mental and physical well-being,
- managing day-to-day life in both graduate school and industry,
- dealing with challenges and conflict, and more.

In addition to the panel, we will be selecting forty next generation circuit designers in academia and industry to attend a keynote from a distinguished speaker, an informal fireside chat with a high-profile leader in the field, and participate in an elevator pitch. The selected designers will also get the opportunity for networking and mentoring through virtual events leading up to the workshop. The morning virtual event will be followed by an optional evening in-person event, which will include further networking opportunities.
SE2:
IEEE SSCS WiC Next Generation Circuit Designer 2022

7:00AM – 7:10AM: Workshop Opening and Introduction
Yildiz Sinangil, Apple, Cupertino, CA
Alice Wang, Everactive, Plano, TX
Sophia Shao, University of Berkeley, Berkeley, CA

7:10AM – 7:20AM: Video - "Advice to Next Generation Circuit Designers", presented by Kathy Wilcox, AMD, Boxborough, MA

7:20AM – 8:00AM: Fireside Discussion with
Megan Smith, United States Chief Technology Officer (CTO) of the United States

Introduction and Facilitator:
Rabia Tugce Yazicigil, Boston University, Boston, MA

8:05AM – 9:00AM: Next Generation Circuit Designers Elevator Pitch
Introduction and Facilitator:
Deeksha Lal, Anokiwave, Billerica, MA
Najme Ebrahimi, University of Florida, Gainesville, FL

The selected next generation circuit designers will have the chance to give an elevator pitch to the attendees.

9:05AM – 9:45AM: Special Talk by Tsu-Jae King Liu, Dean of the College of Engineering at the University of California, Berkeley, CA

Introduction and Facilitator:
Alicia Klinefelter, NVIDIA, Durham, NC

9:50AM – 10:50AM: Our Path To Circuit Design Panel
Panel Moderator:
Dina Reda El-Damak, University of Science and Technology at Zewail City, Egypt

The panel on “Our Path to Circuit Design”, with panelists from diverse regions, backgrounds and career levels, will touch upon topics such as:

- networking and mentoring,
- choosing or changing a career path, a research topic, or an advisor,
- time management, work-life balance, and mental and physical well-being,
- managing day-to-day life in both graduate school and industry,
- dealing with challenges and conflict, and more.

Panelists:
Alvin Loke, NXP, San Jose, CA
Andreia Cathelin, ST Microelectronics, Grenoble, France
Canan Dagdeviren, MIT, Cambridge, MA
Ada Poon, Stanford University, Stanford, CA
Brian Floyd, North Carolina State University, Raleigh, NC
Plenary Session I — Invited Papers

Session Chair: Kevin Zhang, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan
ISSCC Conference Chair

Session Co-Chair: Edith Beigné, Meta, Menlo Park, CA
ISSCC International Technical Program Chair

6:45 AM
FORMAL OPENING OF THE CONFERENCE

7:00 AM

1.1 Catalysts of the Impossible: Silicon, Software, and Smarts for the Era of SysMoore
Aart de Geus, Chairman & Co-CEO, Synopsys, Mountain View, CA

As we confront global scale challenges with immense intertwined datasets, the distillation of usable insights will require an exponential increase in AI processing capability. The impossibility horizon – sustained by the slowing of Moore’s Law – will be pierced by rapid advancements in materials, devices, software, and architecture (the ‘SysMoore’ era). Autonomous design instruments – super-tools fusing together hundreds of algorithms precision-guided by AI – are unlocking opportunity for circuit designers ushering in a new wave of architectural vitality.

In the follow up to ‘Builders of the Imaginary’, we will unveil the next chapter in autonomous design, piecing together a new breed of super-monolithic devices, dense interconnects, and chiplets, into software-defined, heterogeneous architectures.

7:45 AM

1.2 Intelligent Sensing: Enabling the Next “Automation Age”
Marco Cassis, President, Analog, MEMS and Sensors Group
Head of STMicroelectronics’ Strategy, System Research and Applications, Innovation Office, Geneva, Switzerland / Tokyo, Japan

Sensors have undergone extraordinary proliferation since the beginning of the 21st Century. Thanks to IoT, connected smart sensors can now be found all around us. This makes it possible to collect a wealth of data autonomously and continuously without human intervention, automating routine activities while unlocking previously unattainable insights and functionality. As we enter the Automation Age, the information generated from these sensors can be processed and acted on locally to take action in the physical world.

Sensing, artificial intelligence, and actuation will enable autonomous end-to-end system solutions in existing and new application fields including automotive, digital health, agriculture, environmental control, and decarbonization. The Semiconductor Industry is driving this transformation and sensors, smart embedded actuators, analog interfaces, connectivity, security and embedded AI, offer a perfect toolset for companies to continue to innovate. To fuel this innovation, we need to develop energy-efficient, high-accuracy, autonomous, ultra-compact, and trusted ICs. These chips need to feature state-of-the-art system and embedded security techniques to protect the gathered data, its processing and the resulting actuation. New and super-efficient computational hardware technologies supporting AI and machine learning are already transforming at-the-edge data processing and are pushing the envelope on intelligent functionality and IoT network scalability.

Future advances will rely on these evolving IC technologies as well as associated packaging solutions. These will include super-integration, wafer-to-wafer bonding, and system-in-package, to enable the heterogenous integration of multiple technologies.
Processors
Session Chair: Hugh Mair, Mediatek, Fairview, TX
Session Co-Chair: Shidhartha Das, ARM, Cambridge, United Kingdom

8:30 AM
2.1 Ponte Vecchio: A Multi-Tile 3D Stacked Processor for Exascale Computing
W. Gomes1, A. Koker2, P. Stover3, D. Ingerly1, S. Siers2, S. Venkataraman1, C. Pelto1, T. Shah2, A. Rao3, F. O’Mahony1, E. Kari1, L. Cheney2, I. Rajwan3, H. Jain1, R. Cortez2, A. Chandrasekhar4, B. Kanthi5, R. Koduri6, Intel, Portland, OR; 1Intel, Folsom, CA; 3Intel, Chandler, AZ; 4Intel, Bengaluru, India; 5Intel, Austin, TX; 6Intel, Santa Clara, CA

8:40 AM
2.2 Sapphire Rapids: The Next-Generation Intel Xeon Scalable Processor
N. Nassif1, A. O. Munch1, C. L. Molnar1, G. Pasdast2, S. V. Iyer3, Z. Yang1, Q. Mendoza1, M. Huddart1, S. Venkataraman2, R. Marom4, A. M. Kern1, B. Bowhill5, D. R. Mulvihill5, S. Nimmagadda3, V. Kalidindi1, J. Krause1, M. M. Haq1, R. Sharma1, K. Duda1, Intel, Hudson, MA; 1Intel, Santa Clara, CA
2Intel, Bangalore, India; 4Intel, Haifa, Israel; 5Intel, Fort Collins, CO

8:50 AM
2.3 IBM Telum: A 16-Core 5+ GHz DCM
O. Geva1, C. Berry1, R. Sonnelitter1, D. Wolpert1, A. Collura1, T. Strach2, D. Phan3, C. Lichtenaus3, A. Buyuktosunoglu4, H. Harrer1, J. Zitz1, C. Marquart1, D. Malone1, T. Weber5, A. Jakowski1, J. Isakson1, D. Hamid1, M. Cichanski1, M. Romain1, F. Hasen1, K. Williams1, J. Surprise1, C. Cavitt1, M. Cohen1
1IBM Systems and Technology, Poughkeepsie, NY; 2IBM Systems and Technology, Boeblingen, Germany; 3IBM Research, Yorktown Heights, NY; 4IBM Systems and Technology, Austin, TX

9:00 AM
2.4 POWER10™: A 16-Core SMT8 Server Processor with 2TB/s Off-Chip Bandwidth in 7nm Technology
R. M. Rao1, C. Gonzalez2, E. Fluhr3, A. Mathews3, A. Bianchi3, D. Dreps3, D. Wolpert4, E. Lai5, G. Strevig1, G. Wiedemeier1, P. Saltz6, R. Kruse1, IBM, Bengaluru, India; 1IBM, Yorktown Heights, NY; 2IBM, Austin, TX; 3IBM, Poughkeepsie, NY; 4IBM, Boblingen, Germany

9:10 AM
2.5 A 5nm 3.4GHz Tri-Gear ARMv9 CPU Subsystem in a Fully Integrated 5G Flagship Mobile SoC
A. Nayak1, H. Chen1, H. Mail1, R. Lagerquist1, T. Chen1, A. Rajagopalan1, G. Gammie1, R. Madhavaram1, M. Jagota1, C. Chung1, J. Wiedemeier1, B. Meera1, C-Y. Yeh1, M. Lin2, C. Lin2, V. Lin2, J. Lin2, Y. Chen2, B. Chen2, C-Y. Wu2, R. ChangChien3, R. Tzeng3, K. Yang2, A. Thippana1, E. Wang2, S. Hwang2
1MediaTek, Austin, TX; 2MediaTek, Hsinchu, Taiwan

9:20 AM
2.6 A 16nm 785GMACs/J 784-Core Digital Signal Processor Array with a Multilayer Switch Box Interconnect, Assembled as a 2×2 Dielet with 10μm-Pitch Inter-Dielet I/O for Runtime Multi-Program Reconfiguration
U. Rathore*, S. S. Nagi*, S. Iyer, D. Marković, *Equally-Credited Authors (ECAs)
University of California, Los Angeles, CA

9:30 AM
2.7 Zen3: The AMD 2nd-Generation 7nm x86-64 Microprocessor Core
T. Burdi1, W. Li2, J. Pistole1, S. Venkataraman1, M. McCabe1, T. Johnson1, J. Vint1, T. Yu1, M. Wasio1, H-H. Wong1, D. Liu1, J. White2, B. Munger2, J. Lindner2, J. Olson2, S. Bakke2, J. Sniderman2, C. Henrion3, R. Schreiber4, E. Busta1, B. Johnson1, T. Jackson3, A. Miller3, R. Miller3, M. Pickett5, A. Horiuichi5, J. Dvorak3, S. Balagangadharan3, S. Ammikkalilinga5, P. Kumar5
1AMD, Santa Clara, CA; 2AMD, Boxborough, MA; 3AMD, Fort Collins, CO; 4AMD, Austin, TX; 5AMD, Bangalore, India
Analog Techniques & Sensor Interfaces
Session Chair: Viola Schaffer, Texas Instruments, Freising, Germany
Session Co-Chair: Jiawei Xu, Fudan University, Shanghai, China

8:30 AM

3.1 A Single-Crystal-Oscillator-Based Clock-Management IC with 18× Start-Up Time Reduction and 0.68ppm/°C Duty-Cycled Machine-Learning-Based RCO Calibration
J. Jung, S. Oh, J. Kim, G. Ha, J. Lee, S. Kim, E. Park, J. Lee, Y. Yoon, S. Bae, W. Kim, Y. Lim, K. Lee, J. Huh, J. Lee, T. B. Cho
Samsung Electronics, Hwaseong, Korea

8:40 AM

3.2 A 52MHz -158.2dBc/Hz PN @ 100kHz Digitally Controlled Crystal Oscillator Utilizing a Capacitive-Load-Dependent Dynamic Feedback Resistor in 28nm CMOS
J. Jung, S. Kim, W. Kim, J. Han, E. Park, S. Hwang, S. Oh, S. Han, K. Lee, J. Huh, J. Lee
Samsung Electronics, Hwaseong, Korea

8:50 AM

3.3 A 174μVrms Input Noise, 1GS/s Comparator in 22nm FDSOI with a Dynamic-Bias Preamp Amplifier Using Tail Charge Pump and Capacitive Neutralization Across the Latch
H. S. Bindra, J. Ponte, B. Nauta
University of Twente, Enschede, The Netherlands

9:00 AM

3.4 A Second-Order Temperature-Compensated On-Chip R-RC Oscillator Achieving 7.93ppm/°C and 3.3pJ/Hz in -40°C to 125°C Temperature Range
Y. Ji1, J. Liao2, S. Arjmandpour1,2, A. Novello1, J-Y. Sim2, T. Jang1
1ETH Zürich, Zürich, Switzerland
2Pohang University of Science and Technology, Pohang, Korea
3Sharif University of Technology, Tehran, Iran

9:10 AM

3.5 A ±25A Versatile Shunt-Based Current Sensor with 10kHz Bandwidth and ±0.25% Gain Error from −40°C to 85°C Using 2-Current Calibration
Z. Tang1, R. Zamparette1, Y. Furuta2, T. Nezuka2, K. A. A. Makinwa1
1Delft University of Technology, Delft, The Netherlands
2MIRISE Technologies, Aichi, Japan

9:20 AM

3.6 A MEMS Coriolis-Based Mass-Flow-to-Digital Converter with 100μg/h/√Hz Noise Floor and Zero Stability of ±0.35mg/h
A. C. de Oliveira, S. Pan, K. A. A. Makinwa
Delft University of Technology, Delft, The Netherlands

9:30 AM

3.7 A 2.6mW 10pT/√Hz 33kHz Magnetoimpedance-Based Magnetometer with Automatic Loop-Gain and Bandwidth Enhancement
I. Akita1, T. Kawano2, H. Aoyama2, S. Tatematsu2, M. Hioki1
1Advanced Industrial Science and Technology (AIST), Tsukuba, Japan
2Aichi Steel, Tohkai, Japan

9:40 AM

3.8 A BJT-Based CMOS Temperature Sensor Achieving an Inaccuracy of ±0.45°C (3σ) from -50°C to 180°C and a Resolution-FoM of 7.2pJ-K² at 150°C
B. Wang1, M-K. Law2, A. Bermak1
1Hamad Bin Khalifa University, Doha, Qatar
2University of Macau, Macau, China
mm-Wave and Sub-THz ICs for Communication and Sensing

Session Chair: Yiwu Tang, Qualcomm Technologies, San Diego, CA
Session Co-Chair: Ho-Jin Song, POSTECH, Pohang, Korea

8:30 AM

4.1 Fully Integrated 2D Scalable TX/RX Chipset for D-Band Phased-Array-on-Glass Modules

M. Elkhouly¹, J. Ha², M. J. Holyoak¹, D. Hendry², M. Sayginer¹, R. Enright¹, I. Kimionis¹, Y. Baeyens¹, S. Shahramanian¹
¹Nokia Bell Labs, New Providence, NJ; ²now with L3 Harris, Queensland, Australia

8:40 AM

4.2 A Fully Integrated 160Gb/s D-Band Transmitter with 1.1pJ/b Efficiency in 22nm FinFET Technology

S. Callender*¹, A. Whitcombe*², A. Agrawal*¹, R. Bhat³, M. Rahman³, C. C. Lee⁴, P. Sagazios⁵, G. Dogiamis⁶, B. Carlton¹, M. Chakravorti², S. Pellerano¹, C. Hull³, *Equally-Credited Authors (ECAs)
¹Intel, Hillsboro, OR; ²Intel, Santa Clara, CA; ³now with IIT Delhi, New Delhi, India
⁴now with Nebula Microsystems, Richardson, TX; ⁵Intel, Chandler, AZ

8:50 AM

4.3 A 140GHz Transceiver with Integrated Antenna, Inherent-Low-Loss Duplexing and Adaptive Self-Interference Cancellation for FMCW Monostatic Radar

X. Chen¹, M. I. W. Khan¹, X. Yi²,², X. Li²,³, W. Chen³, J. Zhu³, Y. Yang³, K. E. Kolodziej⁴, N. M. Monroe¹, R. Han¹
¹Massachusetts Institute of Technology, Cambridge, MA
²South China University of Technology, Guangzhou, China; ³Tsinghua University, Beijing, China
⁴University of Technology Sydney, Ultimo, Australia; ⁵MIT Lincoln Laboratory, Lexington, MA

9:00 AM

4.4 A 23-to-29GHz Receiver with mm-Wave N-Input-N-Output Spatial Notch Filtering and Autonomous Notch-Steering Achieving 20-to-40dB mm-Wave Spatial Rejection and -14dBm In-Notch IP1dB

L. Zhang, M. Babaie, Delft University of Technology, Delft, The Netherlands

9:10 AM

4.5 Electronic THz Pencil Beam Forming and 2D Steering for High Angular-Resolution Operation: A 98×98-Unit 265GHz CMOS Reflectarray with In-Unit Digital Beam Shaping and Squint Correction

N. M. Monroe¹, G. C. Dogiamis², R. Stingel², P. Myers², X. Chen¹, R. Han¹
¹Massachusetts Institute of Technology, Cambridge, MA; ²Intel Corporation, Chandler, AZ

9:20 AM

4.6 A 430GHz CMOS Concurrent Transceiver Pixel Array for High Angular Resolution Reflection-Mode Active Imaging

Y. Zhu¹, P. R. Byreddy¹, S. Dong¹, K. K. O¹, W. Cho²
¹University of Texas at Dallas, Richardson, TX; ²Oklahoma State University, Stillwater, OK

9:30 AM

4.7 A 300GHz 52mW CMOS Receiver with On-Chip LO Generation

O. Memioglu, Y. Zhao, B. Razavi, University of California, Los Angeles, CA

9:40 AM

4.8 A 3.4mW/element Radiation-Hardened Ka-Band CMOS Phased-Array Receiver Utilizing Magnetic-Tuning Phase Shifter for Small Satellite Constellation

Tokyo Institute of Technology, Tokyo, Japan
Imagers, Range Sensors and Displays

Session Chair: Mutsumi Hamaguchi, Sharp, Tenri, Japan
Session Co-Chair: Seong-Jin Kim, Ulsan National Institute of Science and Technology, Ulsan, Korea

8:30 AM

5.1 A 0.37W 143dB-Dynamic-Range 1Mpixel Backside-Illuminated Charge-Focusing SPAD Image Sensor with Pixel-Wise Exposure Control and Adaptive Clocked Recharging

8:40 AM

5.2 A 64×64-Pixel Flash LiDAR SPAD Imager with Distributed Pixel-to-Pixel Correlation for Background Rejection, Tunable Automatic Pixel Sensitivity and First-Last Event Detection Strategies for Space Applications
E. Manuzzato1, A. Tontini1, A. Seljak2, M. Perenzoni2
1Fondazione Bruno Kessler, Trento, Italy; 2Jozef Stefan Institute, Ljubljana, Slovenia

8:50 AM

5.3 An 80×60 Flash LiDAR Sensor with In-Pixel Histogramming TDC Based on Quaternary Search and Time-Gated Δ-Intensity Phase Detection for 45m Detectable Range and Background Light Cancellation
S. Park1, B. Kim1, J. Cho2, J-H. Chun2,3, J. Cho2,3, S-J. Kim1
1Ulsan National Institute of Science and Technology, Ulsan, Korea; 2SolidVue, Suwon, Korea
3Sungkyunkwan University, Suwon, Korea

9:00 AM

5.4 A 38μm Range Precision Time-of-Flight CMOS Range Line Imager with Gating Driver Jitter Reduction Using Charge-Injection Pseudo Photocurrent Reference
K. Yasutomi, T. Furuhashi, K. Sagawa, T. Takasawa, K. Kagawa, S. Kawahito
Shizuoka University, Hamamatsu, Japan

9:10 AM

5.5 A 1/1.57-inch 50Mpixel CMOS Image Sensor with 1.0μm All-Directional Dual Pixel by 0.5μm-Pitch Full-Depth-Trench Isolation Technology
Samsung Electronics, Hwasung, Korea

9:20 AM

5.6 A 4.9Mpixel Programmable-Resolution Multi-Purpose CMOS Image Sensor for Computer Vision
H. Murakami1, E. Bohannon1, J. Childs1, G. Gui1, E. Moule1, K. Hanzawa1, T. Koda1, C. Takano2, T. Shimizu1, Y. Takiwaza1, A. Basavalingappa1, R. Childs1, C. Cziesler1, R. Jarrott1, K. Nishimura1, S. Rogerson1, Y. Nitta1
1Sony Electronics, San Jose, CA; 2Sony Semiconductor Solutions, Atsugi, Japan
3Sony LSI Design, Atsugi, Japan

9:30 AM

5.7 A Fully Digital Time-Mode CMOS Image Sensor with 22.9pJ/frame-pixel and 92dB Dynamic Range
S. Kim, T. Kim, K. Seo, G. Han, Yonsei University, Seoul, Korea

9:40 AM

5.8 A 64Mpixel CMOS Image Sensor with 0.56μm Unit Pixels Separated by Front Deep-Trench Isolation

9:50 AM

5.9 A 10b Source-Drive IC with LSB-Stacked LV-to-HV-Amplify DAC Achieving
G-W. Lim1, G-G. Kang1, H. Ma2, M. Jeong2, H-S. Kim1
1KAIST, Daejeon, Korea; 2Samsung Display, Yongin, Korea
SESSION 6 Live Q&As
Monday February 21st, 8:30 AM PST

Ultra-High-Speed Wireline
Session Chair: Thomas Toifl, Cisco Systems, Thalwil, Switzerland
Session Co-Chair: Amir Amirkhany, Samsung Display America Lab, San Jose, CA

8:30 AM

6.1 A 1.41pJ/b 224Gb/s PAM-4 SerDes Receiver with 31dB Loss Compensation
Y. Segal1, A. Laufer1, A. Khairi1, Y. Krupnik1, M. Cusmai1, I. Levin1, A. Gordon1, Y. Sabag1, V. Rahinski1, G. Ori1, N. Familia1, S. Litski1, T. Warshavsky1, U. Virobnik1, Y. Horwitz1, A. Balankutty1, S. Kiran2, S. Palermo3, P. M. Li4, A. Cohen1
1Intel, Jerusalem, Israel; 2Intel, Hillsboro, OR; 3Texas A&M University, College Station, TX; 4Intel, San Jose, CA

8:40 AM

6.2 A 112.5Gb/s ADC-DSP-Based PAM-4 Long-Reach Transceiver with >50dB Channel Loss in 5nm FinFET
Z. Guo1, A. Mostafa1, A. Elshazly1, B. Chen1, B. Wang1, C. Han1, C. Wang1, D. Zhou1, D. Visani1, E. Hsiao1, F. Chuu1, F. Lu1, G. Cui1, H. Zhang1, H. Wang1, H. Zhao1, J. Lin1, J. Gu1, L. Luo2, L. Jiang1, M. Singh1, M. Gambhir1, M. Hasan1, M. Wu1, M. J. Yoo2, P. Liu1, S. Kollu1, T. Ye2, X. Zhao2, X. Yang1, Y. Huang1, X. Han1, Y. Sun1, Z. Yu1, Z. H. Jiang1, Z. Adal1, Z. Yan1
1Marvell, Santa Clara, CA; 2Marvell, Shanghai, China

8:50 AM

6.3 A 2.29pJ/b 112Gb/s Wireline Transceiver with RX 4-Tap FFE for Medium-Reach Applications in 28nm CMOS
Peking University, Beijing, China

9:00 AM

6.4 An 182mW 1-60Gb/s Configurable PAM-4/NRZ Transceiver for Large Scale ASIC Integration in 7nm FinFET Technology
N. Kocaman1, U. Singh1, B. Raghavan1, A. Iyer1, K. Thasari1, S. Surana1, J. W. Jung1, J. Jeong1, H. Zhang1, A. Vasan1, Y. Shim1, Z. Huang1, A. Garg1, H-B. Lee1, B. Wu2, F. Liu1, R. Wang1, M. Loh2, A. Wang2, M. Caresosa1, B. Zhang1, A. Moortz1
1Broadcom, Irvine, CA; 2Broadcom, San Jose, CA

9:10 AM

6.5 A 1.6Tb/s Chiplet over XSR-MCM Channels using 113Gb/s PAM-4 Transceiver with Dynamic Receiver-Driven Adaptation of TX-FFE and Programmable Roaming Taps in 5nm CMOS
G. Gangasani1, D. Hanson1, D. Storaska1, H. H. Xu1, M. Kelly1, M. Shannon1, M. Sorna1, M. Wielgos1, P. B. Ramakrishna2, S. Shi1, S. Parker1, U. K. Shukla1, W. Kelly1, W. Su2, Z. Yu2
1Marvell, Hopewell Junction, NY; 2Marvell, Bangalore, India; 3Marvell, Shanghai, China; 4Marvell, Santa Clara, CA

9:20 AM

6.6 A 1-58.125Gb/s, 5-33dB IL Multi-Protocol Ethernet-Compliant Analog PAM-4 Receiver with 16 DFE Taps in 10nm
Intel, Toronto, Canada

9:30 AM

6.7 A 50Gb/s PAM-4 Bi-Directional Plastic Waveguide Link with Carrier Synchronization
H-I. Song1, H. Choi2, J. Y. Yoo1, H-S. Won1, C. M. Lee1, H. Jin1, T. Y. Kim1, W. Kwon2, K. Lim1, K. Kwon1, C-A. Kim1, T. Kim1, J. G. Jo1, J. Eu1, S. Park1, H-M. Bae2
1Point2 technology, Seoul, Korea; 2KAIST, Daejeon, Korea
**SESSION 7 Live Q&As**  
Monday February 21st, 8:30 AM PST

**NAND Flash Memory**  
Session Chair: Violante Moschiano, Micron Semiconductor, Avezzano, Italy  
Session Co-Chair: Seung-Jae Lee, Samsung, Hwasung-si, Kyeonggi-do, Korea

### 8:30 AM

**7.1 A 1-Tb 4b/Cell 4-Plane 162-Layer 3D Flash Memory with a 2.4-Gb/s I/O Speed Interface**  
J. Yuh\(^1\), J. Li\(^1\), H. Li\(^1\), Y. Oyama\(^1\), C. Hsu\(^1\), P. Anantula\(^1\), S. Jeong\(^1\), A. Amarnath\(^1\), S. Darne\(^1\), S. Bhatia\(^1\), T. Tang\(^1\), A. Arya\(^1\), N. Rastogi\(^1\), N. Okumura\(^1\), H. Mizukoshi\(^2\), A. Yap\(^1\), D. Wang\(^1\), S. Kim\(^1\), Y. Wu\(^1\), M. Peng\(^1\), J. Lu\(^1\), T. Ip\(^1\), S. Malhotra\(^1\), D. Han\(^1\), M. Okumura\(^1\), J. Liu\(^1\), J. Sohn\(^1\), H. Chibvongodze\(^1\), M. Balaga\(^1\), A. Matsuda\(^1\), C. Puri\(^1\), C. Chen\(^1\), I. K V\(^1\), C. Gi\(^1\), V. Ramachandra\(^1\), Y. Kato\(^1\), R. Kumar\(^1\), H. Wang\(^1\), F. Moogat\(^1\), I. Yoon\(^1\), K. Kanda\(^2\), T. Shimizu\(^2\), N. Shibata\(^2\), T. Shigeoka\(^2\), K. Yanagidaira\(^2\), T. Kodama\(^2\), R. Fukuda\(^2\), Y. Hirashima\(^2\), M. Abe\(^2\)  
\(^1\)Western Digital, Milpitas, CA  
\(^2\)KIOXIA Corporation, Yokohama, Japan

### 8:40 AM

**7.2 A 1-Tb Density 4b/Cell 3D-NAND Flash on 176-Tier Technology with 4-Independent Planes for Read using CMOS-Under-the-Array**  
T. Pekny\(^1\), L. Vu\(^1\), J. Tsai\(^1\), D. Srinivasan\(^1\), E. Yu\(^1\), J. Babustan\(^1\), J. Xu\(^1\), S. Deshmukh\(^1\), K-F. Chan\(^1\), M. Piccardi\(^1\), K. Xu\(^1\), G. Wang\(^1\), K. Shakeri\(^1\), V. Patel\(^1\), T. Iwasaki\(^2\), T. Wang\(^1\), P. Musunuri\(^1\), C. Gu\(^1\), A. Mohammadzadeh\(^1\), A. Ghalam\(^1\), V. Moschiano\(^2\), T. Vali\(^2\), J. Park\(^1\), J. Lee\(^1\), R. Ghods\(^2\)  
\(^1\)Micron Technology, San Jose, CA  
\(^2\)Micron Technology, Avezzano, Italy

### 8:50 AM

**7.3 A 1-Tb, 4b/Cell, 176-Stacked-WL 3D-NAND Flash Memory with Improved Read Latency and a 14.8Gb/mm\(^2\) Density**  
SK hynix, Icheon, Korea

### 9:00 AM

**7.4 A 1Tb 3b/Cell 8th-Generation 3D-NAND Flash Memory with 164MB/s Write Throughput and a 2.4Gb/s Interface**  
Samsung Electronics, Hwaseong, Korea

### 9:10 AM

**7.5 A 512Gb In-Memory-Computing 3D-NAND Flash Supporting Similar-Vector-Matching Operations on Edge-AI Devices**  
H-W. Hu\(^1,2\), W-C. Wang\(^1,3\), C-K. Chen\(^1\), Y-C. Lee\(^1\), B-R. Lin\(^1\), H-M. Wang\(^1\), Y-P. Lin\(^1\), Y-C. Lin\(^1\), C-C. Hsieh\(^1\), C-M. Hu\(^1\), Y-T. Lai\(^1\), H-S. Chen\(^1\), Y-H. Chang\(^1\), H-P. Li\(^1\), T-W. Kuo\(^1,3\), K-C. Wang\(^1\), M-F. Chang\(^1\), C-H. Hung\(^1\), C-Y. Lu\(^1\)  
\(^1\)Macronix, Hsinchu, Taiwan  
\(^2\)National Tsing Hua University, Hsinchu, Taiwan  
\(^3\)National Taiwan University, Taipei, Taiwan  
\(^4\)Academia Sinica, Taipei, Taiwan  
\(^5\)City University of Hong Kong, Hong Kong, China
Plenary Session II — Invited Papers

Session Chair:
Kevin Zhang, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan
ISSCC Conference Chair

Session Co-Chair:
Edith Beigné, Meta, Menlo Park, CA
ISSCC International Technical Program Chair

7:00 AM
1.3 The Art of Scaling: Distributed and Connected to Sustain the Golden Age of Computation
Inyup Kang, President, Samsung Electronics, Hwaseong, Korea

The history of computer was nothing short of a miracle. Thanks to the rapid innovations in semiconductor manufacturing technology, we have started from gigantic machines that filled a whole room, to cheap and tiny microchips that billions of people can afford and keep in their pockets (or should I say, hands?) all day long. Still, even with this level of progress, mobile devices are barely capable of replicating the “brain” of a jellyfish, and the trend shows that we are already hitting our limits in semiconductor scaling. In this paper, we define the Cost-Performance Ratio (CPR) metric that captures the trend in a single equation. We suggest that we shall find solutions in each area of intra-chip, inter-chip, and inter-device level, and highlight the domain-specific computing, 3D packaging, and advanced communication as the main drivers to the next level of computing, satisfying humans’ unquenchable greed.

7:45 AM
1.4 The Future of the High-Performance Semiconductor Industry and Design
Renée James, Founder, Chairman, & CEO, Ampere Computing, Santa Clara, CA

While the explosive growth of today’s modern cloud was fueled by high performance, present-day efficient modern cloud services have moved to a new phase of compute that require scalability and elasticity, while still achieving the highest performance levels to run a myriad of cloud services. The new breed of software underlying today’s cloud services is initiating a third phase of compute unencumbered by architectural complexity designed for client- and server-enterprise applications. Initially, cloud computing was able to leverage traditional processor architectures to deliver value to the end customers. However, massive adoption of cloud-based services has amplified the limitations of the incumbent architectures that were designed for a very different software model in client-server enterprises. The requirement of high-performance for cloud computing has fundamentally changed from one of peak performance at a CPU-level to overall performance at the system-level. This system-level performance refers to maximizing system-level throughput while staying within or further reducing power and cost envelopes, and with much higher emphasis on predictable and consistent performance. This cloud-driven computing requires a fundamental shift in the processor, as well as in SOC architectures and designs, and demands continued innovation to stay ahead of cloud computing growth for the next decade. These innovations need to address the entire vertical stack from software, architecture, design, to packaging and manufacturing domains. The paper will discuss a new approach in architectural thinking and design based on cloud computing as the driving force for demand.

8:30 AM
ISSCC, SSCS, IEEE Award Presentations
8:30 AM
8.1 A 0.0078mm² 3.4mW Wideband Positive-Feedback-Based Noise-Cancelling LNA in 28nm CMOS Exploiting $G_m$ Boosting
Z. Liu, C. C. Boon, C. Li, K. Yang, Y. Dong, T. Guo
Nanyang Technological University, Singapore, Singapore

8:40 AM
8.2 A 2-to-2.48GHz Voltage-Interpolator-Based Fractional-N Type-I Sampling PLL in 22nm FinFET Assisting Fast Crystal Startup
S. Kundu, T. Huusari, H. Luo, A. Agrawal, E. Alban, S. Shahraini, T. Xiong, D. Lake, S. Pellerano, J. Mix, N. Kurd, M. Abdel-moneum, B. Carlton
Intel, Hillsboro, OR

8:50 AM
8.3 A 9-to-12GHz Coupled-RTWO FMCW ADPLL with 97fs RMS Jitter, -120dBc/Hz PN at 1MHz Offset, and with Retrace Time of 12.5ns and 2μs Chirp Settling Time
H. Shanan¹, D. Dalton², V. Chillara³, P. Dato⁴
¹Analog Devices, Somerset, NJ
²Xilinx, Cork, Ireland
³Vishay, Cork, Ireland
⁴Bosch, Valencia, Spain
High-Quality GHz-to-THz Frequency Generation and Radiation

Session Chair: Conan Zhan, MediaTek, Hsinchu, Taiwan
Session Co-Chair: Swami Sankaran, Texas Instruments, Dallas, TX

9:00 AM

9.1 Series-Resonance BiCMOS VCO with Phase Noise of -138dBc/Hz at 1MHz Offset from 10GHz and -190dBc/Hz FoM
A. Franceschin, D. Riccardi, A. Mazzanti
University of Pavia, Pavia, Italy

9:10 AM

9.2 A 0.049mm² 7.1-to-16.8GHz Dual-Core Triple-Mode VCO Achieving 200dB FoM_A in 22nm FinFET
J. Gong¹, B. Patra², L. Enthoven¹, J. V. Staveren¹, F. Sebastiano¹, M. Babaie¹,²
¹Delft University of Technology, Delft, The Netherlands
²QuTech, Delft, The Netherlands
³Intel, Hillsboro, OR

9:20 AM

9.3 A 53.6-to-60.2GHz Many-Core Fundamental Oscillator with Scalable Mesh Topology Achieving -136.0dBc/Hz Phase Noise at 10MHz Offset and 190.3dBc/Hz Peak FoM in 65nm CMOS
H. Jia, R. Ma, W. Deng, Z. Wang, B. Chi
Tsinghua University, Beijing, China

9:30 AM

9.4 A Highly Power Efficient 2×3 PIN-Diode-Based Intercoupled THz Radiating Array at 425GHz with 18.1dBm EIRP in 90nm SiGe BiCMOS
S. Razavian¹, A. Babakhani²
¹University of California, Los Angeles, CA
²University of California, Los Angeles
10.1 A 10GS/s 8b 25fJ/c-s 2850um² Two-Step Time-domain ADC Using Delay-Tracking Pipelined-SAR TDC with 500fs Time Step in 14nm CMOS Technology
J. Liu, M. Hassanpourghadi, M. S-W. Chen
University of Southern California, Los Angeles, CA

10.2 A 0.82mW 14b 130MS/s Pipelined-SAR ADC with a Distributed Averaging Correlated Level Shifting (DACLS) Ringamp and Bypass-Window Backend
J-C. Wang, T-H. Kuo
National Cheng Kung University, Tainan, Taiwan

10.3 A 0.004mm² 200MS/s Pipelined SAR ADC with kT/C Noise Cancellation and Robust Ring-Amp
M. Zhan¹, L. Jie¹, X. Tang², N. Sun¹
¹Tsinghua University, Beijing, China
²Peking University, Beijing, China

10.4 A 0.97mW 260MS/s 12b Pipelined-SAR ADC with Ring-TDC-Based Fine Quantizer for PVT Robust Automatic Cross-Domain Scale Alignment
H. Zhao, F. F. Dai
Auburn University, Auburn, AL

10.5 A 24b 2MS/s SAR ADC with 0.03ppm INL and 106.3dB DR in 180nm CMOS
J. Steensgaard¹, R. Reay², R. Perry³, D. Thomas³, G. Tu³, G. Reitsma²
¹Analog Devices, Sequim, WA
²Analog Devices, Santa Clara, CA

10.6 A 4.96μW 15b Self-Timed Dynamic-Amplifier-Based Incremental Zoom ADC
Y. Liu¹, M. Zhao¹, Y. Zhao¹, X. Yu¹, N. N. Tan¹, L. Ye², Z. Tan¹
¹Zhejiang University, Hangzhou, China
²Peking University, Beijing, China

10.7 A 0.014mm² 10kHz-BW Zoom-Incremental-Counting ADC Achieving 103dB SNDR and 100dB Full-Scale CMRR
L. Jie¹, M. Zhan¹, X. Tang², N. Sun¹
¹Tsinghua University, Beijing, China
²Peking University, Beijing, China
SESSION 11 Live Q&As Tuesday February 22nd, 8:30 AM PST

Compute-in-Memory and SRAM
Session Chair: Eric Karl, Intel, Portland, OR
Session Co-Chair: Yasuhiko Taito, Renesas Electronics Corporation, Kodaira, Japan

8:30 AM

11.1 A 1ynm 1.25V 8Gb, 16Gb/s/pin GDDR6-based Accelerator-in-Memory supporting 1TFLOPS MAC Operation and Various Activation Functions for Deep-Learning Applications

8:40 AM

11.2 A 22nm 4Mb STT-MRAM Data-Encrypted Near-Memory Computation Macro with a 192Gb/s Read-and-Decryption Bandwidth and 25.1-55.1TOPS/W 8b MAC for AI Operations
Y-C. Chiu*, C-S. Yang*, S-H. Teng1, H-Y. Huang1, F-C. Chang1, Y. Wu1, Y-A. Chien1, F-L. Hsieh1, C-Y. Li1, G-Y. Lin1, P-J. Chen1, T-H. Pan1, C-C. Lo1, W-S. Khwa2, R-S. Liu1, C-C. Hsieh1, K-T. Tang1, C-P. Lo2, Y-D. Chih2, T-Y. J. Chang1, M-F. Chang1,2, *Equally-Credited Authors (ECAs)
1National Tsing Hua University, Hsinchu, Taiwan; 2TSMC, Hsinchu, Taiwan

8:50 AM

11.3 A 40-nm, 2M-Cell, 8b-Precision, Hybrid SLC-MLC PCM Computing-in-Memory Macro with 20.5 - 65.0TOPS/W for Tiny-AI Edge Devices
W-S. Khwa*, Y-C. Chiu*, C-J. Jhang2, S-P. Huang2, C-Y. Lee2, T-H. Wen1, F-C. Chang1, S-M. Yu1, T-Y. Lee1, M-F. Chang1,2, *Equally-Credited Authors (ECAs)
1TSMC Corporate Research, Hsinchu, Taiwan; 2National Tsing Hua University, Hsinchu, Taiwan

9:00 AM

11.4 An 8-Mb DC-Current-Free Binary-to-8b Precision ReRAM Nonvolatile Computing-in-Memory Macro using Time-Space-Readout with 1286.4 - 21.6TOPS/W for Edge-AI Devices
J-M. Hung1, Y-H. Huang1, S-P. Huang1, F-C. Chang1, T-H. Wen1, C-I. Su1, W-S. Khwa2, C-C. Lo1, R-S. Liu1, C-C. Hsieh1, K-T. Tang1, Y-D. Chih1, T-Y. J. Chang1, M-F. Chang1,2
1National Tsing Hua University, Hsinchu, Taiwan; 2TSMC, Hsinchu, Taiwan

9:10 AM

11.5 Single-Mode CMOS 6T-SRAM Macros with Keeper-Loading-Free Peripherals and Row-Separate Dynamic Body Bias Achieving 2.53fW/bit Leakage for AIoT Sensing Platforms
Y. Zhang1, C. Xue1, X. Wang1, T. Liu1, J. Gao1, P. Chen1, J. Liu2, L. Sun2, L. Shen1, J. Ru1, L. Ye1,2, R. Huang1
1Peking University, Beijing, China; 2Nano Core Chip Electronic Technology, Hangzhou, China
3Advanced Institute of Information Technology of Peking University, Hangzhou, China

9:20 AM

11.6 A 5-nm 254-TOPS/W 221-TOPS/mm² Fully-Digital Computing-in-Memory Macro Supporting Wide-Range Dynamic-Voltage-Frequency Scaling and Simultaneous MAC and Write Operations
H. Fujiwara1, H. Mon1, W-C. Zhao1, M-C. Chuang1, R. Naous2, C-K. Chuang1, T. Hashizume3, D. Sun4, C-F. Lee1, K. Akarvardar1, S. Adham1, T-L. Chou1, M. E. Sinangil4, Y. Wang1, Y-D. Chih4, Y-H. Chen1, H-J. Liao1, T-Y. J. Chang1
1TSMC, Hsinchu, Taiwan; 2TSMC, San Jose, CA; 3TSMC, Yokohama, Japan; 4TSMC, Austin, TX

9:30 AM

11.7 A 1.041-Mb/mm² 27.38-TOPS/W Signed-INT8 Dynamic-Logic-Based ADC-less SRAM Compute-In-Memory Macro in 28nm with Reconfigurable Bitwise Operation for AI and Embedded Applications
B. Yan1, J-L. Hsu1, P-C. Yu1, C-C. Lee1, Y. Zhang1, W. Yue1, G. Mei1, Y. Yang1, Y. Yang2, H. Li1, Y. Chen4, R. Huang1
1Peking University, Beijing, China; 2NeoNexus, Singapore, Singapore
3Pimchip Technology, Beijing, China; 4Duke University, Durham, NC

9:40 AM

11.8 A 28nm 1Mb Time-Domain Computing-in-Memory 6T-SRAM Macro with a 6.6ns Latency, 1241GOPS and 37.01TOPS/W for 8b MAC Operations for Edge-AI Devices
P-C. Wu1, J-W. Su1, Y-L. Chung1, L-Y. Hong1, J-S. Ren1, F-C. Chang1, Y. Wu1, H-Y. Chen1, C-H. Lin1, H-M. Hsiao1, S-H. Li1, S-S. Sheu1, S-C. Chang1, W-C. Lo1, C-C. Lo1, R-S. Liu1, C-C. Hsieh1, K-T. Tang1, C-I. Wu1, M-F. Chang1
4Equally-Credited Authors (ECAs)
1National Tsing Hua University, Hsinchu, Taiwan; 2Industrial Technology Research Institute, Hsinchu, Taiwan
**SESSION 12 Live Q&As**
Tuesday February 22nd, 8:30 AM PST

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**Monolithic System for Robot and Bio Applications**

*Session Chair: Milin Zhang, Tsinghua University, Beijing, China*
*Session Co-Chair: Daniel Morris, Meta, Menlo Park, CA*

8:30 AM

**12.1** A 210 × 340 × 50μm Integrated CMOS System for Micro-Robots with Energy Harvesting, Sensing, Processing, Communication and Actuation

L. Xu¹, M. Lassiter², X. Wu¹, Y. Kim¹, J. Lee¹, M. Yasuda², M. Kawaminami³, M. Miskin³, D. Blaauw¹, D. Sylvester¹

¹University of Michigan, Ann Arbor, MI; ²University of Pennsylvania, Philadelphia, PA; ³United Semiconductor Japan, Kuvana, Japan

8:40 AM

**12.2** A 200 x 256 Image Sensor Heterogeneously Integrating a 2D Nanomaterial-Based Photo-FET Array and CMOS Time-to-Digital Converters

H. Hinton¹, H. Jang¹, W. Wu¹, M-H. Lee², M. Seo³, H-J. Shin³, S. Park³, D. Ham¹

¹Harvard University, Cambridge, MA; ²Samsung Advanced Institute of Technology, Suwon, Korea

8:50 AM

**12.3** A Self-powering Wireless Soil-pH and Electrical Conductance Monitoring IC with Hybrid Microbial Electrochemical and Photovoltaic Energy Harvesting

C-Y. Wu¹, C-W. Liu¹, J-S. Chen¹, C-S. Huang¹, T-H. Lu¹, L-C. Chen¹, I-C. Ou¹, S-K. Chen², Y-C. Chen², P-H. Chen¹, C-T. Liu², Y-C. Liao², Y-T. Liao¹

¹National Yang Ming Chiao Tung University, Hsinchu, Taiwan; ²National Taiwan University, Taipei, Taiwan

9:00 AM

**12.4** A 256-Channel Actively-Multiplexed μECoG Implant with Column-Parallel Incremental ΔΣ ADCs Employing Bulk-DACs in 22-nm FDSOI Technology

X. Huang¹,², H. Londoño-Ramírez¹,²,³, M. Ballini¹,², C. Van Hoof¹,², J. Genoe¹,², S. Haesler¹,²,³, G. Gielen¹,², N. Van Helleputte¹, C. Mora Lopez¹

¹imec, Leuven, Belgium; ²KU Leuven, Leuven, Belgium

9:10 AM

**12.5** A CMOS Cellular Interface Array for Digital Physiology Featuring High-Density Multi-Modal Pixels and Reconfigurable Sampling Rate

A. Y. Wang*¹, Y. Sheng*¹, W. Lf², D. Jung³, G. Jenke³, J. Park³, D. Lee¹, M. Wang², S. Maharjan³, S. Kumashi³, J. Hao³, Y. S. Zhang³, K. Eggan¹, H. Wang²

*Equally-Credited Authors (ECAs)

¹Georgia Institute of Technology, Atlanta, GA; ²Brigham and Women’s Hospital, Harvard University, Cambridge, MA; ³Qualcomm, San Diego, CA

9:20 AM

**12.6** A CMOS Molecular Electronics Chip for Single-Molecule Biosensing

D. A. Hall¹, N. Ananthapadmanabhan¹, C. Cho², L. Zheng³, P. P. Pan³, C. W. Fuller³, P. P. Padayatti³, C. Gardner³, D. Gebhardt³, Z. Majzik³, P. Sinha³, P. W. Mola³, B. Merriman³

¹University of California, San Diego, CA; ²Roswell Biotechnology, San Diego, CA

9:30 AM

**12.7** 1024 3D-Stacked Monolithic NEMS Array with 375μm2 0.5mW 0.28pm Frequency Deviation Pixel-level Readout for Zeptogram Gravimetric Sensing


CEA-Léti, Grenoble, France
Digital Techniques for Clocking, Variation Tolerance and Power Management

Session Chair: Tanay Karnik, Intel, Hillsboro, OR
Session Co-Chair: Ping-Hsuan Hsieh, National Tsing Hua University, Hsinchu, Taiwan

8:30 AM

13.1 Clock Generator with ISO26262 ASIL-D Grade Safety Mechanism for SoC Clocking Application
Samsung Electronics, Hwaseong, Korea

8:40 AM

13.2 A 97fs_{rms}-Jitter and 68-Multiplication Factor, 8.16GHz Ring-Oscillator Injection-Locked Clock Multiplier with Power-Gating Injection-Locking and Background Multi-Functional Digital Calibrator
S. Park*, S. Yoo**, Y. Shin†, J. Lee‡, J. Choi§
*Equally-Credited Authors (ECAs)
1KAIST, Daejeon, Korea; 2Qualcomm, San Diego, CA

8:50 AM

13.3 A 0.021mm² 65nm CMOS 2.5GHz Digital Injection-Locked Clock Multiplier with Injection Pulse Shaping Achieving -79dBc Reference Spur and 0.496mW/GHz Power Efficiency
R. Xu, D. Ye, S. Li, C.-J. R. Shi
1Fudan University, Shanghai, China; 2University of Washington, Seattle, WA

9:00 AM

13.4 Fully Automated Hardware-Driven Clock-Gating Architecture with Complete Clock Coverage for 5nm Exynos Mobile SoC
Samsung Electronics, Hwaseong, Korea

9:10 AM

13.5 Deterministic Frequency Boost and Voltage Enhancements on the POWER10™ Processor
B. T. Vanderpool, P. J. Restle, E. J. Fluhr, G. S. Still, F. Campisano, I. Carmichael, E. Marz, R. Batra, R. Willaman
1IBM, Rochester, MN; 2IBM, Yorktown Heights, NY; 3IBM, Austin, TX; 4IBM, Research Triangle Park, NC; 5IBM, Essex Junction, VT

9:20 AM

13.6 A 0.65V 1316μm² Fully Synthesizable Digital Temperature Sensor Using Wire Metal Achieving 0.16nJ⋅°C²-Accuracy FoM in 5nm FinFET CMOS
J. Park, J. Kim, K. Kim, J-H. Yang, M. Choi, J. Shin
Samsung Electronics, Gyeonggi, Korea

9:30 AM

13.7 Energy Minimization of Duty-Cycled Systems Through Optimal Stored-Energy Recycling from Idle Domains
C-H. Huang, A. Manda, D. Peña-Colaiocco, E. Pereira Da Silva, V. Sathe
1University of Washington, Seattle, WA; 2NXP Semiconductors, Austin, TX

9:40 AM

13.8 A 194nW Energy-Performance-Aware IoT SoC Employing a 5.2nW 92.6% Peak Efficiency Power Management Unit for System Performance Scaling, Fast DVFS and Energy Minimization
X. Liu, S. Kamineni, J. Breiholz, B. H. Calhoun, S. Li
University of Virginia, Charlottesville, VA
GaN, High-Voltage and Wireless Power

Session Chair: Bernhard Wicht, University of Hannover, Hannover, Germany
Session Co-Chair: Patrik Arno, ST Microelectronics, Grenoble, France, Metropolitan

8:30 AM

14.1 A Monolithic GaN-Based Driver and GaN Power HEMT with Diode-Emulated GaN Technique for 50MHz Operation and Sub-0.2ns Deadtime Control
Y-Y. Kao1, T-W. Wang1, S-H. Hung1, Y-H. Wen1, T-H. Yang1, S-Y. Li1, K-H. Chen1, Y-H. Lin2, S-R. Lin2, T-Y. Tsai2
1National Yang Ming Chiao Tung University, Hsinchu, Taiwan
2Realtek Semiconductor, Hsinchu, Taiwan

8:40 AM

14.2 A 110V/230V 0.3W Offline Chip-Scale Power Supply with Integrated Active Zero-Crossing Buffer and Voltage-Interval-Based Dual-Mode Control
C. Rindfleisch, B. Wicht, Leibniz University Hannover, Hannover, Germany

8:50 AM

14.3 A Monolithic GaN Direct 48V/1V AHB Switching Power IC with Auto-Lock Auto-Break Level Shifting, Self-Bootstrapped Hybrid Gate Driving, and On-Die Temperature Sensing
D. Yan, D. B. Ma, University of Texas, Dallas, TX

9:00 AM

14.4 A 2.5−5MHz 87% Peak Efficiency 48V-to-1V Integrated Hybrid DC-DC Converter Adopting Ladder SC Network with Capacitor Assisted Dual Inductor Filtering
C. Chen, J. Liu, H. Lee, University of Texas, Dallas, TX

9:10 AM

14.5 2-Tx Digital Envelope-Tracking Supply Modulator Achieving 200MHz Channel Bandwidth and 93.6% Efficiency for 2G/3G/LTE/NR RF Power Amplifiers
Samsung Electronics, Hwaseong, Korea

9:20 AM

14.6 A 27W D2D Wireless Power Transfer System with Compact Single-Stage Regulated Class-E Architecture and Adaptive ZVS Control
X. Ma1,2, Y. Lu1, W-H. Ki1
1Hong Kong University of Science and Technology, Hong Kong, China
2University of Macau, Macau, China

9:30 AM

14.7 A 1.2W 51%-Peak-Efficiency Isolated DC-DC Converter with a Cross-Coupled Shoot-Through-Free Class-D Oscillator Meeting the CISPR-32 Class-B EMI Standard
D. Pan1, G. Li1, F. Miao1, W. Sun1, X. Gong2, L. Zhang2, L. Cheng1
1University of Science and Technology of China, Hefei, China
2Suzhou Novosense Microelectronics, Suzhou, China

9:40 AM

14.8 A 68.3% Efficiency Reconfigurable 400-/800-mW Capacitive Isolated DC-DC Converter with Common-Mode Transient Immunity and Fast Dynamic Response by Through-Power-Link Hysteretic Control
J. Tang, L. Zhao, C. Huang, Iowa State University, Ames, IA
21.1 SambaNova SN10 RDU: A 7nm Dataflow Architecture to Accelerate Software 2.0
R. Prabhakar, S. Jairath, J. L. Shin
SambaNova Systems, Palo Alto, CA

21.2 A64FX: 52-Core Processor Designed for the 442PetaFLOPS Supercomputer Fugaku
Fujitsu, Kawasaki, Japan

V. B. Suresh¹, C. S. Katta², S. Rajagopalan³, T. Z. Zhou³, A. Patel⁴, R. Rakha⁵, N. K. Gopalakrishna⁵, S. Mathew⁴, A. Hukkoo⁵
¹Intel, Hillsboro, OR
²Intel, Santa Clara, CA
³Intel, San Diego, CA

21.4 The Wormhole AI Training Processor
D. Ignjatovic, D. W. Bailey, L. Bajic
Tenstorrent, Toronto, Canada

7:00-7:45
Panel Q&A
This year, Demonstration Session 1 extending in selected regular papers, both Academic and Industrial, will take place on Wednesday, February 23rd starting at 7:00 am. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2022, as noted by the symbol **DS1**.

### 3.8 | A BJT-Based CMOS Temperature Sensor Achieving an Inaccuracy of ±0.45°C (3σ) from -50°C to 180°C and a Resolution-FoM of 7.2pJ-K² at 150°C

### 4.1 | Fully Integrated 2D Scalable TX/RX Chipset for D-Band Phased-Array-on-Glass Modules

### 4.5 | Electronic THz Pencil Beam Forming and 2D Steering for High Angular-Resolution Operation: A 98×98-Unit 265GHz CMOS Reflectarray with In-Unit Digital Beam Shaping and Squint Correction

### 5.2 | A 64×64-Pixel Flash LiDAR SPAD Imager with Distributed Pixel-to-Pixel Correlation for Background Rejection, Tunable Automatic Pixel Sensitivity and First-Last Event Detection Strategies for Space Applications

### 5.3 | An 80×60 Flash LiDAR Sensor with In-Pixel Histogramming TDC Based on Quaternary Search and Time-Gated Δ-Intensity Phase Detection for 45m Detectable Range and Background Light Cancellation

### 5.9 | A 10b Source-Driven IC with LSB-Stacked LV-to-HV-Amplify DAC Achieving 2688μm²/channel and 4.8mV DVO for Mobile OLED Displays

### 6.1 | A 1.41pJ/b 224Gb/s PAM-4 SerDes Receiver with 31dB Loss Compensation

### 6.7 | A 50Gb/s PAM-4 Bi-Directional Plastic Waveguide Link with Carrier Synchronization Using PI-Based Costas Loop

### 8.2 | A 2-to-2.48GHz Voltage-Interpolator-Based Fractional-N Type-I Sampling PLL in 22nm FinFET Assisting Fast Crystal Startup

### 12.5 | A CMOS Cellular Interface Array for Digital Physiology Featuring High-Density Multi-Modal Pixels and Reconfigurable Sampling Rate

### 12.6 | A CMOS Molecular Electronics Chip for Single-Molecule Biosensing

### 14.2 | A 110V/230V 0.3W Offline Chip-Scale Power Supply with Integrated Active Zero-Crossing Buffer and Voltage-Interval-Based Dual-Mode Control

### 18.5 | A 12 A I max, Fully Integrated Multi-Phase Voltage Regulator with 91.5% Peak Efficiency at 1.8 to 1V, Operating at 50 MHz and Featuring a Digitally Assisted Controller with Automatic Phase Shedding and Soft Switching in 4nm Class FinFET CMOS

### 19.3 | A 28GHz Compact 3-Way Transformer-Based Parallel-Series Doherty Power Amplifier with 20.4%/14.2% PAE at 6-/12-dB Power Back-Off and 25.5dBm P 50 in 55nm Bulk CMOS

### 20.2 | A Time-Division Multiplexed 8-Channel Non-Contact ECG Recording IC with a Common-Mode Interference Tolerance of 20Vpp


### 32.1 | BatDrone: A 9.83M-focal-points/s 7.76μs-Latency Ultrasound Imaging System with On-Chip Per-Voxel RX Beamfocusing for 7m-Range Drone Applications
Highlighted Chip Releases: Systems and Quantum Computing

Session Chair: Fabio Sebastiano, Delft University of Technology, Delft, The Netherlands
Session Co-Chair: Alice Wang, Everactive, Plano, TX

26.1 Beyond-Classical Computing Using Superconducting Quantum Processors
J. Bardin\(^1,2\)
\(^1\)Google Quantum AI, Goleta, CA
\(^2\)University of Massachusetts, Amherst, MA

26.2 Design Considerations for Superconducting Quantum Systems
G. Zettles\(^*1\), S. Willenborg\(^*1\), B. Johnson\(^2\), A. Wack\(^2\), B. Allison\(^1\)
\(^*\)Equally-Credited Authors (ECAs)
\(^1\)IBM, Rochester, MN
\(^2\)IBM, Yorktown Heights, NY

26.3 Augmented Reality – The Next Frontier of Image Sensors and Compute Systems
C. Liu, S. Chen, T-H. Tsai, B. De Salvo, J. Gomez
Meta Reality Labs, Redmond, WA

26.4 3D V-Cache: The Implementation of a Hybrid-Bonded 64MB Stacked Cache for a 7nm x86-64 CPU
J. Wuu\(^1\), R. Agarwa\(^F\), M. Ciraula\(^1\), C. Dietz\(^1\), B. Johnson\(^1\), D. Johnson\(^1\), R. Schreiber\(^9\), R. Swaminathan\(^9\), W. Walker\(^9\), S. Naffziger\(^1\)
\(^1\)AMD, Fort Collins, CO
\(^2\)AMD, Santa Clara, CA
\(^9\)AMD, Austin, TX

7:45 - 8:30
Panel Q&A
This year, Demonstration Session 2 extending in selected regular papers, both Academic and Industrial, will take place on Wednesday, February 23rd starting at 7:45 am. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2022, as noted by the symbol DS2.

### 2.7 Zen3: The AMD 2nd-Generation 7nm x86-64 Microprocessor Core

### 4.3 A 140GHz Transceiver with Integrated Antenna, Inherent-Low-Loss Duplexing and Adaptive Self-Interference Cancellation for FMCW Monostatic Radar

### 7.5 A 512Gb In-Memory-Computing 3D-NAND Flash Supporting Similar-Vector-Matching Operations on Edge-AI Devices

### 11.1 A 1ynm 1.25V 8Gb, 16Gb/s/pin GDDR6-based Accelerator-in-Memory supporting 1TFLOPS MAC Operation and Various Activation Functions for Deep-Learning Applications

### 11.7 A 1.041-Mb/mm2 27.38-TOPS/W Signed-INT8 Dynamic-Logic-Based ADC-less SRAM Compute-In-Memory Macro in 28nm with Reconfigurable Bitwise Operation for AI and Embedded Applications

### 15.4 Hiddenite: 4K-PE Hidden Network Inference 4D-Tensor Engine Exploiting On-Chip Model Construction Achieving 34.8-to-16.0TOPS/W for CIFAR-100 and ImageNet

### 15.8 Analog Matrix Processor for Edge AI Real-Time Video Analytics

### 16.3 A 40nm 60.64TOPS/W ECC-Capable Compute-in-Memory/Digital 2.25MB/768KB RRAM/SRAM System with Embedded Cortex M3 Microprocessor for Edge Recommendation Systems

### 16.4 Flex6502: A Flexible 8b Microprocessor in 0.8μm Metal-Oxide Thin-Film Transistor Technology Implemented with a Complete Digital Design Flow Running Complex Assembly Code

### 16.6 A 65nm 63.3μW 15Mbps Transceiver with Switched-Capacitor Adiabatic Signaling and Combinatorial-Pulse-Position Modulation for Body-Worn Video-Sensing AR Nodes

### 21.3 Bonanza Mine: An Ultra-Low-Voltage Energy-Efficient Bitcoin Mining ASIC

### 24.2 A 1.66Gb/s and 5.8pJ/b Transcutaneous IR-UWB Telemetry System with Hybrid Impulse Modulation for Intracortical Brain-Computer Interfaces

### 27.3 A 24-to-30GHz 256-Element Dual-Polarized 5G Phased Array with Fast Beam-Switching Support for >30,000 Beams

### 33.1 A 1.05A/m Minimum Magnetic Field Strength Single-Chip Fully Integrated Biometric Smart Card SoC Achieving 1014.7ms Transaction Time with Anti-Spoofing Fingerprint Authentication

### 33.3 A HD 31fps 7×7-View Light-Field Factorization Processor for Dual-Layer 3D Factored Display

### 33.4 DSPU: A 281.6mW Real-Time Depth Signal Processing Unit for Deep Learning-Based Dense RGB-D Data Acquisition with Depth Fusion and 3D Bounding Box Extraction in Mobile Platforms

### 34.3 ShieldNN: A Threshold-Implementation-Based Neural-Network Accelerator Securing Model Parameters and Inputs Against Power Side-Channel Attacks
ML Processors

Session Chair: SukHwan Lim, Samsung Electronics, Hwaseong-si, Korea
Session Co-Chair: Sophia Shao, University of California, Berkeley, Berkeley, CA

8:30 AM

15.1 A Multi-Mode 8K-MAC HW-Utilization-Aware Neural Processing Unit with a Unified Multi-Precision Datapath in 4nm Flagship Mobile SoC
J-S. Park1, C. Park1, S. Kwon1, H-S. Kim1, T. Jeon1, Y. Kang1, H. Lee1, D. Lee1, J. Kim1, Y. Lee1, S. Park1, J-W. Jang2, S. Ha1, M. Kim1, J. Bang1, S. H. Lim1, I. Kang1
1Samsung Electronics, Hwaseong, Korea
2Samsung Advanced Institute of Technology, Suwon, Korea

8:40 AM

15.2 A 65nm Systolic Neural CPU Processor for Combined Deep Learning and General-Purpose Computing with 95% PE Utilization, High Data Locality and Enhanced End-to-End Performance
Y. Ju, J. Gu, Northwestern University, Evanston, IL

8:50 AM

15.3 COMB-MCM: Computing-on-Memory-Boundary NN Processor with Bipolar Bitwise Sparsity Optimization for Scalable Multi-Chiplet-Module Edge Machine Learning
1Fudan University, Shanghai, China; 2Alibaba DAMO Academy, Shanghai, China

9:00 AM

15.4 Hiddenite: 4K-PE Hidden Network Inference 4D-Tensor Engine Exploiting On-Chip Model Construction Achieving 34.8-to-16.0TOPS/W for CIFAR-100 and ImageNet

9:10 AM

15.5 A 28nm 29.2TFLOPS/W BF16 and 36.5TOPS/W INT8 Reconfigurable Digital CIM Processor with Unified FP/INT Pipeline and Bitwise In-Memory Booth Multiplication for Cloud Deep Learning Acceleration
F. Tu1,2, Y. Wang1, Z. Wu1, L. Liang2, Y. Ding2, B. Kim2, L. Liu1, S. Wei1, Y. Xie2, S. Yin1
1Tsinghua University, Beijing, China; 2University of California, Santa Barbara, CA

9:20 AM

15.6 DIANA: An End-to-End Energy-Efficient Digital and ANAlog Hybrid Neural Network SoC
K. Ueyoshi1, I. A. Papistas2, P. Houshmand1, G. M. Sarda1,2, V. Jain1, M. Shi1, Q. Zheng1, S. Giraldo1, P. Vrancx2, J. Doevenspeck2, D. Bhattacharjee2, S. Cosemans2, A. Malik2, P. Debacker2, D. Verkest2, M. Verhelst1,2, 1KU Leuven, Leuven, Belgium; 2imec, Leuven, Belgium

9:30 AM

15.7 ARCHON: A 332.7TOPS/W 5b Variation-Tolerant Analog CNN Processor Featuring Analog Neuronal Computation Unit and Analog Memory
J-O. Seo1, M. Seok2, S. Choi1, 1KAIST, Daejeon, Korea; 2Columbia University, New York, NY

9:40 AM

15.8 Analog Matrix Processor for Edge AI Real-Time Video Analytics
L. Fick1, S. Skrzyniarz1, M. Parikh1, M. B. Henry2, D. Fick1
1Mythic, Austin, TX; 2Mythic, Redwood City, CA

9:50 AM

15.9 A 0.8V Intelligent Vision Sensor with Tiny Convolutional Neural Network and Programmable Weights Using Mixed-Mode Processing-in-Sensor Technique for Image Classification
*Equally-Credited Authors (ECAs), National Tsing Hua University, Hsinchu, Taiwan
SESSION 16 LIVE Q&As  Wednesday February 23rd, 8:30 AM PST

Emerging Domain-Specific Digital Circuits and Systems
Session Chair: Huichu Liu, Meta, Menlo Park, CA
Session Co-Chair: Mijung Noh, Samsung Electronics, Hwaseong-si, Korea

8:30 AM

16.1 DIMC: 2219TOPS/W 2569F2/b Digital In-Memory Computing Macro in 28nm Based on Approximate Arithmetic Hardware
D. Wang1, C-T. Lin1, G. K. Chen2, P. Knag2, R. K. Krishnamurthy2, M. Seok1
1Columbia University, New York, NY
2Intel, Portland, OR

8:40 AM

16.2 A 40nm 64kb 26.56TOPS/W 2.37Mb/mm2 RRAM Binary/Compute-in-Memory Macro with 4.23× Improvement in Density and >75% Use of Sensing Dynamic Range
S. D. Spetalnick1, M. Chang1, B. Crafton1, W-S. Khwa2, Y-D. Chih3, M-F. Chang2, A. Raychowdhury1
1Georgia Institute of Technology, Atlanta, GA
2TSMC Corporate Research, Hsinchu, Taiwan
3TSMC Design Technology, Hsinchu, Taiwan

8:50 AM

16.3 A 40nm 60.64TOPS/W ECC-Capable Compute-in-Memory/Digital 2.25MB/768KB RRAM/SRAM System with Embedded Cortex M3 Microprocessor for Edge Recommendation Systems
M. Chang1, S. D. Spetalnick1, B. Crafton1, W-S. Khwa2, Y-D. Chih3, M-F. Chang2, A. Raychowdhury1
1Georgia Institute of Technology, Atlanta, GA
2TSMC Corporate Research, Hsinchu, Taiwan
3TSMC Design Technology, Hsinchu, Taiwan

9:00 AM

16.4 Flex6502: A Flexible 8b Microprocessor in 0.8μm Metal-Oxide Thin-Film Transistor Technology Implemented with a Complete Digital Design Flow Running Complex Assembly Code
H. Çeliker1,2, A. Sou3, B. Cobb3, W. Dehaene1,2, K. Myny1,2
1imec, Leuven, Belgium
2KU Leuven ESAT, Leuven, Belgium
3PragmatIC Semiconductor Ltd, Cambridge, United Kingdom

9:10 AM

16.5 FlexSpin: A Scalable CMOS Ising Machine with 256 Flexible Spin Processing Elements for Solving Complex Combinatorial Optimization Problems
Y. Su1, T-H. Kim1, B. Kim2
1Nanyang Technological University, Singapore, Singapore
2University of California, Santa Barbara, CA

9:20 AM

16.6 A 65nm 63.3μW 15Mbps Transceiver with Switched-Capacitor Adiabatic Signaling and Combinatorial-Pulse-Position Modulation for Body-Worn Video-Sensing AR Nodes
B. Chatterjee, A. Datta, M. Nath, G. K. K, N. Modak, S. Sen
Purdue University, West Lafayette, IN

9:30 AM

16.7 An Optimal Digital Beamformer for mm-Wave Phased Arrays with 660MHz Instantaneous Bandwidth in 28nm CMOS
D. Peña-Colaicco, C-H. Huang, K-D. Chu, J. C. Rudell, V. Sathe
University of Washington, Seattle, WA
8:30 AM  
**17.1 A 4.6pJ/b 200Gb/s Analog DP-QPSK Coherent Optical Receiver in 28nm CMOS**  
*Equally-Credited Authors (ECAs)  
Peking University, Beijing, China

8:40 AM  
**17.2 A 2.4pJ/b 100Gb/s 3D-Integrated PAM-4 Optical Transmitter with Segmented SiP MOSCAP Modulators and a 2-Channel 28nm CMOS Driver**  
A. Hashemi Talkhooncheh¹, W. Zhang², M. Wang¹, D. J. Thomson², M. Ebert², L. Kø², G. T. Reed², A. Emami¹  
¹California Institute of Technology, Pasadena, CA  
²University of Southampton, Southampton, United Kingdom

8:50 AM  
**17.3 A 10Gb/s Digital Isolator Using Coupled Split-Ring Resonators with 24kVpk Surge Capability and 100kV/μS Common-Mode Transient Immunity**  
J. Xu, R. Yun, B. Chen  
Analog Devices, Wilmington, MA

9:00 AM  
**17.4 A 56GHz 23mW Fractional-N PLL with 110fs Jitter**  
Y. Zhao, O. Memioglu, B. Razavi  
University of California, Los Angeles, CA

9:10 AM  
**17.5 A 480-Multiplication-Factor 13.2-to-17.3GHz Sub-Sampling PLL Achieving 6.6mW Power and -248.1dB FoM Using a Proportionally Divided Charge Pump**  
L. Zhang, A. Niknejad  
University of California, Berkeley, CA

9:20 AM  
**17.6 A 65nm CMOS, 3.5-to-11GHz, Less-Than-1.45LSB-INLpp, 7b Twin Phase Interpolator with a Wideband, Low-Noise Delta Quadrature Delay-Locked Loop for High-Speed Data Links**  
Z. Wang, P. R. Kinget  
Columbia University, New York, NY

9:30 AM  
**17.7 A 9b-Linear 14GHz Integrating-Mode Phase Interpolator in 5nm FinFET Process**  
A. K. Mishra¹, Y. Li², P. Agarwal², S. Shekhar³  
¹University of British Columbia, Vancouver, Canada  
²MaxLinear, Carlsbad, CA  
³MaxLinear, Carlsbad, CA
DC-DC Converters

Session Chair: Harish Krishnamurthy, Intel, Hillsboro, OR
Session Co-Chair: Xun Liu, The Chinese University of Hong Kong, Shenzhen, Shenzhen, China

8:30 AM

18.1 A 1.23W/mm² 83.7%-Efficiency 400MHz 6-Phase Fully-Integrated Buck Converter in 28nm CMOS with On-Chip Capacitor Dynamic Re-Allocation for Inter-Inductor Current Balancing and Fast DVS of 75mV/ns
J-H. Cho¹, D-K. Kim¹, H-H. Bae¹, Y-J. Lee¹,², S-T. Koh¹, Y. Choo², J-S. Paek², H-S. Kim¹
¹KAIST, Daejeon, Korea; ²Samsung Electronics, Hwaseong, Korea

8:40 AM

18.2 A 12V/24V-to-1V DSD Power Converter with 56mV Droop and 0.9μs 1% Settling Time for a 3A/20ns Load Transient
J. Yuan, Z. Liu, F. Wu, L. Cheng
University of Science and Technology of China, Hefei, China

8:50 AM

18.3 A 4A 12-to-1 Flying Capacitor Cross-Connected DC-DC Converter with Inserted D>0.5 Control Achieving >2x Transient Inductor Current Slew Rate and 0.73x Theoretical Minimum Output Undershoot of DSD
T. Hu¹, M. Huang¹, Y. Lu¹, R. P. Martins¹,²
¹University of Macau, Macau, China; ²University of Lisboa, Lisbon, Portugal

9:00 AM

18.4 A Monolithic 3:1 Resonant Dickson Converter with Variable Regulation and Magnetic-Based Zero-Current Detection and Autotuning
P. H. McLaughlin, K. Datta, J. T. Stauth
Dartmouth College, Hanover, NH

9:10 AM

18.5 A 12 A Imax, Fully Integrated Multi-Phase Voltage Regulator with 91.5% Peak Efficiency at 1.8 to 1V, Operating at 50 MHz and Featuring a Digitally Assisted Controller with Automatic Phase Shedding and Soft Switching in 4nm Class FinFET CMOS
C. Schaef¹, T. Salus², R. Rayess³, S. Kulasekaran⁴, M. Manusharow⁴, K. Radhakrishnan⁴, J. Douglas⁴
¹Intel, Hillsboro, OR; ²Intel, Haifa, Israel; ³Intel, Hudson, MA; ⁴Intel, Chandler, AZ

9:20 AM

18.6 A 5V Input 98.4% Peak Efficiency Reconfigurable Capacitive-Sigma Converter with Greater than 90% Peak Efficiency for the Entire 0.4–1.2V Output Range
X. Yang, L. Zhao, M. Zhao, Z. Tan, L. He, Y. Ding, W. Li, W. Qu
Zhejiang University, Hangzhou, China

9:30 AM

18.7 A 2–5MHz Multiple DC Output Hybrid Boost Converter with Scalable CR Boosting Scheme Achieving 91% Efficiency at a Conversion Ratio of 12
C. Chen, J. Liu, H. Lee
University of Texas, Dallas, TX

9:40 AM

18.8 A Battery-Input Sub-1V Output 92.9% Peak Efficiency 0.3A/mm² Current Density Hybrid SC-Parallel-Inductor Buck Converter with Reduced Inductor Current in 65nm CMOS
G. Cai¹, Y. Lu¹, R. Martins¹,²
¹University of Macau, Macau, China; ²University of Lisboa, Lisbon, Portugal
Power Amplifiers and Building Blocks
Session Chair: Hongtao Xu, Fudan University, Shanghai, China
Session Co-Chair: Yves Baeyens, Nokia - Bell Labs, New Providence, NJ

8:30 AM

19.1 A 110-to-130GHz SiGe BiCMOS Doherty Power Amplifier with Slotline-Based Power-Combining Technique Achieving >22dBm Saturated Output Power and >10% Power Back-Off Efficiency
X. Li, W. Chen, S. Li, H. Wu, X. Yi, R. Han, Z. Feng
1Tsinghua University, Beijing, China
2South China University of Technology, Guangzhou, China
3Massachusetts Institute of Technology, Boston, MA

8:40 AM

19.2 A 1V 32.1dBm 92-to-102GHz Power Amplifier with a Scalable 128-to-1 Power Combiner Achieving 15% Peak PAE in a 65nm Bulk CMOS Process
W. Zhu, J. Wang, R. Wang, J. Zhang, C. Li, S. Yin, Y. Wang
Tsinghua University, Beijing, China

8:50 AM

19.3 A 28GHz Compact 3-Way Transformer-Based Parallel-Series Doherty Power Amplifier with 20.4%/14.2% PAE at 6-/12-dB Power Back-Off and 25.5dBm P_{SAT} in 55nm Bulk CMOS
Z. Ma, K. Ma, K. Wang, F. Meng
1Tianjin University, Tianjin, China
2University of Electronic Science and Technology of China, Chengdu, China

9:00 AM

19.4 A 26-to-39GHz Broadband Ultra-Compact High-Linearity Switchless Hybrid N/PMOS Bi-Directional PA/LNA Front-End for Multi-Band 5G Large-Scaled MIMO System
J. Park, H. Wang
1Georgia Institute of Technology, Atlanta, GA
2ETH Zurich, Zurich, Switzerland

9:10 AM

19.5 A 16nm, +28dBm Dual-Band All-Digital Polar Transmitter Based on 4-core Digital PA for Wi-Fi6E Applications
1Intel, Haifa, Israel
2Intel, Oregon, OR

9:20 AM

19.6 A Broadband Mm-Wave VSWR-Resilient Joint True Power Detector and Impedance Sensor Supporting Single-Ended Antenna Interfaces
D. J. Munzer, N. S. Mannem, E. Garay, H. Wang
1Georgia Institute of Technology, Atlanta, GA
2ETH Zurich, Zurich, Switzerland

9:30 AM

19.7 A 1-to-18GHz Distributed-Stacked-Complementary Triple-Balanced Passive Mixer With up to 33dBm IIP3 and Integrated LO Driver in 45nm CMOS SOI
C. Hill, J. F. Buckwalter
1LintrinsIC Semiconductors, Somerville, MA
2University of California, Santa Barbara, CA
SESSION 20 LIVE Q&As  Wednesday February 23rd, 8:30 AM PST

Body and Brain Interfaces
Session Chair: Sohmyung Ha, New York University Abu Dhabi, Abu Dhabi, United Arab Emirates
Session Co-Chair: Rikky Muller, University of California, Berkeley, CA

8:30 AM
20.1  A 0.5mΩ/√Hz 106dB SNR 0.45cm² Dry-Electrode Bioimpedance Interface with Current Mismatch Cancellation and Boosted Input Impedance of 100MΩ at 50kHz
Q. Pan, T. Qu, B. Tang, F. Shan, Z. Hong, J. Xu, Fudan University, Shanghai, China

8:40 AM
20.2  A Time-Division Multiplexed 8-Channel Non-Contact ECG Recording IC with a Common-Mode Interference Tolerance of 20Vpp
K-J. Choi, J-Y. Sim, Pohang University of Science and Technology, Pohang, Korea

8:50 AM
20.3  A 0.7V 17fJ/step-FOMw 178.1dB-FOMSNDR 178.1dB-FOMSNDR 10kHz-BW 560mVpp True-ExG Biopotential Acquisition System with Parasitic-Insensitive 421MΩ Input Impedance in 0.18μm CMOS
S. Lee1, Y. Choi1, G. Kim1, S. Baik1, T. Seol1, H. Jang1, D. Lee1, M. Je2, J-W. Choi3, A. K. George4, J. Lee5
1Daegu Gyeongbuk Institute of Science and Technology, Daegu, Korea; 2KAIST, Daejeon, Korea

9:00 AM
20.4  A 256-Channel 0.227μJ/class Versatile Brain Activity Classification and Closed-Loop Neuromodulation SoC with 0.004mm²-1.51μW/channel Fast-Settling Highly Multiplexed Mixed-Signal Front-End
U. Shin1,2, L. Somappa1, C. Ding1, B. Zhu1,2, Y. Vyza1, A. Trouillet1, S. P. Lacour1,3, M. Shoaran1,3
1EPFL, Lausanne, Switzerland; 2Cornell University, Ithaca, NY
3Center for Neuroprosthetics, Geneva, Switzerland

9:10 AM
20.5  A Miniaturized Wireless Neural Implant with Body-Coupled Data Transmission and Power Delivery for Freely Behaving Animals
C. Lee*,1, B. Kim*,2, J. Kim*,1, S. Lee3,4, T. Jeon1, W. Choi1, S. Yang3,4, J-H. Ahn1, J. Bae2, Y. Chae1
*Equally-Credited Authors (ECAs); 1Yonsei University, Seoul, Korea
2Kangwon National University, Chuncheon, Korea; 3Incheon National University, Incheon, Korea
4gBrain, Incheon, Korea

9:20 AM
20.6  A Reconfigurable Sub-Array Multiplexing Microelectrode Array System with 24,320 Electrodes and 380 Readout Channels for Investigating Neural Communication
J-H. Cha1, J-H. Park1, Y. Park1, H. Shin2, K. S. Hwang2, I-J. Cho3, S-J. Kim1
1Ulsan National Institute of Science and Technology, Ulsan, Korea
2Korea Institute of Science and Technology, Seoul, Korea

9:30 AM
20.7  An SpO2 Sensor Using Reconstruction-Free Sparse Sampling for 70% System Power Reduction
S. Faraji Alamouti1, C. Yalcin1, J. Jan1, J. Ting1, A. C. Arias1, R. Muller1,2
1University of California, Berkeley, CA; 2Chan Zuckerberg Biohub, San Francisco, CA

9:40 AM
20.8  A 145.2dB-DR Baseline-Tracking Impedance Plethysmogram IC for Neckband-Based Blood Pressure and Cardiovascular Monitoring
C. S. Park1, H. Kim1, K. Lee1, D. S. Keum1, D. P. Jang1, J. J. Kim1
1Ulsan National Institute of Science and Technology, Ulsan, Korea
2SOSO H&C, Daegu, Korea; 3Hanyang University, Seoul, Korea
22.1 A Cryo-CMOS Low-Power Semi-Autonomous Qubit State Controller in 14nm FinFET Technology
D. J. Frank1, S. Chakraborty1, K. Tien1, P. Rosno2, T. Fox1, M. Yeck1, J. A. Glick1, R. Robertazzi1, R. Richetta1, J. F. Bulzacchelli1, D. Ramirez2, D. Yilma2, A. Davies3, R. V. Joshi1, S. D. Chambers2, S. Lekuch1, K. Inoue1, D. Underwood1, D. Wisniewski1, C. Baks1, D. Bethune1, J. Timmerwilke1, B. R. Johnson1, B. P. Gaucher1, D. J. Friedman1
1IBM T. J. Watson Research Center, Yorktown Heights, NY
2IBM Systems, Rochester, MN; 3IBM Almaden Research Center, San Jose, CA

22.2 A Cryo-CMOS Controller IC with Fully Integrated Frequency Generators for Superconducting Qubits
*Equally-Credited Authors (ECAs), Pohang University of Science and Technology, Pohang, Korea

22.3 A Cryogenic SiGe BiCMOS Hybrid Class B/C Mode-Switching VCO Achieving 201dBc/Hz Figure-of-Merit and 4.2GHz Frequency Tuning Range
Y. Peng1,2, A. Ruffino1, J. Benserhir1, E. Charbon1
1Ecole Polytechnique Fédérale de Lausanne, Neuchâtel, Switzerland
2Southern University of Science and Technology, Shenzhen, China

22.4 A WiFi and Bluetooth Backscattering Combo Chip Featuring Beam Steering via a Fully-Reflective Phased-Controlled Multi-Antenna Termination Technique Enabling Operation Over 56 Meters
S-K. Kuo, M. Dunna, D. Bharadia, P. P. Mercier, University of California, San Diego, CA

22.5 A 108nW 0.8mm² Analog Voice Activity Detector (VAD) Featuring a Time-Domain CNN as a Programmable Feature Extractor and a Sparsity-Aware Computational Scheme in 28nm CMOS
F. Chen1, K-F. Uni1, W-H. Yu1, P-I. Mak1, R. P. Martins1,2
1University of Macau, Macau, China
2University of Lisboa, Lisbon, Portugal

22.6 A 23μW Solar-Powered Keyword-Spotting ASIC with Ring-Oscillator-Based Time-Domain Feature Extraction
K. Kim1, C. Gao1, R. Graça1, I. Kiselev1, H-J. Yoo1, T. Delbruck1, S-C. Liu1
1University of Zurich and ETH Zurich, Zurich, Switzerland

22.7 An 82nW 0.53pJ/SOP Clock-Free Spiking Neural Network with 40μs Latency for AIoT Wake-Up Functions Using Ultimate-Event-Driven Bionic Architecture and Computing-in-Memory Technique
Y. Liu1, Z. Wang1,2, W. He1, L. Shen1, Y. Zhang1, P. Chen1, M. Wu1, H. Zhang1, P. Zhou3, J. Liu1, G. Sun1, J. Ru1, L. Ye1,2, R. Huang1
1Peking University, Beijing, China
2Advanced Institute of Information Technology of Peking University, Hangzhou, China
3Nano Core Chip Electronic Technology, Hangzhou, China
SESSION 23 LIVE Q&As Thursday February 24th, 7:00 AM PST

Frequency Synthesizers
Session Chair: Jun Yin, University of Macau, Taipa, Macau
Session Co-Chair: Jeremy Dunworth, Qualcomm Technologies, La Jolla, CA

7:00 AM
23.1  A Cascaded PLL (LC-PLL + RO-PLL) with a Programmable Double Realignment Achieving 204fs Integrated Jitter (100kHz to 100MHz) and -72dB Reference Spur
T-H. Tsai1, R-B. Sheen1, S-Y. Hsu1, Y-T. Chang1, C-H. Chang1, R. B. Staszewski2
1TSMC, Hsinchu, Taiwan
2University College Dublin, Dublin, Ireland

7:10 AM
23.2  A 188fsrms-Jitter and –243dB-FoMjitter 5.2GHz-Ring-DCO-Based Fractional-N Digital PLL with a 1/8 DTC-Range-Reduction Technique Using a Quadruple-Timing-Margin Phase Selector
C. Hwang*, H. Park*, T. Seong, J. Choi
*Equally-Credited Authors (ECAs), KAIST, Daejeon, Korea

7:20 AM
23.3  A 2.6-to-4.1GHz Fractional-N Digital PLL Based on a Time-Mode Arithmetic Unit Achieving -249.4dB FoM and -59dBc Fractional Spurs
Z. Gao1, J. He1, M. Fritz2, J. Gong1, Y. Shen1, Z. Zong1, P. Chen3, G. Spalink2, B. Eite2, K. Yamamoto4, R. B. Staszewski1,3, M. S. Alavi1, M. Babaie1
1Delft University of Technology, Delft, The Netherlands
2Sony Europe, Stuttgart, Germany
3University College Dublin, Dublin, Ireland
4Sony Semiconductor Solutions, Atsugi, Japan

7:30 AM
23.4  A 100MHz-Reference, 8GHz/16GHz, 177fsrms/223fsrms RO-Based IL-ADPLL Incorporating Reference Octupler with Probability-Based Fast Phase-Error Calibration
H. Kim1, H-S. Oh2, W. Jung1, Y. Song1, J. Oh3, D-K. Jeong1
1Seoul National University, Seoul, Korea
2University of California, Berkeley, CA
3Columbia University, New York, NY

7:40 AM
23.5  A Sub-100MHz Reference-Driven 25-to-28GHz Fractional-N PLL with -250dB FoM
D. Yang1, D. Murphy1, H. Darabi1, A. Behzad1, A. Abid2, S. Au1, S. Mundlapudi1, K. Shi2, W. Leng2
1Broadcom, San Jose, CA
2University of California, Los Angeles, CA

7:50 AM
23.6  A 68.6fsrms-Total-Integrated-Jitter and 1.56μs-Locking-Time Fractional-N Bang-Bang PLL Based on Type-II Gear Shifting and Adaptive Frequency Switching
S. M. Dartizio*1, F. Buccoleri*1, F. Tesolini1, L. Avallone2, A. Santiccioli1, A. Iesurum3, G. Steffan2, D. Chernaia2, L. Bertulessi1, A. Bevilacqua2, C. Samori1, A. L. Lacaita2, S. Levantino1
*Equally-Credited Authors (ECAs)
1Politecnico di Milano, Milan, Italy
2Infineon Technologies, Villach, Austria
3University of Padova, Padova, Italy

8:00 AM
23.7  A 25.8GHz Integer-N PLL with Time-Amplifying Phase-Frequency Detector Achieving 60fsrms Jitter, -252.8dB FoM, and Robust Lock Acquisition Performance
X. Geng, Y. Tian, Y. Xiao, Z. Ye, Q. Xie, Z. Wang
University of Electronic Science and Technology of China, Chengdu, China
Low-Power and UWB Radios for Communication and Ranging

Session Chair: Maryam Tabesh, Google, Mountain View, CA
Session Co-Chair: Jan Prummel, Dialog Semiconductor B.V., A Renesas Company, ’s-Hertogenbosch, The Netherlands

7:00 AM

24.1 A Long-Range Narrowband RF Localization System with a Crystal-Less Frequency-Hopping Receiver
C-W. Tseng¹, D. Komma¹, K-Y. Chen¹, R. Rothe¹, Z. Feng¹, M. Yasuda², M. Kawaminami², H-S. Kim¹, D. Blaauw¹
¹University of Michigan, Ann Arbor, MI
²United Semiconductor Japan, Kuwana, Japan

7:10 AM

24.2 A 1.66Gb/s and 5.8pJ/b Transcutaneous IR-UWB Telemetry System with Hybrid Impulse Modulation for Intracortical Brain-Computer Interfaces
M. Song¹, Y. Huang¹, Y. Shen¹, C. Shi²³, A. Breeschoten¹, M. Konijnenburg¹, H. Visser¹, J. Romme¹, B. Dutta¹, M. S. Alavi³, C. Bachmann¹, Y-H. Liu¹
¹imec-Netherlands, Eindhoven, The Netherlands
²Delft University of Technology, Delft, The Netherlands
³Eindhoven University of Technology, Eindhoven, The Netherlands

7:20 AM

24.3 A 6.5-to-10GHz IEEE 802.15.4/4z-Compliant 1T3R UWB Transceiver
Newradio Technology, Shenzhen, China

7:30 AM

24.4 A 22nm 0.84mm² BLE Transceiver with Self IQ-Phase Correction Achieving 39dB Image Rejection and On-Chip Antenna Impedance Tuning
K. Shibata, H. Matsui, H. Asano, Y. Kusaka, K. Ueda, N. Matsuno, H. Sato
Renesas Electronics, Tokyo, Japan

7:40 AM

24.5 A 266μW Bluetooth Low-Energy (BLE) Receiver Featuring an N-Path Passive Balun-LNA and a Pipeline Down-Mixing BB-Extraction Scheme Achieving 77dB SFDR and -3dBm OOB-B-1dB
H. Shao¹, P-I. Mak¹, G. QF, R. P. Martins¹³
¹University of Macau, Macau, China
²Sun Yat-Sen University, Zhuhai, China
³University of Lisboa, Lisbon, Portugal

7:50 AM

24.6 A 110μW 2.5kb/s -103dBm-Sensitivity Dual-Chirp Modulated ULP Receiver Achieving -41dB SIR
M. Moosavifar¹, J. Im¹, T. Odelberg, D. Wentzloff
¹Equally-Credited Authors (ECAs)
University of Michigan, Ann Arbor, MI

8:00 AM

24.7 An LPWAN Radio with a Reconfigurable Data/Duty-Cycled-Wake-Up Receiver
K-M. Kim¹, K-S. Choi¹, H. Jung¹², B. Yun¹, S. Kim², W. Oh², E-S. Lee³, S. Park², E-R. Jeong³, J. Ko², S-G. Lee¹
¹KAIST, Daejeon, Korea
²PHYCHIPS, Daejeon, Korea
³Hanbat National University, Daejeon, Korea
Noise-Shaping ADCs

Session Chair: Dominique Morche, CEA-LETI, Grenoble, France
Session Co-Chair: Yan Zhu, University of Macau, Taipa, Macau

7:00 AM
25.1 A 4.4μW 2.5kHz-BW 92.1dB-SNDR 3rd-Order VCO-Based ADC with Pseudo Virtual Ground Feedforward Linearization
C. Pochet, D. Hall
University of California, San Diego, CA

7:10 AM
25.2 A 2.87μW 1kHz-BW 94.0dB-SNDR 2-0 MASH ADC using FIA with Dynamic-Body-Biasing Assisted CLS Technique
Y. Hu1, Y. Zhao1, W. Qu1, L. Ye2, M. Zhao1, Z. Tan1
1Zhejiang University, Hangzhou, China
2Peking University, Beijing, China

7:20 AM
25.3 A 0.0375mm2 203.5μW 108.8dB DR DT Single-Loop DSM Audio ADC Using a Single-Ended Ring-Amplifier-Based Integrator in 180nm CMOS
C. Y. Lee, U-K. Moon
Oregon State University, Corvallis, OR

7:30 AM
25.4 A 5GS/s 360MHz-BW 68dB-DR Continuous-Time 1-1-1 Filtering MASH ΔΣ ADC in 40nm CMOS
Q. Liu1,2, L. Breems1,2, C. Zhang1,2, S. Bajoria1,2, M. Bolatkale2,3, R. Rutten2, G. Radulov1
1Eindhoven University of Technology, Eindhoven, The Netherlands
2NXP Semiconductors, Eindhoven, The Netherlands
3Delft University of Technology, Delft, The Netherlands

7:40 AM
25.5 A 28nm 6GHz 2b Continuous-Time ΔΣ ADC with -101dBc THD and 120MHz Bandwidth Using Digital DAC Error Correction
M. Bolatkale1, R. Rutten1, H. Brekelmans1, S. Bajoria1, Y. Gao2, B. Burdiek2, L. Breems1
1NXP Semiconductors, Eindhoven, The Netherlands
2NXP Semiconductors, Hamburg, Germany

7:50 AM
T. Wang, T. Xie, Z. Liu, S. Li
Georgia Institute of Technology, Atlanta, GA
SE3: Semiconductor Supply Chain

Organizers: Rahul M. Rao, IBM, Bangalore, India
Co-Organizers: Mijunh Noh, Samsung Electronics, Hwaseong-si, Korea
Massimo Alioto, National University of Singapore, Singapore
Chia-Hsiang Yang, National Taiwan University, Taipei, Taiwan
Moderator: Jimmy Goodrich, Semiconductor Industry Association, Washington, DC

The Semiconductor supply chain is a highly specialized global complex system stretching from design houses to manufacturing fabs, to test and assembly units, and integration factories, which varies by the nature of the company, market and product. The pandemic of 2020, with component shortages, along with the geopolitical trade conflicts, and the threat of counterfeiting, have highlighted the challenges and need for a better orchestrated and diversified management chain. This panel will highlight the risks ahead, and ways to get ahead of these challenges through market awareness, transparency, open platforms, global supplier landscape, and academic research.

Panelists:
Shawn Han, Samsung Foundry, Seoul, Korea
Jung Yoon, IBM, Poughkeepsie, NY
Bindiya Vakil, Resilinc, Milpitas, CA
Michael Reiha, Soitec Microelectronics, Singapore
Fredrik Tillman, Ericsson, Lund, Sweden
Willy C. Shih, Harvard Business School, Boston, MA

SE4: The Bright and Dark Side of Artificial Intelligence (AI)

Co-Organizers: Denis Daly, Apple, Cambridge, MA
Sriram Vangal, Intel, Hillsboro, OR
Jae-sun Seo, Arizona State University, Tempe, AZ
Moderator: Tinoosh Mohsenin, University of Maryland, Baltimore, MD

What is the golden vision for futuristic AI platforms? What are compelling AI use-cases and where are the risks? For instance, AI holds a great deal of promise for cybersecurity and human-centric robots. However, these sectors also have some of the highest potential for fallout. The panel will discuss forward-looking policy developments and ethical, legal, and societal issues related to AI, including socio-economic challenges.

Panelists:
Kailash Gopalakrishnan, IBM T. J. Watson Research Center, Yorktown Heights, NY
Evgeni Gousev, Qualcomm, San Diego, CA
Nele Mentens, KU Leuven, Leuven, Belgium, and Leiden University, Leiden, The Netherlands
Robert Muchsel, Analog Devices, Dallas, TX
Lama Nachman, Intel, Santa Clara, CA
Hoi-Jun Yoo, KAIST, Daejeon, Korea
SESSION 27 LIVE Q&As

Thursday February 24th, 7:00 AM PST

mm-Wave & Sub-6GHz Receivers and Transceivers for 5G Radios

Session Chair: Shahriar Shahramian, Nokia – Bell Labs, New Providence, NJ
Session Co-Chair: Byung-Wook Min, Yonsei University, Seoul, Korea

7:00 AM

27.1 A 16-Channel, 28/39GHz Dual-Polarized 5G FR2 Phased-Array Transceiver IC with a Quad-Stream IF Transceiver Supporting Non-Contiguous Carrier Aggregation up to 1.6GHz BW

A. Verma1, V. Bhagavatula1, A. Singh1, W. Wu1, H. Nagarajan1, P-K. Lau1, X. Yu1, O. Elsayed1, A. Jain1, A. Sarkar1, F. Zhang1, C-C. Kuo1, P. McElwee1, P-Y. Chiang1, C. Guo1, Z. Bai1, T. Chang1, A. Mann1, A. Rydin1, X. Zhao1, J. Lee2, D. Yoon2, C-W. Yao1, S. I. Lu1, S. W. Son1, T. B. Cho2

1Samsung Semiconductor, San Jose, CA
2Samsung Electronics, Hwaseong, Korea

7:10 AM

27.2 A Power-Efficient 24-to-71GHz CMOS Phased-Array Receiver Utilizing Harmonic-Selection Technique Supporting 36dB Inter-Band Blocker Rejection for 5G NR

J. Pang, Y. Zhang, Z. Li, M. Tang, Y. Liao, A. A. Fadila, A. Shirane, K. Okada
Tokyo Institute of Technology, Tokyo, Japan

7:20 AM

27.3 A 24-to-30GHz 256-Element Dual-Polarized 5G Phased Array with Fast Beam-Switching Support for >30,000 Beams

B. Sadhu1, A. Paidimarri1, W. Lee1, M. Yeck1, C. Ozdag1, Y. Tojo2, J-O. Plouchart1, X. Gu1, Y. Uemichi2, S. Chakraborty1, Y. Yamaguchi1, N. Guan2, A. Valdes-Garcia1

1IBM T. J. Watson Research Center, Yorktown Heights, NY
2Fujikura, Sakura, Japan

7:30 AM

27.4 A Hybrid Coupler-First 5GHz Noise-Cancelling Dual-Mode Receiver with +10dBm In-Band IIP3 in Current-Mode and 1.7dB NF in Voltage-Mode

Nanyang Technological University, Singapore, Singapore

7:40 AM

27.5 A Single-Path Digital-IF Receiver Supporting Inter/Intra 5-CA with a Single Integer LO-PLL in 14nm CMOS FinFET

Samsung Electronics, Hwaseong, Korea
SESSION 28 LIVE Q&As Thursday February 24th, 7:00 AM PST

DRAM and Interface

Session Chair: Bor-Doou Rong, Etron, Hsinchu, Taiwan
Session Co-Chair: Hye-Ran Kim, Samsung Electronics, Hwasung, Korea

7:00 AM

28.1 A 192-Gb 12-High 896-GB/s HBM3 DRAM with a TSV Auto-Calibration Scheme and Machine-Learning-Based Layout Optimization
SK hynix, Icheon, Korea

7:10 AM

28.2 A 16Gb 27Gb/s/pin T-coil based GDDR6 DRAM with Merged-MUX TX, Optimized WCK Operation, and Alternative-Data-Bus
Samsung Electronics, Hwaseong, Korea

28.3 A 16Gb 9.5Gb/s/pin LPDDR5X SDRAM with Low-Power Schemes Exploiting Dynamic Voltage-Frequency Scaling and Offset-Calibrated Readout Sense Amplifiers in a Fourth Generation 10nm DRAM Process
Samsung Electronics, Hwaseong, Korea

7:20 AM

28.4 A 20 Gb/s/pin 1.18pJ/b 1149μm² Single-Ended Inverter-based 4-tap Addition-Only Feed-Forward Equalization Transmitter with Improved Robustness to Coefficient Errors in 28nm CMOS
C. Moon, J. Seo, M. Lee, I. Jang, B. Kim, Pohang University of Science and Technology, Pohang, Korea

7:40 AM

28.5 A 0.385-pJ/bit 10-Gb/s TIA-Terminated Di-Code Transceiver with Edge-Delayed Equalization, ECC, and Mismatch Calibration for HBM Interfaces
H. Park1, Y. Choi1, J. Sim1, J. Choi1, Y. Kwon1, J. Song2, C. Kim3
1Korea University, Seoul, Korea; 2Incheon National University, Incheon, Korea

7:50 AM

28.6 A 78.8-fJ/b/mm 12.0-Gb/s/Wire Capacitively Driven On-Chip Link Over 5.6mm with an FFE-Combined Ground-Forcing Biasing Technique for DRAM Global Bus Line in 65nm CMOS
S. Lee, J. Yun, S. Kim, Seoul National University, Seoul, Korea

8:00 AM

28.7 A 20-Gb/s/pin 0.0024-mm² Single-Ended DECS TRX with CDR-less Self-Slicing/Auto-Deserialization to Improve Tolerance on Duty Cycle Error and RX Supply Noise for DCC/CDR-less Short-Reach Memory Interfaces
J. Seo1, S. Lee2, M. Lee1, C. Moon1, B. Kim1
1Pohang University of Science and Technology, Pohang, Korea
2Samsung Electronics, Hwaseong, Korea

8:10 AM

28.8 A Supply-Noise-Induced Jitter-Cancelling Clock Distribution Network for LPDDR5 Mobile DRAM featuring a 2nd-order Adaptive Filter
Y. Jung1,*, S. Lee1,*, H. Kim3, S. Cho3, *Equally-Credited Authors (ECAs)
1Samsung Electronics, Hwaseong-si, Korea; 2SK hynix, Icheon, Korea
3Korea Aerospace Research Institute, Daejeon, Korea; 4KAIST, Daejeon, Korea
ML Chips for Emerging Applications
Session Chair: Jun Deguchi, Kioxia, Kawasaki, Japan
Session Co-Chair: Jae-sun Seo, Arizona State University, Tempe, AZ

8:30 AM

29.1 184QPS/W 64Mb/mm² 3D Logic-to-DRAM Hybrid Bonding with Process-Near-Memory Engine for Recommendation System
D. Niu¹, S. Li¹, Y. Wang¹, W. Han¹, Z. Zhang², Y. Guan², T. Guan², F. Sun¹, F. Xue¹, L. Duan¹, Y. Fang¹, H. Zheng¹, X. Jiang¹, S. Wang¹, F. Zuo¹, Y. Wang¹, B. Yu¹, Q. Ren¹, Y. Xie¹
¹Alibaba DAMO Academy, Sunnyvale, CA
²Alibaba DAMO Academy, Beijing, China

8:40 AM

29.2 A 28nm 27.5TOPS/W Approximate-Computing-Based Transformer Processor with Asymptotic Sparsity Speculating and Out-of-Order Computing
Y. Wang¹, Y. Qin¹, D. Deng¹, J. Wei¹, Y. Zhou¹, Y. Fan¹, T. Chen², H. Sun¹, L. Liu¹, S. Wei¹, S. Yin¹
¹Tsinghua University, Beijing, China
²Tsing Micro, Beijing, China

8:50 AM

29.3 A 28nm 15.59μJ/Token Full-Digital Bitline-Transpose CIM-Based Sparse Transformer Accelerator with Pipeline/Parallel Reconfigurable Modes
F. Tu¹², Z. Wu¹, Y. Wang¹, L. Liang², L. Liu², Y. Ding², L. Liu², S. Wei¹, Y. Xie², S. Yin¹
¹Tsinghua University, Beijing, China
²University of California, Santa Barbara, CA

9:00 AM

29.4 ReckOn: A 28nm Sub-mm² Task-Agnostic Spiking Recurrent Neural Network Processor Enabling On-Chip Learning over Second-Long Timescales
C. Frenkel, G. Indiveri
University of Zurich and ETH Zurich, Zurich, Switzerland
Power Management Techniques
Session Chair: Min Chen, Analog Devices, Santa Clara, CA
Session Co-Chair: Li Geng, Xi’an Jiaotong University, Xi’an, China

8:30 AM
S. Li, X. Liu, B. H. Calhoun
University of Virginia, Charlottesville, VA

8:40 AM
30.2 A 130V Triboelectric Energy-Harvesting Interface in 180nm BCD with Scalable Multi-Chip-Stacked Bias-Flip and Daisy-Chained Synchronous Signaling Technique
KAIST, Daejeon, Korea

8:50 AM
30.3 A Reconfigurable Series-Parallel Charger for Dual-Battery Applications with 89W 97.7% Efficiency in Direct Charging Mode
Samsung Electronics, Hwaseong, Korea

9:00 AM
30.4 A 0.76V $V_{th}$ Triode Region 4A Analog LDO with Distributed Gain Enhancement and Dynamic Load-Current Tracking in Intel 4 CMOS Featuring Active Feedforward Ripple Shaping and On-Chip Power Noise Analyzer
Intel, Portland, OR
Audio Amplifiers

Session Chair: Qinwen Fan, Delft University of Technology, Delft, The Netherlands
Session Co-Chair: Mahdi Kashmiri, Broadcom, San Jose, CA

8:30 AM

31.1 A -117dBc THD (-132dBc HD3) and 126dB DR Audio Decoder with Code-Change-Insensitive RT-DEM Algorithm and Circuit Technique for Relaxing Velocity Saturation Effect of Poly Resistors
MediaTek, Hsinchu, Taiwan

8:40 AM

31.2 A 121.4dB DR, -109.8dB THD+N Capacitively-Coupled Chopper Class-D Audio Amplifier
H. Zhang¹, M. Berkhout², K. A. A. Makinwa¹, Q. Fan¹
¹Delft University of Technology, Delft, The Netherlands
²Goodix Technology, Nijmegen, The Netherlands

8:50 AM

31.3 A 121dB DR, 0.0017% THD+N, 8× Jitter-Effect Reduction Digital-Input Class-D Audio Amplifier with Supply-Voltage-Scaling Volume Control and Series-Connected DSM
W-H. Sun, S-H. Chien, T-H. Kuo
National Cheng Kung University, Tainan, Taiwan

9:00 AM

31.4 A -91dB THD+N Resistor-Less Class-D Piezoelectric Speaker Driver Using a Dual Voltage/Current Feedback for LC Resonance Damping
S. Karmakar¹, M. Berkhout ², K. A. A. Makinwa¹, Q. Fan¹
¹Delft University of Technology, Delft, The Netherlands
²Goodix Technology, Nijmegen, The Netherlands
Ultrasound and Beamforming Applications
Session Chair: Jun-Chau Chien, National Taiwan University, Taipei, Taiwan
Session Co-Chair: Jerald Yoo, National University of Singapore, Singapore, Singapore

8:30 AM
32.1 BatDrone: A 9.83M-focal-points/s 7.76μs-Latency Ultrasound Imaging System with On-Chip Per-Voxel RX Beamfocusing for 7m-Range Drone Applications
*Equally-Credited Authors (ECAs)
1National University of Singapore, Singapore, Singapore
2University of California, Berkeley, CA
3Digipen Institute of Technology, Singapore, Singapore
4Southern University of Science and Technology, Shenzhen, China
5The N.1 Institute for Health, Singapore, Singapore

8:40 AM
32.2 A Pitch-Matched ASIC with Integrated 65V TX and Shared Hybrid Beamforming ADC for Catheter-Based High-Frame-Rate 3D Ultrasound Probes
1Delft University of Technology, Delft, The Netherlands
2Erasmus MC, Rotterdam, The Netherlands

8:50 AM
32.3 A 1.2mW/channel 100μm-Pitch-Matched Transceiver ASIC with Boxcar-Integration-Based RX Micro-Beamformer for High-Resolution 3D Ultrasound Imaging
1Delft University of Technology, Delft, The Netherlands
2Erasmus MC, Rotterdam, The Netherlands

9:00 AM
32.4 An Electronically Tunable Multi-Frequency Air-Coupled CMUT Receiver Array with sub-100μPa Minimum Detectable Pressure Achieving a 28kb/s Wireless Uplink Across a Water-Air Interface
A. Singhvi, A. Fitzpatrick, A. Arbabian
Stanford University, Stanford, CA

9:10 AM
32.5 A Multimode 157μW 4-Channel 80dBA-SNDR Speech-Recognition Frontend with Self-DOA Correction Adaptive Beamformer
T. Kang, S. Lee, S. Song, M. R. Haghighat, M. P. Flynn
*Equally-Credited Authors (ECAs)
1University of Michigan, Ann Arbor, MI
2Intel, Santa Clara, CA
Domain-Specific Processors
Session Chair: Sanu Mathew, Intel, Portland, OR
Session Co-Chair: Chia-Hsiang Yang, National Taiwan University, Taipei, Taiwan

8:30 AM

33.1 A 1.05A/m Minimum Magnetic Field Strength Single-Chip Fully Integrated Biometric Smart Card SoC Achieving 1014.7ms Transaction Time with Anti-Spoofing Fingerprint Authentication
Samsung Electronics, Hwaseong, Korea

8:40 AM

33.2 A 96.2nJ/class Neural Signal Processor with Adaptable Intelligence for Seizure Prediction
Y-Y. Hsieh, Y-C. Lin, C-H. Yang
National Taiwan University, Taipei, Taiwan

8:50 AM

33.3 A HD 31fps 7×7-View Light-Field Factorization Processor for Dual-Layer 3D Factored Display
National Tsing Hua University, Hsinchu, Taiwan

9:00 AM

33.4 DSPU: A 281.6mW Real-Time Depth Signal Processing Unit for Deep Learning-Based Dense RGB-D Data Acquisition with Depth Fusion and 3D Bounding Box Extraction in Mobile Platforms
D. Im, G. Park, Z. Li, J. Ryu, S. Kang, D. Han, J. Lee, H-J. Yoo
KAIST, Daejeon, Korea
34.1 A 28nm 48KOPS 3.4μJ/Op Agile Crypto-Processor for Post-Quantum Cryptography on Multi-Mathematical Problems
Y. Zhu¹, W. Zhu¹, M. Zhu², C. Li¹, C. Deng¹, C. Chen¹, S. Yin¹, S. Yin¹, S. Wei¹, L. Liu¹
¹Tsinghua University, Beijing, China
²Micro Innovation Integrated Circuit Design, Wuxi, China

34.2 Side-Channel Attack Counteraction via Machine Learning-Targeted Power Compensation for Post-Silicon HW Security Patching
Q. Fang*¹, L. Lin*¹,², Y. Z. Wong¹, H. Zhang¹, M. Alioto¹
*Equally-Credited Authors (ECAs)
¹National University of Singapore, Singapore, Singapore
²Southern University of Science and Technology, Shenzhen, China

34.3 ShieldNN: A Threshold-Implementation-Based Neural-Network Accelerator Securing Model Parameters and Inputs Against Power Side-Channel Attacks
S. Maji¹, U. Banerjee², S. H. Fuller¹,², A. P. Chandrakasan¹
¹Massachusetts Institute of Technology, Cambridge, MA
²Indian Institute of Science, Bengaluru, India
³Analog Devices, Wilmington, MA

34.4 An 8.3-to-18Gbps Reconfigurable SCA-Resistant/Dual-Core/Blind-Bulk AES Engine in Intel 4 CMOS
R. Kumar, V. B. Suresh, M. A. Anders, S. K. Hsu, A. Agarwal, V. K. De, S. K. Mathew
Intel, Hillsboro, OR
As AI network- and dataset-sizes keep growing, the flow of data – from various tiers of the memory hierarchy to the compute-engines, and back – becomes critically important. In the worst-case, this data-flow can start to constrain further improvements in both system-performance and the energy-efficiency of future AI processing systems.

The idea of processing data at the spot where it is stored or generated, instead of moving it back and forth, has led to a broad variety of promising compute-in-x system concepts; where, x can be a memory array, a memory die, a memory package, the storage, a sensor, the network, etc.

This forum will highlight the state-of-the-art for several such compute-in-x system concepts, as well as related in-the-near-future challenges and opportunities for the SSCS community.

**Agenda**

<table>
<thead>
<tr>
<th>Time</th>
<th>Topic</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:00 AM</td>
<td>Introduction</td>
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<tr>
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<td><em>Kyu-Hyun (KH) Kim</em>, IBM T. J. Watson, Yorktown Heights, NY</td>
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<tr>
<td>7:15 AM</td>
<td>AI Memory Challenges and How to Solve Them For Data-Flow Accelerators</td>
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<td><em>Swagath Venkataramani</em>, IBM T. J. Watson, Yorktown Heights, NY</td>
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<td>7:30 AM</td>
<td>Nano-System for AI:</td>
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<td><em>N3XT 3D with Dense-Memory, Illusion-Scaleup, Co-Design</em></td>
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<td><em>Subhasish Mitra</em>, Stanford University, Stanford, CA</td>
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<tr>
<td>7:45 AM</td>
<td>Computing In and Near Memory: Practical Challenges and Future Directions</td>
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<td><em>Nam Sung Kim</em>, University of Illinois, Urbana, IL</td>
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<td>8:00 AM</td>
<td>Future Prospects of Computing In or Near Flash Memories</td>
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<td><em>Hang-Ting (Oliver) Lue</em>, Macronix International, Hsinchu, Taiwan</td>
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<tr>
<td>8:15 AM</td>
<td>We’ve Rethought Our Commute; Can We Rethink Our Data’s Commute?</td>
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<td><em>Frank Hady</em>, Intel, Portland, OR</td>
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<tr>
<td>8:30 AM</td>
<td>6G: Convergence of Communication, Computing, Control and Sensing</td>
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<td><em>Mallik Tatipamula</em>, Ericsson, Santa Clara, CA</td>
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<td>8:45 AM</td>
<td>Charge-Domain Signal Compression in Ultra-High-Speed CMOS Image Sensors</td>
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<td><em>Keiichiro Kagawa</em>, Shizuoka University, Hamamatsu, Japan</td>
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<td>9:00 AM</td>
<td>Neuromorphic Computing</td>
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<td><em>Steve B. Furber</em>, The University of Manchester, Manchester, United Kingdom</td>
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</table>
The Internet of Things is currently in the process of transitioning from concept to execution, and yet, many technical challenges remain. In particular, emerging IoT devices require increasingly small form factors and therefore must consume very low power, all while operating in congested wireless environments with security designed-in from the ground up. Emerging devices also require built-in machine-learning capabilities in tiny footprints while consuming low power.

This forum covers topics ranging from how to build energy-efficient yet long-range and robust IoT-centric wireless links, how to build low-power sensor interfaces, how to design physically and cryptographically-secure protocols, how to integrate signal processing and machine learning into small nodes, and how to perform efficient yet compact power management/energy harvesting.

**Agenda**

<table>
<thead>
<tr>
<th>Time</th>
<th>Topic</th>
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<tr>
<td>7:00 AM</td>
<td>Introduction</td>
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<tr>
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<td><strong>Patrick Mercier</strong>, University of California, San Diego, CA</td>
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<tr>
<td>7:15 AM</td>
<td>Connecting Massive IoT in the New Decade and Beyond</td>
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<td><strong>Tinglan Ji</strong>, Qualcomm, San Diego, CA</td>
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<tr>
<td>7:30 AM</td>
<td>Sensor Interface, Analog, and Mixed-Signal Circuits for Miniaturized IoT Devices</td>
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<td><strong>Taekwang Jang</strong>, ETH Zurich, Zurich, Switzerland</td>
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<td>7:45 AM</td>
<td>Wide-Range Wireless Communication Circuits for NB-IoT and eMTC</td>
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<td><strong>Kim B. Östman</strong>, Nordic Semiconductor, Turku, Finland</td>
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<tr>
<td>8:00 AM</td>
<td>Low-Power Wireless Communication Technologies for Emerging Short-Range Internet-of-Things</td>
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<td><strong>Po-Han Peter Wang</strong>, Broadcom, San Diego, CA</td>
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<td>8:15 AM</td>
<td>Manufacturing Semiconductors is Complex. How About Manufacturing Secure Semiconductors?</td>
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<td><strong>Miroslav Knezevic</strong>, NXP, Austin, TX</td>
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<td>8:30 AM</td>
<td>Memory System Design to Innovate Edge Computing for IoT Devices</td>
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<td><strong>Takashi Ita</strong>, Renesas Electronics, Tokyo, Japan</td>
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<tr>
<td>8:45 AM</td>
<td>Energy-Constrained Tiny-ML for IoT Applications</td>
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<td><strong>Tony Tae-Hyoung Kim</strong>, Nanyang Technological University, Singapore, Singapore</td>
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<td>9:00 AM</td>
<td>Extending Battery Life Through Lower Iq without Compromising System Performance or Solution Size</td>
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<td><strong>Keith Kunz</strong>, Texas Instruments, Tucson, AZ</td>
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</table>
F3: The Path to 6G: Architectures, Circuits, Technologies for Sub-THz Communications, Sensing, and Imaging

Organizer:  
Giuseppe Gramegna, IMEC, Leuven, Belgium

Committee:  
Shuhei Amakawa, Hiroshima University, Higashihiroshima, Japan  
Matteo Bassi, Infineon Technologies, Villach, Austria  
Patrick Reynaert, KU Leuven, Leuven, Belgium  
Swaminathan Sankaran, Texas Instruments, Dallas, TX  
Ho-Jin Song, Pohang University of Science and Technology, Pohang, Korea

Champions:  
Andreia Cathelin, STMicroelectronics, Crolles, France  
Kostas Doris, NXP, Eindhoven, The Netherlands  
Chih-Ming Hung, MediaTek, Taipei, Taiwan

The demand for faster communications and wider coverage keeps fueling research towards 6G that will leverage higher frequencies within a broader application spectrum. This is stimulating rapid transformations and innovations in several fields, such as communication, sensing, and imaging. A wide range of new architectures, circuits and technologies are under investigation to support this trend. In this forum, experts will illuminate the way to the future of Sub-THz design and applications by transversally focusing on circuits, architectures, and also technology, packaging, and testing solutions.

Agenda

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<tr>
<th>Time</th>
<th>Topic</th>
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<tr>
<td>7:00 AM</td>
<td>Introduction</td>
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<td></td>
<td>Giuseppe Gramegna, IMEC, Leuven, Belgium</td>
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<tr>
<td>7:15 AM</td>
<td>6G Communications: Vision and Challenges</td>
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<td>Gary Xu, Samsung, Plano, TX</td>
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<tr>
<td>7:30 AM</td>
<td>Emerging Device and Heterogenous Integration Technologies for sub-THz Applications</td>
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<td>Nadine Collaert, IMEC, Leuven, Belgium</td>
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<td>7:45 AM</td>
<td>Highly Integrated D-Band Phased Arrays for 6G Wireless Communications</td>
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<td>Mohamed Elkhouly, Bell Laboratories, New Providence, NJ</td>
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<td>8:00 AM</td>
<td>Sub-Terahertz Transceivers in Silicon</td>
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<td>Minoru Fujishima, Hiroshima University, Higashi-Hiroshima, Japan</td>
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<tr>
<td>8:15 AM</td>
<td>ICs and Transceiver Module Design for 100-300GHz Wireless</td>
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<td>Mark J. W. Rodwell, University of California, Santa Barbara, CA</td>
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<tr>
<td>8:30 AM</td>
<td>Sub-THz InP-Based Wireless Connection Techniques Toward 6G</td>
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<td>Hiroshi Hamada, NTT DoCoMo, Yokosuka, Japan</td>
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<tr>
<td>8:45 AM</td>
<td>Measurement and Validation of Sub-THz Radios: What Will it Take?</td>
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<td>Roger Nichols, Keysight Technologies, Santa Rosa, CA</td>
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WITHDRAWN:  
Concepts, Architectures and Circuits for Sub-THz Sensing and Imaging
SPECIAL EVENTS  
Friday February 25th, 8:30 AM PST

**SE5: Shifting Tides of Innovation – Where is Cutting-Edge Research Happening Today?**

Organizers:  
Alicia Klinefelter, NVIDIA, Durham, NC  
Mingoo Seok, Columbia University, New York, NY

Co-Organizers:  
Sophia Shao, University of California, Berkeley, CA  
Chiraag Juvekar, Analog Devices, Cambridge, MA

Moderator:  
Alicia Klinefelter, NVIDIA, Durham, NC

As research becomes more complex, multidisciplinary and system oriented, the focal point of innovation has begun to shift. Resource constraints such as people per project or the cost of working in the latest technology node also impacts who can participate in cutting-edge research. Industry does not have strong incentives to publish their most innovative and competitive work, leaving many in the dark as to what the state of the art is within companies. Even within industry, innovation can come from research, product, or startups. On the academic side, funding bodies and trends can also impact the innovation process. How can we close this gap and who really has the edge? Is industry-guided academic research the way to get the best of both worlds? The traditional debate has been between academia and industry, but there are many more facets to the discussion. This panel explores a variety of perspectives of how innovation occurs across the industry.

Panelists:  
James Myers, Arm, Cambridge, United Kingdom  
Tezaswi Raja, NVIDIA, Santa Clara, CA  
Nam Sung Kim, University of Illinois, Urbana-Champaign, IL  
Scott Hanson, Ambiq, Austin, TX  
Christal Gordon, Booz Allen Hamilton, McLean, VA  
Thomas Parry, Systematic Design, Rotterdam, The Netherlands

**SE6: Next Trillion-Dollar Market**

Co-Organizers:  
Jane Gu, University of California, Davis, Davis, CA  
Wei-Zen Chen, National Yang Ming Chiao Tung University, Hsin-Chu, Taiwan  
Kazuko Nishimura, Panasonic, Moriguchi, Japan  
Patrick Mercier, University of California, San Diego, La Jolla, CA

Moderator:  
Tom Lee, Stanford University, Stanford, CA

Innovations and technologies, which impact humanity in many aspects, enable rapidly evolving and emerging applications: including 5G and beyond wireless communications, wireline communications, autonomous vehicle, sensing, artificial intelligence (AI), machine learning, internet of things (IoT), internet of everything (IoE), virtual reality (VR), augmented reality (AR), silicon photonics, quantum computing, etc. Which of these will be the next trillion-dollar market driver for chips?

A collection of distinguished experts, from various domains, had been assembled to discuss the challenges and opportunities for growth in multiple, potentially large, sectors; the enabling technologies in each sector; and the ones required, particularly, from the semiconductor industry, as well as their timelines and questions raised by you, the audience.

Panelists:  
Lawrence Loh, Mediatek, Hsinchu City, Taiwan  
Vladimir Stojanovic, University of California, Berkeley, Berkeley, CA  
Hayato Wakabayashi, Sony Semiconductor Solutions, Atsugi, Japan  
Nancy Shemwell, Trilogy Networks, Dallas, TX  
Bill Dally, NVIDIA, Incline Village, NV  
Jay Gambetta, IBM Quantum, Yorktown Heights, NY
F4: Paving the Way to 200Gb/s Transceivers

Organizers: Patrick Yue, Hong Kong University of Science and Technology, Clear Water Bay, Hong Kong
Sudip Shekhar, University of British Columbia, Vancouver, Canada

Committee: Thomas Toifl, Cisco Systems, Thalwil, Switzerland
Bo Zhang, Broadcom, Irvine, CA
Munehiko Nagatani, NTT, Kanagawa, Japan
Milin Zhang, Tsinghua University, Beijing, China

Champions: Franz Dielacher, Infineon Technologies, Villach, Austria
Bill Redman-White, HiLight Semiconductor, Southampton, United Kingdom

This Forum aims to provide a comprehensive background for the upcoming 200Gb/s electrical and optical links. Seven industry and academic experts will address the state of the art and offer insightful projections on related topics, including standards, circuits and technology. The Forum will begin with the design considerations for different standardizations of end-to-end channels at 224Gb/s. Next, the challenges and opportunities of serial transceiver design, signaling schemes beyond PAM4, equalization, DSP, and advanced forward-error-correction techniques will be presented. Switching gears to the technology side of things, advancements in silicon photonic technologies to support 200Gb/s operation will be discussed. A design example of a coherent optical transceiver will conclude the forum presentation.

Agenda

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<tr>
<th>Time</th>
<th>Topic</th>
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<tbody>
<tr>
<td>7:00 AM</td>
<td>Introduction, Patrick Yue, Hong Kong University of Science and Technology, Clear Water Bay, Hong Kong</td>
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<td>7:15 AM</td>
<td>224 Gb/s Transceiver, End-to-End Channels, and Standardizations, Mike Li, Intel, San Jose, CA</td>
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<tr>
<td>7:30 AM</td>
<td>200Gb/s Serial Transceiver Design: Challenges and Opportunities, Jonathan Rogers, Alphawave IP, Toronto, Canada</td>
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<td>7:45 AM</td>
<td>200Gb/s: Beyond PAM4, Gain Kim, DGIST, Daegu, Korea</td>
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<td>8:00 AM</td>
<td>DSP-Based Transceivers for 200Gb/s: Challenges and the Path Forward, Tamer Ali, Mediatek, Irvine, CA</td>
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<td>8:15 AM</td>
<td>Advanced FEC for 200Gb/s Transceiver Applications, Xinyuan Wang, Huawei Technologies, Beijing, China</td>
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<td>WITHDRAWN: Semiconductor Technology – the Path Forward for the Coming Decades</td>
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<td>8:30 AM</td>
<td>Silicon Photonics Technology for Next-Generation Transceivers, Joris Van Campenhout, IMEC, Leuven, Belgium</td>
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<tr>
<td>8:45 AM</td>
<td>Coherent Optical Transceivers for &gt;200Gb/s per Wavelength, Alex Rylyakov, Nokia, New York, NY</td>
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F5: How to Improve AI Efficiency Further: New Devices, Architectures and Algorithms

Organizers:  
Rangharajan Venkatesan, NVIDIA, Santa Clara, CA  
Alicia Klinefelter, NVIDIA, Durham, NC

Committee:  
Kea-Tiong Tang, National Tsing Hua University, Hsinchu, Taiwan  
Rui Huang, Peking University, Beijing, China  
Mingoo Seok, Columbia University, New York, NY  
Shidhartha Das, Arm, Cambridge, United Kingdom

Champions:  
Yan Li, Western Digital, Milpitas, CA  
Fatih Hamzaoglu, Intel, Hillsboro, OR

Machine learning (ML) algorithms and applications continue to evolve at a rapid pace relative to Moore’s Law. There is simultaneously a demand for bigger and more complex ML models, ever-growing computational throughput and improved energy efficiency over the coming decade. As we start to hit the limits of technology scaling, what are the latest design strategies to improve performance and energy efficiency of machine learning processors of the future? Further, can ML-based tools improve hardware design methodology? This forum aims to explore novel circuits, architectures, algorithms, as well as ML-based chip design tools that will push the limits of AI efficiency.

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<td>7:00 AM</td>
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<td><strong>Rangharajan Venkatesan</strong>, NVIDIA, Santa Clara, CA</td>
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<tr>
<td>7:15 AM</td>
<td>GPU Architectures for Efficient Deep Learning</td>
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<td><strong>Ronny Krashinsky</strong>, NVIDIA, Santa Clara, CA</td>
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<td>7:30 AM</td>
<td>Mixed-Signal Compute-in-Memory Processing for Energy Efficient Algorithms</td>
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<td><strong>Laura Fick</strong>, Mythic, Cedar Park, TX</td>
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<td>7:45 AM</td>
<td>Neuromorphic Intelligence: Using Populations of Inhomogeneous Spiking</td>
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<td>Neurons to Carry Out Robust Computation in Neuromorphic Processors</td>
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<td><strong>Giacomo Indiveri</strong>, University of Zurich and ETH Zurich, Zurich, Switzerland</td>
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<td>8:00 AM</td>
<td>Artificial Intelligence Processor Using Diffractive Photonic Computing</td>
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<td><strong>Xing Lin</strong>, Tsinghua University, Beijing, China</td>
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<td>8:15 AM</td>
<td>Quantization Techniques for Low-Precision Inference and Training</td>
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<td><strong>Kailash Gopalakrishnan</strong>, IBM Research, Yorktown Heights, NY</td>
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<td>8:30 PM</td>
<td>Graphs: Powerful But Hard to Beat</td>
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<td><strong>Stijn Eyerman</strong>, Intel, Kontich, Belgium</td>
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<td>8:45 PM</td>
<td>Acceleration for Graph Neural Network Inference</td>
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<td><strong>Sachin S. Sapatnekar</strong>, University of Minnesota, Minneapolis, MN</td>
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<tr>
<td>9:00 PM</td>
<td>Machine Learning in Chip Design Tools</td>
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<td><strong>Evangeline Young</strong>, Chinese University of Hong Kong, Shatin, Hong Kong</td>
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Present-day computer systems are increasingly under attack on multiple fronts with new vulnerabilities being discovered every day at system, architecture, memory and physical level. While countermeasures against such attacks exist, they often impose significant overheads in performance and power. This forum will give an overview of recent security vulnerabilities, including speculative side-channels, memory exploits, physical attacks and discuss the overheads of detecting/mitigating against them. The forum also includes post-quantum cryptographic algorithms and homomorphic encryption accelerators that promise very high security value propositions, while imposing orders-of-magnitude increase in computational complexity.

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<table>
<thead>
<tr>
<th>Time</th>
<th>Topic</th>
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| 7:00 AM | Introduction  
*Massimo Alioto*, National University of Singapore, Singapore |
| 7:15 AM | Overview of Security Challenges, Applications, Common Practice and Directions in SOC Design  
*Serge Leef*, Darpa, Bellevue, WA |
| 7:30 AM | Microarchitectural Side-Channel Attacks  
*Todd Austin*, University of Michigan, Ann Arbor, MI |
| 7:45 AM | Microarchitectural Vulnerabilities: Evolving Landscape  
*Carlos Rozas*, Intel, Portland, OR |
| 8:00 AM | DRAM Circuit Design for Protecting Natural/Artificial Faults and Reliability Degradation  
*Dongkyun Kim*, SK hynix, Icheon-si, Korea |
| 8:15 AM | Memory Architecture Mitigations and Impact on System-Level Performance  
*Ruby Lee*, Princeton University, Princeton, NJ |
| 8:30 AM | Physical Side-Channel Attacks and Counteraction Through Design Automation  
*Ileana Buhan*, Radboud University, Nijmegen, The Netherlands |
| 8:45 AM | Integrated Sense-and-React Countermeasures Against Physical Attacks  
*Noriyuki Miura*, Osaka University, Osaka, Japan |
| 9:00 AM | Hardware Implementation Challenges in Post-Quantum Encryption and Fully Homomorphic Encryption  
*Sujoy Sinha Roy*, Graz University of Technology, Graz, Austria |
Short Course: High Speed/High Performance Data Converters: Metrics, Architectures, and Emerging Topics

Q&A Time: Topic:

7:00 AM Introduction by Chair, Daniel Friedman
IBM Thomas J. Watson Research Center, Yorktown Heights, NY

7:05 AM Introduction to ADCs/DACs: Metrics, Topologies, Trade Space, and Applications
Boris Murmann, Stanford University, Stanford, CA

7:35 AM Ultra-High-Data-Rate ADCs and DACs: Architectures and Implementations
Gabriele Manganaro, MediaTek, Woburn, MA

8:05 AM High-Precision and Low-Power ADCs
Pieter Harpe, Eindhoven University of Technology, Eindhoven, The Netherlands

8:35 AM Emerging Data-Converter Concepts
Nan Sun, Tsinghua University, Beijing, China

Introduction
Data converters provide the gateway between the analog and digital worlds. They play a critical role in a vast range of systems, and integrated converters represent a central and growing element in high performance designs in applications from wireline to wireless and more. In this course, we start with an introduction to data converters, discussing key topologies, metrics, and the associated trade space. We continue with a discussion of ultra-high data rate converter design approaches before moving to high precision and low power converter topics. In our final session, we discuss emerging data converter concepts that will shape the future of research in this area.
**SC1: Introduction to ADCs/DACs: Metrics, Topologies, Trade Space, and Applications**

*Boris Murmann, Stanford University, Stanford, CA*

This presentation provides a short introduction to ADCs and DACs. The intent is to prepare the audience for the subsequent talks that will cover intricate details of modern, fine-tuned realizations. Topics include elementary data converter building blocks and their imperfections, converter topologies and their basic tradeoffs, performance metrics and figures of merit, as well as selected application aspects.

*Boris Murmann* is a Professor of Electrical Engineering at Stanford University. He joined Stanford in 2004 after completing his Ph.D. degree in electrical engineering at the University of California, Berkeley in 2003. From 1994 to 1997, he was with Neutron Microelectronics, Germany, where he developed low-power and smart-power ASICs in automotive CMOS technology. Since 2004, he has worked as a consultant with numerous Silicon Valley companies. Dr. Murmann’s research interests are in mixed-signal integrated circuit design, with special emphasis on sensor interfaces, data converters and embedded machine learning. He has served the Data Converter Subcommittee Chair and Technical Program Chair of the IEEE International Solid-State Circuits Conference (ISSCC). He is a Fellow of the IEEE.

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**SC2: Ultra-High-Data-Rate ADCs and DACs: Architectures and Implementations**

*Gabriele Manganaro, MediaTek, Woburn, MA*

Ten years ago or so, the term high-speed data converter was synonymous with sample rates on the order of a few hundreds of MHz, barring rare exceptions. Today, medium resolution ADCs (10-to-12b) and DACs clocked at tens of GHz, and even faster 6-to-8b converters, have been demonstrated without melting the die. So how could this level of advancement happen in the face of the end of Dennard scaling? The answer lies with the combination of architecture innovation and digital assistance. This presentation will give an overview of this rapidly (no pun intended) developing topic, aiming to illustrate the key design principles, their practical applicability, and will complement this material with examples of recently published multi-GSPS data converters.

*Gabriele Manganaro* (Fellow IEEE) holds a Dr. Eng. (1994) and a Ph.D. degree (1997) in Electronics from the University of Catania, Italy. He has worked in analog IC design, primarily in high-speed data converters design, both in Europe and the USA for over twenty years. He’s presently a Director of Technology at MediaTek in Woburn, Massachusetts. He has authored/co-authored more than 60 peer-reviewed papers, three books (notably “Advanced Data Converters”, Cambridge University Press, 2011) and has been granted 18 US patents, with more pending.
ADC designs are progressing rapidly over time in terms of architectural developments and circuit innovations. In this talk, we will focus on high-precision designs and on low-power design techniques of ADC topologies such as pipelined ADCs, Delta-Sigma modulators, and SAR (successive-approximation) ADCs. Besides discussing general challenges and solutions, some state-of-the-art ADC examples will be explained in the context of the principles outlined in this lecture, and a short review from a system integration perspective will be given.

Pieter Harpe received M.Sc. and Ph.D. degrees from the Eindhoven University of Technology, The Netherlands. He spent several years as a researcher at imec, The Netherlands, and joined Eindhoven University of Technology in 2011, where he is currently Associate Professor on low-power mixed-signal circuits. Dr. Harpe is co-organizer of the yearly AACC workshop, an analog subcommittee chair for the ESSCIRC conference, and the SSSC CONFedu program chair. He served as an ISSCC ITPC member, SSCS Distinguished Lecturer, and JSSC guest editor. He is a Senior Member of the IEEE and a recipient of the ISSCC 2015 Distinguished Technical Paper Award.

This talk presents several novel data-converter architectures, including hybrid ADCs that combine traditional architectures (e.g., a noise-shaping SAR) and Nyquist-rate ADCs with continuous-time (CT) front ends (e.g., a CT-pipe and CT-SAR). It also includes scaling-friendly time-domain ADCs that use digital gates to process analog signals. This talk also covers circuit-level innovations, including the use of open-loop and closed-loop dynamic amplifiers for residue amplification, as well as noise cancellation techniques that break the kT/C noise limit.

Nan Sun is a Professor of Electronic Engineering at Tsinghua University. He was Assistant and then Associate Professor with the University of Texas at Austin. He received the B.Sc. degree from Tsinghua University and the PhD degree from Harvard University. He received the NSF Career Award in 2013 and the IEEE SSCS New Frontier Award in 2020. He has graduated 24 PhDs (9 of whom are professors) and published 200 papers, including 30+ JSSC and 40+ ISSCC/VLSI/CICC papers. He serves on the TPC of CICC and A-SSCC. He served as an Associate Editor for IEEE TCAS-I and for JSSC. He also serves as a Distinguished Lecturer for the IEEE Circuits and Systems Society as well as for the IEEE Solid-State Circuits Society.
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