

# ADVANCE PROGRAM



## 2023 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

FEBRUARY  
19, 20, 21, 22, 23

### CONFERENCE THEME:

**BUILDING ON 70 YEARS OF  
INNOVATION IN SOLID-STATE  
CIRCUIT DESIGN**

**In  
PERSON  
EVENT**

SAN FRANCISCO  
MARRIOTT MARQUIS HOTEL

DRAFT 2-8-2023

### SUNDAY ALL-DAY

3 FORUMS: TRANSCIEVERS FOR EMASCALE; FUTURE OF AUTOMOTIVE TECHNOLOGY; WIRELESS POWER AMPLIFICATION

### 12 TUTORIALS:

FUNDAMENTALS OF FREQUENCY REFERENCES; BRIDGING RF AND POWER; FUNDAMENTALS OF DATA CONVERTERS; AUTOMOTIVE SYSTEM DESIGN; FUNDAMENTAL CONCEPTS TO FUTURE TRENDS; SOLID-STATE CMOS LIDAR; FUNDAMENTALS OF UL VOLTAGE; CURRENT-MODE PASSIVE MIXERS & N-PATH IN RF RECEIVERS; PHYSICAL-LAYER SECURITY FOR LATENCY; ART OF MM-WAVE; DIGITAL EQUALIZATION & TIMING RECOVERY; EXTENDING PROCESSOR CORES FOR ML

2 EVENING EVENTS: GRADUATE STUDENT RESEARCH IN PROGRESS; MENTORING SESSION/NETWORKING BRIG

### THURSDAY ALL-DAY

#### 4 FORUMS:

ADVANCING TECHNOLOGIES FOR XR; EXTREME DATA CONVERTERS;  
HETEROGENEOUS MULTI-CORE ARCHITECTURES FOR AI;  
WEARABLE & IMPLANTABLE DEVICES

#### SHORT-COURSE:

QUANTUM COMPUTING & THE APPLICATION OF CRYOELECTRONICS

**5-DAY  
PROGRAM**

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## ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and application to maintain technical currency, and to network with leading experts.

## CONFERENCE TECHNICAL HIGHLIGHTS

On Sunday, February 19th, the day before the official opening of the Conference, ISSCC 2023 offers:

- A choice of 12 Tutorials, or
- A choice of 1 of 3 all-day Advanced-Circuit-Design Forums:
  - "Transceivers for Exascale: Towards Tbps/mm and sub-pJ/bit"*
  - "The Power Behind Electrical Vehicles – Accelerating the Future of Automotive Technology"*
  - "Efficient Wireless Power Amplification and Linearization"*

The 90-minute tutorials offer background information and a review of the basics in specific circuit- and system-design topics. In the all-day Advanced-Circuit-Design Forums, leading experts present state-of-the-art design strategies in a workshop-like format. The Forums are targeted at designers experienced in the technical field.

On Sunday, February 19th, there are two events: "Mentoring Session/Networking Bingo" will be offered starting at 3:00 pm. In addition, the Student-Research Preview, featuring ninety-second introductory presentations followed by a poster session from selected graduate-student researchers from around the world will begin at 8:00 pm. The SRP will start with an inspirational lecture by Professor Mark Horowitz (Stanford University).

On Monday, February 20th, ISSCC 2023 at 8:30 am offers four plenary papers on the theme: *"Building on 70 Years of Innovation in Solid-State Circuit Design"*. On Monday at 1:30 pm, there are five parallel technical sessions, followed by a Social Hour at 5:15 pm open to all ISSCC attendees. The Social Hour, held in conjunction with Book Displays and Author Interviews, will also include a Demonstration Session, featuring posters and live demonstrations of selected papers from industry and academia. Monday evening includes two events, entitled, *"Integrated Circuits in an Interconnected World"* and *"The Path to Sustainable IC Ecosystems"*

On Tuesday, February 21st, there are five parallel technical sessions, both morning and afternoon. Book Displays and Author Interviews, will also include a second Demonstration Session. Tuesday evening includes two events, entitled: *"The Smartest Designer in The Universe, Post-Pandemic!"* and *"What will be the Essential Skills for IC Designers in the Next Decade?"*

On Wednesday, February 22nd, there will be five parallel technical sessions, both morning and afternoon, followed by Author Interviews.

On Thursday, February 23rd, ISSCC offers a choice of five all-day events:

- A Short Course entitled:
  - "Principles of Quantum Computing and the Application of Cryoelectronics to Qubit Control and Readout"*
- Four Advanced-Circuit-Design Forums entitled:
  - "Advancing Technologies for Extended Reality (XR) to Make the "Metaverse" Possible"*
  - "Extreme Data Converters and Their Peripherals"*
  - "The Future of Heterogeneous Multi-Core Architectures for AI and Other Specialized Processing"*
  - "Advanced Circuits and Technologies for Wearable and Implantable Devices"*

This year, again, there is an option which allows an attendee to sample parts of all 5 Thursday offerings. Registration for educational events on Sunday and Thursday will be filled on a first-come first-served basis. Use of the ISSCC Web-Registration Site (<http://www.isscc.org>) is strongly encouraged. Registrants will be provided with immediate confirmation on registration for the Conference, Tutorials, Forums, and the Short Course.

**Need Additional Information? Go to: [www.isscc.org](http://www.isscc.org)**

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### ISSCC 2023 Circuit Insights

**Organizer/Moderator:**     **Ali Sheikholeslami**, *University of Toronto, Toronto, Canada*  
   *ISSCC Education Chair*

ISSCC 2023 offers the second edition of its Circuit Insights on Saturday, Feb. 18, 2023, 7:30am -12:00pm PST. Like its initial debut in 2022, this event is targeting third-year undergraduate students and starting graduate students in the area of circuit design, but may be of interest to new circuit design engineers as well. The event will be held in person for a small audience of 50 students (by invitation only) at the ISSCC venue at the Marriott Hotel in San Francisco, and will be broadcast live via YouTube/Zoom worldwide. This event is free of charge but requires registration through [isscc.org/insights](https://isscc.org/insights).

The event consists of four 45-minute talks on fundamentals of Circuit Design, each to be followed by a 15-minute Q&A Session, with a 30-minute break after the second talk. The Q&A session will be interactive, entertaining questions from the in-person as well as the online attendees.

| Agenda      |  |
|-------------|--|
| <u>Time</u> | <u>Topic</u>   |
| 7:00 AM     | Light Breakfast  |
| 7:30 AM     | <b>Opening Remarks</b><br><b>Ali Sheikholeslami</b> , <i>Circuit Insights Organizer/Moderator</i>                                |
| 7:35 AM     | <b>Welcoming Remarks</b><br><b>Eugenio Cantatore</b> , <i>ISSCC Conference Chair</i><br><b>John Long</b> , <i>SSCS President</i> |
| 7:40 AM     | <b>The CMOS Latch</b><br><b>Asad Abidi</b> , <i>University of California, Los Angeles, CA</i>                                    |
| 8:25 AM     | Interactive Q & A  |
| 8:40 AM     | <b>The Art of Linear Analysis for Analog Circuits</b><br><b>Jaeha Kim</b> , <i>Seoul National University, Korea</i>              |
| 9:25 AM     | Interactive Q & A  |
| 9:40 AM     | Break  |
| 10:10 AM    | <b>The Basics of Low Noise Amplifiers</b><br><b>Rabia Yazicigil Kirby</b> , <i>Boston University, MA</i>                         |
| 10:55 AM    | Interactive Q & A  |
| 11:10 AM    | <b>The Basics of Analog-to-Digital Converters</b><br><b>Maurits Ortmanns</b> , <i>University of Ulm, Germany</i>                 |
| 11:55 AM    | Interactive Q & A  |
| 12:10 PM    | Attendees Feedback   |
| 12:20 PM    | Networking Lunch   |
| 1:30 PM     | Conclusion   |

There are a total of 12 tutorials this year on 12 different topics. Each tutorial, selected through a competitive process within each subcommittee of the ISSCC, presents the basic concepts and working principles of a single topic of broad interest. The tutorials are intended for non-experts, graduate students, and practicing engineers who wish to explore and understand a new topic. Tutorial registration bundles access to all 12 of the tutorials. Participants are asked to select between the option for only on-demand access to the tutorials (provided ahead of the conference) or the option to additionally attend a full-day live Q&A and networking session with the presenters during the conference, at no additional charge. The coordinators for the 2023 ISSCC Tutorials are (in the same order as the tutorials): Jens Anders (T1), Yan Lu (T2), Shahrzad Naraghi (T3), Chia-Hsiang Yang (T4), Eric J.-W. Fang (T5), Leonardo Gasparini (T6), Yih Wang (T7), Jeff Walling (T8), Noriyuki Miura (T9), Bodhisatwa Sadhu (T10), Byungsub Kim (T11), Jae-Sun Seo (T12).

**Naveen Verma**  
*ISSCC Tutorials Chair*

The presentations of all 12 tutorials will be available online, on-demand, as of:  
**Friday, Feb. 10, 2023, 5:00pm, PST**

**Live Q&A in person for the tutorials:**  
**Sunday Feb. 19, 2023**

**10:00 AM - Live Q&A in person - February 19**  
**T1: Fundamentals of Frequency References**  
*Danielle Griffith, Texas Instruments, Dallas, TX*

Frequency references are a fundamental building block in a vast array of electronic systems. This tutorial will introduce several types of oscillators commonly used as frequency references, including crystal and MEMS oscillators as well as fully-integrated oscillators. Classical circuit architectures and recent advances will be shown. The tutorial will focus on how system-level requirements influence the circuit-level architecture, the required frequency accuracy, power consumption, and other design targets. Design tradeoffs will be described for each oscillator type. At the end of this tutorial, attendees will have a solid understanding of frequency reference specifications, common oscillator architectures, tradeoffs, and recent innovations in the field.

**Danielle Griffith** received the B.S.E.E. and M.Eng. degrees from the Massachusetts Institute of Technology. She is currently a Fellow at Texas Instruments in Dallas, Texas. Her areas of expertise are circuits and architectures for efficient wireless systems, low power oscillators, and MEMS circuitry. She has published a book chapter and >50 papers, and holds 22 issued US patents. Danielle has presented at numerous conference tutorial and workshop sessions. She has been a TPC member for the RFIC, ISSCC, and VLSI conferences. She is a senior member of the IEEE, an associate editor of the IEEE JSSC, and a Distinguished Lecturer of the SSCS.

**10:20 AM - Live Q&A in person - February 19**  
**T2: Bridging RF and Power: An Introduction to Envelope Tracking Systems and Building Blocks**  
*Ji-Seon Paek, Pusan National University, Pusan, Korea*

Envelope tracking (ET) is a well-established power-management technique to improve the power efficiency of RF power amplifiers. This tutorial covers the principles of envelope-tracking operation, and the design of building blocks under ET-system link budget considerations. It develops the understanding of standard-specific system specifications, required by 3GPP and IEEE standards, to enable optimal design of each building block. Based on the understanding, various supply-modulator (SM) structures and power-management circuit techniques will be reviewed, which can efficiently power RF power amplifiers while meeting the requirements of wireless communication standards.

**Jiseon Paek** received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2004, 2006, and 2011, respectively. Since 2011, he has been with Samsung Electronics, where he leads various projects developing wireless RF transceivers, envelope tracking (ET) ICs, and fully integrated power ICs for mobile handset applications. Since 2022, he has been an Associate Professor in the Department of Electronics Engineering at Pusan National University (PNU), Korea. He is now serving on the power management sub-committee of ISSCC.

**10:40 AM - Live Q&A in person - February 19****T3: Fundamentals of Data Converters***Yun Chiu, University of Texas at Dallas, Richardson, TX*

A refreshing review of fundamental data-conversion principles and circuit techniques, ranging from the concepts of sampling and quantization, to flash, pipeline and SAR architectures, to common circuit building blocks, to time- and frequency-domain measurement techniques of converters, will be presented in this tutorial. An emphasis will be placed on performance robustness, digital correctability, and calibration in advanced process nodes. The tutorial will wrap up with a historic remark on and a future perspective of the ADC Figure-of-Merits.

**Yun Chiu** is an Erik Jonsson Distinguished Professor of the ECE Department of the University of Texas at Dallas, where he directs the Analog and Mixed-Signal Lab at the Texas Analog Center of Excellence. His industry experience includes working as a Senior Staff Member in a Silicon Valley startup in the late 90s and co-founding Formula Microelectronics in 2015 during his sabbatical leave. He has served on the technical program committees of VLSI-C, CICC, and A-SSCC. He is now serving on the data converter subcommittee of ISSCC. He received his Ph.D. from UC Berkeley.

**11:00 AM - Live Q&A in person - February 19****T4: Automotive System Design***Sugako Otani, Renesas Electronics, Tokyo, Japan*

The automotive industry is in the midst of a significant transformation. "CASE: Connected, Autonomous, Shared & Service, Electric" has been advocated as a trend. Along with this trend, automotive E/E (Electrical/Electronic) architecture has rapidly progressed toward ECU (Electronic Control Unit) integration and centralization in the autonomous driving era. The tutorial introduces automotive system design and key technologies of LSI devices, including processors for advanced vehicle control and cognitive/judgment processing. Multiple safety mechanisms for automotive functional safety are also covered.

**Sugako Otani** is a system and processor architect at Renesas Electronics Corporation. Her current research focuses on application-specific architectures, ranging from IoT devices to automotive. She joined Mitsubishi Electric Corporation, Japan, in 1995 after receiving an M.S. in physics from Waseda University, Tokyo. She received a Ph.D. in Electrical Engineering and Computer Science from Kanazawa University in 2015. From 2005 to 2006, she was a Visiting Scholar at Stanford University. She is a committee member of ISSCC, VLSI Symposium, ESSCIRC, and Cool Chips. Since 2019, she has been a Visiting Associate Professor at Nagoya University, Japan.

**11:20 AM - Live Q&A in person - February 19****T5: All-Digital PLLs:****From Fundamental Concepts to Future Trends***Akihide Sai, Toshiba, Kawasaki, Japan*

Frequency synthesis has become ubiquitous in chip designs for clocking, RF, and data sampling. Traditional analog PLLs have moved to digital implementations, for area, power, and technology portability. This tutorial describes the evolution of all-digital PLLs, from the basic digitization of oscillator control at integer ratios, to low-noise flexible fractional-N frequency synthesis with digital-to-time converters (DTCs). The evolution of two noise-critical blocks is described: time-to-digital converters (TDCs) and fractional dividers. This includes voltage-based TDCs, such as time amplifiers and successive-approximation-register (SAR) architectures, and various DTCs for fractional-divider noise reduction. It concludes with architectures at the limits of noise and size, namely bang-bang TDCs, and looks at future digital PLL trends. The presentation emphasizes key considerations for digital systems, including fast dynamic frequency scaling (DFS), fine resolution, and noise mitigation.

**Akihide Sai** received the B.E. and M.E. degrees from Waseda University, Tokyo, Japan, in 2002 and 2004, respectively. In 2004, he joined the Corporate Research and Development Center, Toshiba Corporation, Kawasaki, Japan. From 2004 to 2015, he has been engaged in the research and development of low-power transceivers and digital/analog phase-locked loops (PLLs). Since 2016, he has been a senior research scientist and a team leader of mixed-signal circuits for automobile LiDAR SoCs. He contributed to high-performance mixed-signal circuit and LiDAR system projects and co-authored more than 20 technical papers and patents.

### 11:40 AM - Live Q&A in person - February 19

#### T6: Solid-State CMOS LiDAR Sensors

*Seong-Jin Kim, Ulsan National Institute of Science and Technology, Ulsan, Korea*

This tutorial will present the technologies behind single-photon avalanche-diode (SPAD)-based solid-state CMOS LiDAR sensors that have emerged to realize level-5 automotive vehicles and the metaverse AR/VR in mobile devices. It will begin with the fundamentals of direct and indirect time-of-flight (ToF) techniques, followed by structures and operating principles of three key building blocks: SPAD devices, time-to-digital converters (TDCs), and signal-processing units for histogram derivation. The tutorial will finally introduce the recent development of on-chip histogramming TDCs with some state-of-the-art examples.

**Seong-Jin Kim** received a Ph.D. degree from KAIST, Daejeon, South Korea, in 2008 and joined the Samsung Advanced Institute of Technology to develop 3D imagers. From 2012 to 2015, he was with the Institute of Microelectronics, A\*STAR, Singapore, where he was involved in designing various sensing systems. He is currently an associate professor at Ulsan National Institute of Science and Technology, Ulsan, South Korea, and a co-founder of SolidVUE, a LiDAR startup company in South Korea. His current research interests include high-performance imaging devices, LiDAR systems, and biomedical interface circuits and systems.

### 1:00 PM - Live Q&A in person - February 19

#### T7: Fundamentals of Ultra-Low Voltage Embedded Memory Design

*Eric Karl, Intel, Portland, OR*

To meet the energy efficiency demands of future applications, system-on-chip (SoC) designs continue to march towards ultra-low-voltage operation. This tutorial will address the fundamental challenges for embedded memory operation at low voltages in advanced process technologies, and cover single and multi-port SRAM, logic flip-flop, logic latch arrays, and eFuse technologies, prevalent in embedded design use. Memory assist circuits, repair, error correction, multi-VCC array design, clocking and min-delay design strategies relevant to enabling ultra-low and near-threshold system operation will be explored. System designers will walk away with a stronger understanding of how to better navigate embedded memory usage in ultra-low-voltage designs.

**Eric Karl** is an Intel Fellow, Director of Advanced Design and Director of Embedded Memory Technology and Circuits. Karl leads the Advanced Design group in Intel's Technology Development organization, where he is responsible for standard-cell library architecture, memory and analog circuit technologies employed by all designers on Intel technology. Karl leads teams at Intel responsible for design technology co-optimization and develops a wide-range of circuits for early development test vehicles to enable technology development. Karl played a lead role in Intel's embedded memory technology development and the transition to FinFET technology in 2012. Karl holds doctoral, master's and bachelor's degrees in electrical engineering from the University of Michigan, Ann Arbor. He has published over 30 peer-reviewed technical papers, holds numerous patents and is currently serving on the memory subcommittee of the International Solid-State Circuits Conference (ISSCC).

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**1:20 PM - Live Q&A in person - February 19****T8: Role of Current-Mode Passive Mixers  
and N-Path Filters in RF Receivers***Masoud Babaie, Delft University of Technology, Delft, The Netherlands*

Modern multimode sub-6GHz receivers heavily employ current-mode passive mixers and N-path filters to simultaneously satisfy the noise requirements and deal with large in-band and out-of-band interferences. After a brief description of a typical receiver structure and its performance matrix, the operation of current-mode receivers and N-path filters will be explained in detail. In particular, this tutorial will focus on the impedance transformation property and reciprocal mixing of those structures. The tutorial will then cover architectures and applications exploiting N-path filters, such as high-order programmable bandpass filters, magnetic-free circulators, mixer-first, and low-noise trans-impedance amplifier (LNTA)-based receivers.

**Masoud Babaie** is a associate professor at the Delft University of Technology, The Netherlands. His research interests include RF/millimeter-wave integrated circuits and systems for wireless communications. He has authored or co-authored one book, three book chapters, 11 patents, and over 80 technical articles. Dr. Babaie serves on the technical program committee of the IEEE ISSCC and is the co-chair for the emerging computing devices and circuits subcommittee of IEEE ESSCIRC. He was a co-recipient of the 2019 IEEE ISSCC demonstration-session certificate of recognition and the 2020 IEEE ISSCC Jan Van Vessel Award for outstanding European paper. He also received the Veni grant from the Netherlands Organization for Scientific Research (NWO) in 2019.

**1:40 PM - Live Q&A in person - February 19****T9: Physical-Layer Security for Latency- and Energy-Constrained  
Integrated Systems***Rabia Tugce Yazicigil, Boston University, Boston, MA*

The boom of connected IoT nodes and ubiquity of wireless communications are projected to increase wireless data traffic by several orders of magnitude in the near future. While these future scalable networks support increasing numbers of wireless devices utilizing the EM spectrum, ensuring the security of wireless communications and sensing is also a critical requirement under tight resource constraints. The physical layer has increasingly become the target of attacks by exploiting hardware weaknesses, e.g., side-channel attacks/fault injection/direct probing, and signal properties, e.g., time, frequency, and modulation characteristics. This tutorial introduces common security vulnerabilities within wireless systems such as jamming, eavesdropping, counterfeiting and spoofing, followed by physical-layer countermeasures, while assessing the trade-offs between performance and security. It examines recent research directions, e.g., secure spatio-temporal modulated arrays, temporal swapping of decomposed constellations, RF fingerprinting, bit-level frequency hopping, and integrated physical-attack-detection (anomaly-detection) sensors, and reaction circuits, and finally discusses research opportunities looking forward.

**Rabia Yazicigil** is an Assistant Professor in the ECE Department at Boston University and a Visiting Scholar at MIT. She was a Postdoctoral Associate at MIT and received her PhD degree from Columbia University in 2016. Her research interests lie at the interface of integrated circuits, signal processing, security, bio-sensing, and wireless communications to innovate system-level solutions for future energy-constrained applications. She has received numerous awards, including the "Electrical Engineering Collaborative Research Award" for her PhD research (2016), second place at the Bell Labs Future X Days Student Research Competition (2015), and 2014 Millman Teaching Assistant Award of Columbia University. She served as the Vice Chair of the Rising Stars 2020 workshop at the ISSCC. She is a member of the ISSCC and ESSCIRC TPCs and 2015 MIT EECS Rising Stars cohort.



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**2:00 PM - Live Q&A in person - February 19****T10: The Art of mm-Wave Design and Layout*****Shahriar Shahramian, Nokia – Bell Labs, New Providence, NJ***

We live in the golden age of mm-wave ASIC design! With the rise of 5G networks & 6G research, a massive push for commercialization of mm-wave integrated circuits is underway. This tutorial explores the hidden impairments that are often overlooked or difficult to locate in mm-wave layouts and interconnects. Using real-life fabricated circuit blocks operating up to and beyond D-band (170GHz), as well as optical circuits operating beyond 100Gb/s, the tutorial will explore layout challenges and impairments that can adversely affect the circuit performance. After modeling these elements, simulations demonstrate the impact of the parasitics on bandwidth, center frequency, stability, and noise figure. Using simple and quick modeling techniques, the designers can incorporate effects of various layout parasitics. Furthermore, mm-wave techniques at the chip level are explored from ground planes to flip-chip bumps. Finally, going beyond the boundaries of integrated circuits, co-design techniques will be explored to carry mm-wave signals into packages, printed circuit boards, and antennas.

**Shahriar Shahramian** received the Ph.D. degree from University of Toronto in 2010 where he focused on the design of mm-wave data converters and transceivers. Dr. Shahramian has been with Bell Laboratories – Nokia since 2009 and is currently the Director of the Communication & Sensing ASICs Research Group. His research focus includes the design of mm-wave wireless and wireline integrated circuits and systems. Dr. Shahramian is a Bell Labs Fellow and leads the design and architecture of several state-of-the-art ASICs for optical coherent and wireless backhaul products. Shahriar serves as the chair of the mm-Wave & THz subcommittee of IEEE BCICTS, as well as chair of mm-Wave SoCs at IEEE RFIC, and is a member of the technical program committee of IEEE ISSCC. He has also served as the Guest Editor of the IEEE Journal of Solid-State Circuits (JSSC). Dr. Shahramian has been the recipient of an Ontario Graduate Scholarship and a University of Toronto Fellowship. He also received the best paper awards at the CSICS Symposium in 2005 and 2015, the RFIC Symposium in 2015 and 2020 and ISSCC in 2018. He was the recipient of the IEEE MTT Young Engineer Award in 2020. He holds an Adjunct Associate Professor position at Columbia University, has received several teaching awards and is the founder and host of The Signal Path educational video series. Dr. Shahramian has presented short courses and workshops at the IEEE CSICS, BCTM, BCICTS, RFIC/IMS and ISSCC conferences.

**2:20 PM - Live Q&A in person - February 19****T11: Digital Equalization and Timing Recovery Techniques for ADC-DSP Based High-Speed Links*****Masum Hossain, University of Alberta, Edmonton, Canada***

As we move beyond 200Gb/s, equalization and timing-recovery techniques have evolved drastically, with ISI and latency playing a significant role in DSP-based receivers, especially with multi-level signaling. This tutorial aims at bridging the gap between well-understood analog/mixed-signal solutions and today's DSP-based solutions. Starting from traditional analog architectures, the tutorial will walk through the evolution toward today's DSP-based equalization and timing recovery. The tutorial will include digital equalization, timing recovery, their interaction, and interdependency. MLSD, a recent trend in DSP-based equalization will also be covered.

**Masum Hossain** received the B.Sc. degree from the Bangladesh University of Engineering and Technology, Dhaka, Bangladesh, in 2002, the M.Sc. degree from Queen's University, Kingston, ON, Canada, in 2005, and the Ph.D. degree from the University of Toronto, Toronto, ON, in 2010. From 2008 to 2010, he was with the Analog and Mixed-Signal Division, Gennum Corporation, Burlington, ON. From 2010 to 2012 he was with Rambus Laboratory, Sunnyvale, CA, USA, as a Senior Member of Technical Staff. In 2013, he joined the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB, Canada. Dr. Hossain was a recipient of the Best Student Paper Award at the 2008 IEEE Custom Integrated Circuits Conference and the Analog Device's Outstanding Student Designer Award in 2010. In 2021 he received EPS society nominated best paper award in IEEE Transaction in Components, Packaging and Manufacturing.

2:40 PM - Live Q&amp;A in person - February 19

**T12: Extending Processor Cores for Machine Learning***Luca Benini, ETH Zürich and UNIBO, Zurich, Switzerland*

Many low-cost, ultra-low-power applications require flexibility and cannot afford the large silicon budget of a specialized machine-learning/artificial-intelligence (ML/AI) accelerator. The tutorial will review the key ideas and approaches to extend the instruction-set architecture (ISA) and microarchitecture, as well as the digital design of processor cores to achieve high efficiency for ML. ISA extension examples (e.g. ARM's Helium and RISC-V extensions) will be analyzed, along with implementation challenges and solutions, drawing insights from various silicon-proven RISC-V cores.

**Luca Benini** holds the Chair of Digital Circuits and Systems at ETH Zürich and is a Full Professor at Università di Bologna. He served as chief architect in STmicroelectronics, France, from 2009-2012. He received a PhD from Stanford University. His research interests are in energy-efficient parallel computing systems, smart sensing micro-systems and machine learning hardware. He is a Fellow of the IEEE, Fellow of the ACM, and a member of the Academia Europaea. He is the recipient of the 2016 IEEE CAS Mac Van Valkenburg award, the 2019 IEEE TCAD Donald O. Pederson Best Paper Award and the ACM/IEEE A. Richard Newton Award 2020.

Transceivers for Exascale: Towards Tbps/mm and sub-pJ/bit

- Organizers:** Tamer Ali, *Mediatek, Irvine, CA*  
Didem Turker Melek, *Cadence Design Systems, San Jose, CA*
- Committee:** Munehiko Nagatani, *NTT, Atsugi, Japan*  
Thomas Toifl, *Cisco Systems, Wallisellen, Switzerland*
- Champions:** Franz Dielacher, *Villach, Austria*  
Bill Redman-White, *HiLight Semiconductor, Southampton, United Kingdom*

Connectivity is a key enabler of exascale computing systems. The forum covers electrical and optical transceivers used throughout these systems, from short die-to-die interconnect to long-distance network interfaces. In addition to state-of-the-art standard and proprietary interfaces, the forum also covers emerging and future works that will significantly increase interface bandwidth and power efficiency, and the design challenges of building high-performance connectivity chips.

Agenda

| <u>Time</u> | <u>Topic</u>   |
|-------------|--|
| 8:00 AM     | Breakfast  |
| 8:15 AM     | <b>Introduction</b><br>Tamer Ali, <i>Mediatek, Irvine, CA</i>  |
| 8:25 AM     | <b>High-Density, Energy-Efficient Interconnect Technologies Inside Supercomputers</b><br>Yuichiro Ajima, <i>Fujitsu, Kawasaki, Japan</i>                 |
| 9:10 AM     | <b>Bandwidth-Density- and Energy-Optimized Die-to-Die Interfaces</b><br>Elad Alon, <i>Blue Cheetah, Sunnyvale, CA</i>                                    |
| 9:55 AM     | Break  |
| 10:10 AM    | <b>Advanced Packaging and 3D-IC Interconnections</b><br>Shenggao Li, <i>TSMC, San Jose, CA</i>   |
| 10:55 AM    | <b>PCIe Rising: The Journey to 64Gb/s and 128Gb/s</b><br>Marc Loinaz, <i>Cadence, San Jose, CA</i>   |
| 11:40 AM    | <b>Circuit Designs for 200+Gb/s Transceivers</b><br>Jihwan Kim, <i>Intel, Hillsboro, OR</i>  |
| 12:25 PM    | Lunch  |
| 1:40 PM     | <b>Electronics and Photonics for Beyond 200G Capable Transceivers</b><br>Peter Ossieur, <i>imec, Ghent, Belgium</i>                                      |
| 2:25 PM     | <b>Direct-drive Optical I/O using Monolithic Silicon Photonics Integration</b><br>Christoph Schulien, <i>Ranovus, Nuremberg, Germany</i>                 |
| 3:10 PM     | Break  |
| 3:25 PM     | <b>Advancements in High-Speed Electrical Terahertz Waveguide Interconnects</b><br>Hyeon-Min Bae, <i>KAIST/Point2-technology, Daejeon, Korea</i>          |
| 4:10 PM     | <b>Realizing Petabit/s IO and sub-pJ/bit System-Wide Communication with Silicon Photonics</b><br>Keren Bergman, <i>Columbia University, New York, NY</i> |
| 4:55 PM     | Closing Remarks  |

The Power Behind Electrical Vehicles –  
Accelerating the Future of Automotive Technology

- Organizer:** Min Chen, *Innoscence America, Santa Clara, CA*
- Committee:** Kousuke Miyaji, *Shinshu University, Nagano, Japan*  
Frank Praemassing, *Infineon Technologies, Villach, Austria*  
Marco Berkhout, *Goodix Technology, Nijmegen, The Netherlands*
- Champion:** Bruce Rae, *STMicroelectronics, Edinburgh, United Kingdom*

Vehicle electrification in EV/HEV is demanding unprecedented power electronic devices, circuits, and systems. This forum provides a comprehensive overview of the mega trend and design challenges on all levels, specifically related to battery protection and management systems, drivetrain topologies & systems, power semiconductor devices and modules, supplemental power electronics, automotive sensors, PMIC, and LED drivers.

Agenda

| <u>Time</u> | <u>Topic</u>   |
|-------------|--|
| 8:00 AM     | Breakfast  |
| 8:15 AM     | <b>Introduction</b><br>Min Chen, <i>Innoscence America, Santa Clara, CA</i>  |
| 8:25 AM     | <b>Mega Trends in Vehicle Electrification and Future EV Technology</b><br>Francesco Gennaro, <i>STMicroelectronics, Catania, Italy</i>                               |
| 9:15 AM     | <b>The Battery System is the Core of Future Mobility</b><br>Patrick Leteinturier, <i>Infineon Technologies, Neubiberg, Germany</i>                                   |
| 10:05 AM    | Break  |
| 10:20 AM    | <b>Trends and Research Cases of 800V Motor Drive Circuits for Battery Electric Vehicle</b><br>Tomonori Kimura, <i>MIRISE Technologies, Nisshin, Japan</i>            |
| 11:10 AM    | <b>The Opportunity from GaN and for GaN in Cars</b><br>Alex Lidow, <i>EPC, El Segundo, CA</i>  |
| 12:00 PM    | Lunch  |
| 1:20 PM     | <b>Power Electronics Components: MCU, Isolated Gate Driver, Isolated Power Supply, and Sensors</b><br>Shunichi Kaeriyama, <i>Renesas Electronics, Kodaira, Japan</i> |
| 2:10 PM     | <b>Long-Range High-Resolution LiDAR Technology</b><br>Katsuyuki Kimura, <i>Toshiba, Kawasaki, Japan</i>  |
| 3:00 PM     | Break  |
| 3:15 PM     | <b>Smart Power ASICs: System Definer and Not Just Components</b><br>Tamer Sinanoglu, <i>Bosch, Reutlingen, Germany</i>   |
| 4:05 PM     | <b>High-Efficiency LED Drivers for Automotive Applications</b><br>Hoi Lee, <i>University of Texas at Dallas, Dallas, Texas</i>                                       |
| 4:55 PM     | Closing Remarks  |

Efficient Wireless Power Amplification and Linearization

- Organizers:** James Buckwalter, *University of California, Santa Barbara, Santa Barbara, CA*  
Jeff Walling, *Virginia Tech, Blacksburg, VA*
- Committee:** Hongtao Xu, *Fudan University, Shanghai, China*  
Byung-Wook Min, *Yonsei University, Seoul, Korea*  
Giuseppe Gramegna, *imec, Leuven, Belgium*  
Wu-Hsin Chen, *Qualcomm, San Diego, CA*
- Champion:** Andreia Cathelin, *STMicroelectronics, Crolles Cedex, France*

This forum reviews the state-of-the-art for power amplification and digital predistortion technologies from RF to mm-wave frequencies with applications to cellular, wifi, and satellite communications. Speakers are chosen to cover advances in CMOS/BiCMOS as well as GaAs/GaN process technologies that comprehensively connect underlying devices, circuits, and system architectures. The forum will also cover the emerging capabilities of digital signal processing for analog and digital PAs in RF bands and mm-wave arrays.

Agenda

| <u>Time</u> | <u>Topic</u>  |
|-------------|---|
| 8:00 AM     | Breakfast   |
| 8:15 AM     | <b>Introduction</b><br>James Buckwalter, <i>University of California, Santa Barbara, Santa Barbara, CA</i>  |
| 8:25 AM     | <b>Emerging Device Technologies for RF/mm-Wave FEM</b><br>Nicholas Comfoltey, <i>GlobalFoundries, San Diego, CA</i>                                   |
| 9:15 AM     | <b>Linear GaAs Technologies for Mobile Power Amplifiers</b><br>David Danzilio, <i>WIN Semiconductors, Taoyuan, Taiwan</i>                             |
| 10:05 AM    | Break   |
| 10:20 AM    | <b>Sub-8GHz Base Station Power Amplifiers and Linearization</b><br>Rui Hou, <i>Ericsson, Stockholm, Sweden</i>  |
| 11:10 AM    | <b>Advances in Highly Efficient All-Digital CMOS Transmitters for Wide Bandwidth Wireless Application</b><br>Ofir Degani, <i>Intel, Haifa, Israel</i> |
| 12:15 PM    | Lunch   |
| 1:20 PM     | <b>Single Transformer-Based Compact Doherty PA for 5G RFICs and Base-Stations</b><br>Hyun-Chul Park, <i>Samsung, Hwaseong, Korea</i>                  |
| 2:10 PM     | <b>Digital Predistortion (DPD) for High-Efficiency 5G Radio Units</b><br>Zohaib Mahmood, <i>Maxlinear, Waltham, MA</i>                                |
| 3:00 PM     | Break   |
| 3:15 PM     | <b>Digital Pre-Distortion for Large-Scale mm-Wave Arrays</b><br>Harish Krishnaswamy, <i>Sivers Semiconductors, Chatham, NJ</i>                        |
| 4:05 PM     | <b>Machine-Learning-Assisted Approaches for Wideband DPD</b><br>Anding Zhu, <i>University College Dublin, Dublin, Ireland</i>                         |
| 4:55 PM     | Closing Remarks   |

Mentoring Session/Networking Bingo Event  
(Open to all Attendees)  
3:00 - 5:00 PM

Women in Circuits (WiC) together with ISSCC will be holding a networking and mentoring session on Sunday afternoon. Distinguished panelists from the “Integrated Circuits in an Interconnected World” panel, WiC members, and other participants will play getting-to-know-you bingo to promote engagement between various members of the community. This will give participants the chance to network and mingle with people across a spectrum of seniority in the field in a casual setting. This event is open to all ISSCC attendees and the public.

EE1: Student Research Preview (SRP)  
8:00 PM

The Student Research Preview (SRP) will highlight selected student research projects in progress. The SRP consists a number of ninety-second presentations followed by a Poster Session, by graduate students from around the world, which have been selected on the basis of a short submission concerning their on-going research. Selection is based on the technical quality and innovation of the work. This year, the SRP will be presented in three theme sections: 1) RF and Analog, 2) Energy-Efficient Circuits and Systems, and 3) Compute-in-Memory (CIM), Artificial Intelligence (AI) and Security.

The SRP will include an inspirational lecture by Professor Mark Horowitz (Stanford University). SRP begins at 8:00 pm on Sunday, February 19th. It is open to all ISSCC registrants.

SRP ORGANIZING COMMITTEE

- Co-Chair: Jerald Yoo, *National University of Singapore, Singapore*
- Co-Chair: Mondira (Mandy) Pant, *Intel, MA*
- Advisor: Anantha Chandrakasan, *MIT, MA*
- Advisor: Jan Van der Spiegel, *University of Pennsylvania, Philadelphia, PA*
- Media/Publications: Laura Fujino, *University of Toronto, Toronto, Canada*
- A/V: Trudy Stetzler, *Halliburton, Houston, TX*

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- Jaydeep Kulkarni, *University of Texas at Austin, TX*
- Jiamin Li, *Southern University of Science and Technology, China*
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- Mondira Pant, *Intel, MA*
- Negar Reiskarimian, *Massachusetts Institute of Technology, MA*
- Atsushi Shirane, *Tokyo Institute of Technology, Japan*
- Mahsa Shoaran, *EPFL, Switzerland*
- Yildiz Sinangil, *Apple, CA*
- Mahmut Sinangil, *Nvidia, CA*
- Filip Tavernier, *KU Leuven, Belgium*
- Chia-Hsiang Yang, *National Taiwan University, Taiwan*
- Lita Yang, *Meta, CA*
- Rabia Tugce Yazicigil, *Boston University, MA*
- Jerald Yoo, *National University of Singapore, Singapore*
- Milin Zhang, *Tsinghua University, China*

Plenary Session — Invited Papers

**Chair:** *Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands*  
*ISSCC Conference Chair*

**Associate Chair:** *Piet Wambacq, imec, Heverlee, Belgium*  
*ISSCC International Technical Program Chair*

**FORMAL OPENING OF THE CONFERENCE** **8:30 AM**

**1.1 Innovation For the Next Decade of Compute Efficiency** **8:45 AM**

*Lisa Su, Chair and Chief Executive Officer, AMD, Austin, TX*

Although traditional scaling has slowed over the past decade, we have made tremendous progress as an industry with new approaches including chiplet-based architectures, domain-specific accelerators, and advanced packaging technologies which have enabled major milestones including the first exascale supercomputers. As we look into the future, we need to accelerate the pace of innovation to drive the next decade of advancement in high-performance computing. By far, the largest limiting factor to delivering continued compounded growth in computation power is energy efficiency. In this paper, we highlight a holistic strategy for accelerating innovation in energy efficiency required for next-generation high-performance computing and ultimately achieving zettascale performance. These approaches will be built on continued innovation in process technologies, modular chiplet architectures, and advanced packaging. Fully meeting the challenge will require new dimensions of improvement through extending domain-specific architectures to accelerate core algorithms in combination with wide-scale deployment of AI across all aspects of the system from transistors to software.

**1.2 Shape the World with Mixed-Signal Integrated Circuits - Past, Present, and Future** **9:20 AM**

*Akira Matsuzawa, Professor Emeritus of Tokyo Institute of Technology and CEO of Tech Idea, Kawasaki, Japan*

The past 50 years has been an era in which analog equipment has been replaced by digital counterparts. Audio, TV, video, camcorder, camera, recording, wired connection, and wireless communication have been subject to digitization. The digitization of these devices and systems was due to the technological shift from bipolar to CMOS, and to the development of logic and memory circuits supported by scaling laws. In addition, design innovation in mixed-signal integrated circuits such as ADCs and DACs has shown to be indispensable. This talk will look back on the digitization of equipment and the mixed-signal integrated circuit technology that contributed to it. Further, we will look forward to future applications and developments.

**ISSCC, SSCS, IEEE AWARD PRESENTATIONS** **9:55 AM**

**BREAK** **10:20 AM**

1.3

**EU Chips Act Drives Pan-European Full-Stack Innovation Partnerships**

10:40 AM

*Jo De Boeck, Executive Vice President and Chief Strategy Officer,  
imec & KU Leuven, Leuven, Belgium*

In every aspect of our life and society, semiconductors play a major role. The pandemic in conjunction with supply chain hiccups and geopolitical tensions made all regions realize that they need to revisit their presence in the semiconductor value chain. The European Commission projected the ambition of achieving a 20% share of the global semiconductor production by 2030.

Europe can leverage existing strengths such as, among others, the unique position of equipment companies and leadership positions in 300mm semiconductor technology R&D. The Chips-for-Europe initiative will invest in pilot lines and ecosystems for chip manufacturing, embracing leading-edge and first-of-a-kind technologies. The pilot lines will allow early exploration of the potential impact of new technology features in advanced chip and system architectures. This will trigger increased demand and accelerate industrial uptake of the novel technologies. This type of innovation loop is also essential for deep-tech start-ups building their unique value proposition. The full-stack, networked model of industry collaboration is at the core of the EU Chips Act ambition and will impact different application domains such as heterogeneous cloud and distributed computing, connectivity, automotive, and health.

It is crucial for all this innovation potential that we, as an industry, consider that semiconductor manufacturing is resource-intensive with respect to energy, water, chemicals, and raw materials. Design-technology co-optimization (DTCO) and System-Technology co-optimization (STCO) methodologies can develop a framework for early sustainability assessments of logic technologies. Finally, we urgently need to get the message across that climate, health, safety, and human connectedness all require complex digital backbones, if we want to stand a chance of attracting the right talent.

1.4

**5G Drives Exponential Increase in Processing Needs Across all Industries**

11:15 AM

*Erik Ekudden, Senior Vice President & Chief Technology Officer, Ericsson,  
Kista, Sweden*

Across essentially all industrial sectors, advanced semiconductor technology is the key enabler for innovations in customer offerings and internal efficiencies. The increase in the value of data and the related push for AI are examples of forces that increase the demand for compute power, which translates to more complex and powerful silicon. Moore's Law, supported by rapidly evolving semiconductor technology and ever more advanced building practices and assembly technologies, has met the need for decades.

But what is driving 5G today? If we look at the processing requirements, it is the digital front-end, physical layer processing, and beam forming. Back in 2010, LTE/4G was a 20MHz carrier with two receive and two transmit branches, and there was a transmission time interval of one millisecond. Fast forward to where we are today on 5G with massive MIMO, we typically have 100MHz carrier bandwidth. That is a factor of five increase. We have 64 transmitter and 64 receiver radios, which is an increase by a factor of 32, and the transmission time is down to 0.5 milliseconds. In other words, there is only half the time to do 160 times more processing. This is driving an exponential increase in processing needs across the telecom business today, and will continue to do so as we race towards 6G. This talk will address whether the semiconductor industry is ready to tackle these challenges.

PRESENTATION TO PLENARY SPEAKERS

11:50 AM

CONCLUSION

11:55 AM



Digital Processors

Session Chair: *Shidhartha Das*, AMD, Cambridge, United Kingdom

Session Co-Chair: *Ji-Hoon Kim*, Ewha Womans University, Seoul, Korea

1:30 PM

2.1 “Zen 4”: The AMD 5nm 5.7GHz x86-64 Microprocessor Core

DS1

*B. Munger<sup>1</sup>, K. Wilcox<sup>1</sup>, J. Sniderman<sup>1</sup>, C. Tung<sup>1</sup>, B. Johnson<sup>2</sup>, R. Schreiber<sup>3</sup>, C. Henrion<sup>2</sup>, K. Gillespie<sup>1</sup>, T. Burd<sup>4</sup>, H. Fair<sup>1</sup>, D. Johnson<sup>2</sup>, J. White<sup>1</sup>, S. McLelland<sup>1</sup>, S. Bakke<sup>1</sup>, J. Olson<sup>1</sup>, R. McCracken<sup>1</sup>, M. Pickett<sup>2</sup>, A. Horiuchi<sup>2</sup>, H. Nguyen<sup>1</sup>, T. H. Jackson<sup>2</sup>*

<sup>1</sup>AMD, Boxborough, MA; <sup>2</sup>AMD, Fort Collins, CO; <sup>3</sup>AMD, Austin, TX; <sup>4</sup>AMD, Santa Clara, CA

2:00 PM

2.2 A 5G Mobile Gaming-Centric SoC with High-Performance Thermal Management in 4nm FinFET

*B-J. Huang, A. Tsai, L. Hsieh, K. Chang, C-J. Tsai, J-M. Chen, E-W. Fang, S-Y. Hsueh, J. Ciao, B. Chen, C. Chang, P. Kao, E. Wang, H. H. Chen, H. Mair, S-A. Hwang*

MediaTek, Hsinchu, Taiwan

2:30 PM

2.3 Amorphica: 4-Replica 512 Fully Connected Spin 336MHz Metamorphic Annealer with Programmable Optimization Strategy and Compressed-Spin-Transfer Multi-Chip Extension

DS1

*K. Kawamura<sup>\*1</sup>, J. Yu<sup>\*1</sup>, D. Okonogi<sup>1</sup>, S. Jimbo<sup>1</sup>, G. Inoue<sup>1</sup>, A. Hyodo<sup>1</sup>, Á. L. García-Arias<sup>1</sup>, K. Ando<sup>2</sup>, B. H. Fukushima-Kimura<sup>2</sup>, R. Yasudo<sup>3</sup>, T. V. Chu<sup>1</sup>, M. Motomura<sup>1</sup>*

<sup>1</sup>Tokyo Institute of Technology, Yokohama, Japan

<sup>2</sup>Hokkaido University, Sapporo, Japan

<sup>3</sup>Kyoto University, Kyoto, Japan

\*Equally Credited Authors (ECAs)

Break 3:00 PM

3:15 PM

2.4 A Fully Integrated End-to-End Genome Analysis Accelerator for Next-Generation Sequencing

*Y-L. Chen<sup>\*1</sup>, C-H. Yang<sup>\*1</sup>, Y-C. Wu<sup>\*1</sup>, C-H. Lee<sup>2</sup>, W-C. Chen<sup>3</sup>, L-Y. Lin<sup>3</sup>, N-S. Chang<sup>3</sup>, C-P. Lin<sup>3</sup>, C-S. Chen<sup>3</sup>, J-H. Hung<sup>2,4</sup>, C-H. Yang<sup>1,2</sup>*

<sup>1</sup>National Taiwan University, Taipei, Taiwan; <sup>2</sup>GeneASIC Technologies, Hsinchu, Taiwan

<sup>3</sup>Taiwan Semiconductor Research Institute, Hsinchu, Taiwan

<sup>4</sup>National Yang Ming Chiao Tung University, Hsinchu, Taiwan

\*Equally Credited Authors (ECAs)

3:45 PM

2.5 A 28nm 142mW Motion-Control SoC for Autonomous Mobile Robots

*I-T. Lin<sup>1</sup>, Z-S. Fu<sup>1</sup>, W-C. Chen<sup>2</sup>, L-Y. Lin<sup>2</sup>, N-S. Chang<sup>2</sup>, C-P. Lin<sup>2</sup>, C-S. Chen<sup>2</sup>, C-H. Yang<sup>1</sup>*

<sup>1</sup>National Taiwan University, Taipei, Taiwan

<sup>2</sup>Taiwan Semiconductor Research Institute, Hsinchu, Taiwan

4:15 PM

2.6 VISTA: A 704mW 4K-UHD CNN Processor for Video and Image Spatial/Temporal Interpolation Acceleration

*K-P. Lin, J-H. Liu, J-Y. Wu, H-C. Liao, C-T. Huang*

National Tsing Hua University, Hsinchu, Taiwan

4:45 PM

2.7 MetaVRain: A 133mW Real-Time Hyper-Realistic 3D-NeRF Processor with 1D-2D Hybrid-Neural Engines for Metaverse on Mobile Devices

DS1

*D. Han, J. Ryu, S. Kim, S. Kim, H-J. Yoo*

Korea Advanced Institute of Science and Technology, Daejeon, Korea

Conclusion 5:15 PM

Amplifiers and Oscillators

Session Chair: **Jens Anders**, University of Stuttgart, Stuttgart, Germany

Session Co-Chair: **Shon-Hang Wen**, MediaTek, Hsinchu, Taiwan

1:30 PM

3.1 **A 120.9dB DR, -111.2dB THD+N Digital-Input Capacitively-Coupled Chopper Class-D Audio Amplifier**

*H. Zhang<sup>1</sup>, M. Berkhout<sup>2</sup>, K. A. A. Makinwa<sup>1</sup>, Q. Fan<sup>1</sup>*

<sup>1</sup>Delft University of Technology, Delft, The Netherlands

<sup>2</sup>Goodix Technology, Nijmegen, The Netherlands

2:00 PM

3.2 **A Chopper-Stabilized Amplifier with a Relaxed Fill-In Technique and 22.6pA Input Current**

*T. Rooijers<sup>1,2</sup>, J. H. Huijsing<sup>1</sup>, K. A. A. Makinwa<sup>1</sup>*

<sup>1</sup>Delft University of Technology, Delft, The Netherlands; <sup>2</sup>now at Broadcom, Bunnik, The Netherlands

2:15 PM

3.3 **Bandpass Filter and Oscillator ICs with THD < -140dBc at 10V<sub>ppd</sub> for Testing High-Resolution ADCs**

*S. Sarkar<sup>1,2</sup>, R. Agarwal<sup>1</sup>, N. Krishnapura<sup>2</sup>*

<sup>1</sup>Texas Instruments, Bangalore, India; <sup>2</sup>Indian Institute of Technology Madras, Chennai, India

2:30 PM

3.4 **A 0.01mm<sup>2</sup> 10MHz RC Frequency Reference with a 1-Point On-Chip-Trimmed Inaccuracy of ±0.28% from -45°C to 125°C in 0.18µm CMOS**

*X. An<sup>\*1,2</sup>, S. Pan<sup>\*1,3</sup>, H. Jiang<sup>2</sup>, K. A. A. Makinwa<sup>1</sup>*

<sup>1</sup>Delft University of Technology, Delft, The Netherlands

<sup>2</sup>Silicon Integrated, Eindhoven, The Netherlands; <sup>3</sup>Tsinghua University, Beijing, China

\*Equally Credited Authors (ECAs)

Break 3:00 PM

3:15 PM

3.5 **A 1.4µW/MHz 100MHz RC Oscillator with ±1030ppm Inaccuracy from -40°C to 85°C After Accelerated Aging for 500 Hours at 125°C**

*K-S. Park, N. Pal, Y. Li, R. Xia, T. Wang, A. Abdelrahman, P. K. Hanumolu*

University of Illinois, Urbana, IL

3:45 PM

**DS1** 3.6 **A 12/13.56MHz Crystal Oscillator with Binary-Search-Assisted Two-Step Injection Achieving 5.0nJ Startup Energy and 45.8µs Startup Time**

*H. Li<sup>1</sup>, K-M. Lei<sup>1</sup>, P-I. Mak<sup>1</sup>, R. P. Martins<sup>1,2</sup>*

<sup>1</sup>University of Macau, Macau, China; <sup>2</sup>Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

4:15 PM

**DS1** 3.7 **A 16MHz XO with 17.5µs Startup Time Under 10<sup>4</sup>ppm-ΔF Injection Using Automatic Phase-Error Correction Technique**

*Z. Cai<sup>1</sup>, X. Wang<sup>1</sup>, Z. Wang<sup>1</sup>, Y. Yin<sup>1</sup>, W. Zhang<sup>1</sup>, T. Xu<sup>2</sup>, Y. Guo<sup>1</sup>*

<sup>1</sup>Nanjing University of Posts and Telecommunications, Nanjing, China; <sup>2</sup>Hefei University, Hefei, China

4:30 PM

3.8 **A 0.954nW 32kHz Crystal Oscillator in 22nm CMOS with Gm-C-Based Current Injection Control**

*Y. Zhang<sup>1</sup>, Y. You<sup>1</sup>, W. Ren<sup>1</sup>, X. Xu<sup>1</sup>, L. Shen<sup>1</sup>, J. Ru<sup>1</sup>, R. Huang<sup>1</sup>, L. Ye<sup>1,2</sup>*

<sup>1</sup>Peking University, Beijing, China

<sup>2</sup>Advanced Institute of Information Technology of Peking University, Hangzhou, China

4:45 PM

3.9 **A 0.5-to-400MHz Programmable BAW Oscillator with Fractional Output Divider Achieving 4ppm Frequency Stability over Temperature and <95fs Jitter**

*S. Mukherjee<sup>1</sup>, Y. Darwhekar<sup>1</sup>, J. Janardhanan<sup>1</sup>, P. Mirajkar<sup>1</sup>, R. Reddy<sup>1</sup>, H. Ramesh<sup>1</sup>, B. Bahr<sup>2</sup>, J. Chand<sup>1</sup>, U. Meda<sup>1</sup>, B. Haroun<sup>2</sup>, S. Karantha<sup>1</sup>, E. Yen<sup>3</sup>, K. Martin<sup>2</sup>, D. Gan<sup>4</sup>, A. Sijelmass<sup>2</sup>, S. Aniruddhan<sup>5</sup>, <sup>1</sup>Texas Instruments, Bangalore, India; <sup>2</sup>Texas Instruments, Dallas, TX*

<sup>3</sup>Texas Instruments, Santa Clara, CA; <sup>4</sup>Texas Instruments, Melaka, Malaysia

<sup>5</sup>Indian Institute of Technology Madras, Chennai, India

Conclusion 5:15 PM

Frequency Synthesizers

Session Chair: *Dmytro Cherniak, Infineon Technologies, Villach, Austria*  
Session Co-Chair: *Wanghua Wu, Samsung Semiconductor, Santa Clara, CA*

1:30 PM

**4.1 DS1 A 16GHz, 41kHz<sub>rms</sub> Frequency Error, Background-Calibrated, Duty-Cycled FMCW Charge-Pump PLL**

*P. T. Renukaswamy<sup>1,2</sup>, K. Vaesen<sup>1</sup>, N. Markulic<sup>1</sup>, V. Derudder<sup>1</sup>, D-W. Park<sup>1</sup>, P. Wambacq<sup>1,2</sup>, J. Craninckx<sup>1</sup>*

<sup>1</sup>imec, Heverlee, Belgium

<sup>2</sup>Vrije Universiteit Brussel, Brussels, Belgium

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**4.2 A 135fs<sub>rms</sub>-Jitter 0.6-to-7.7GHz LO Generator Using a Single LC-VCO-Based Subsampling PLL and a Ring-Oscillator-Based Sub-Integer-N Frequency Multiplier**

*Y. Jo\*, J. Kim\*, Y. Shin, C. Hwang, H. Park, J. Choi*

Korea Advanced Institute of Science and Technology, Daejeon, Korea

\*Equally Credited Authors (ECAs)

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**4.3 A 76.7fs-Integrated-Jitter and -71.9dBc In-Band Fractional-Spur Bang-Bang Digital PLL Based on an Inverse-Constant-Slope DTC and FCW Subtractive Dithering**

*S. M. Dartizio<sup>1</sup>, F. Tesolin<sup>1</sup>, G. Castoro<sup>1</sup>, F. Buccoleri<sup>1</sup>, L. Lanzoni<sup>1</sup>, M. Rossoni<sup>1</sup>, D. Cherniak<sup>2</sup>, L. Bertulessi<sup>1</sup>, C. Samori<sup>1</sup>, A. L. Lacaita<sup>1</sup>, S. Levantino<sup>1</sup>*

<sup>1</sup>Politecnico di Milano, Milano, Italy

<sup>2</sup>Infineon Technologies, Villach, Austria

Break 3:00 PM

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**4.4 A 32kHz-Reference 2.4GHz Fractional-N Nonuniform Oversampling PLL with Gain-Boosted PD and Loop-Gain Calibration**

*J. Qiu, W. Wang, Z. Sun, B. Liu, Y. Zhang, D. Xu, H. Huang, A. A. Fadila, Z. Liu, W. Madany, Y. Xiong, A. Shirane, K. Okada*

Tokyo Institute of Technology, Tokyo, Japan

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**4.5 A 9.25GHz Digital PLL with Fractional-Spur Cancellation Based on a Multi-DTC Topology**

*G. Castoro\*, S. M. Dartizio\*, F. Tesolin<sup>1</sup>, F. Buccoleri<sup>1</sup>, M. Rossoni<sup>1</sup>, D. Cherniak<sup>2</sup>, L. Bertulessi<sup>1</sup>, C. Samori<sup>1</sup>, A. L. Lacaita<sup>1</sup>, S. Levantino<sup>1</sup>*

<sup>1</sup>Politecnico di Milano, Milan, Italy

<sup>2</sup>Infineon Technologies, Villach, Austria

\*Equally Credited Authors (ECAs)

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**4.6 A 47fs<sub>rms</sub>-Jitter and 26.6mW 103.5GHz PLL with Power-Gating Injection-Locked Frequency-Multiplier-Based Phase Detector and Extended Loop Bandwidth**

*J. Bang, J. Kim, S. Jung, S. Park, J. Choi*

Korea Advanced Institute of Science and Technology, Daejeon, Korea

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**4.7 A 0.4V-V<sub>DD</sub> 2.25-to-2.75GHz ULV-SS-PLL Achieving 236.6fs<sub>rms</sub> Jitter, -253.8dB Jitter-Power FoM, and -76.1dBc Reference Spur**

*Z. Zhang<sup>1</sup>, X. Shen<sup>1</sup>, Z. Zhang<sup>1</sup>, G. Li<sup>1</sup>, N. Qi<sup>1</sup>, J. Liu<sup>1</sup>, Y. Chen<sup>2</sup>, N. Wu<sup>1</sup>, L. Liu<sup>1</sup>*

<sup>1</sup>Chinese Academy of Sciences, Beijing, China

<sup>2</sup>University of Macau, Macau, China

Conclusion 5:15 PM

Image Sensors

Session Chair: *Kazuko Nishimura*, Panasonic Holdings, Moriguchi, Japan  
Session Co-Chair: *Masaki Sakakibara*, Sony Semiconductor Solutions, Atsugi-shi, Japan

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**5.1 DS1 A 3-Wafer-Stacked Hybrid 15MPixel CIS + 1MPixel EVS with 4.6GEvent/s Readout, In-Pixel TDC and On-Chip ISP and ESP Function**  
*M. Guo<sup>1</sup>, S. Chen<sup>1</sup>, Z. Gao<sup>2</sup>, W. Yang<sup>1</sup>, P. Bartkovjak<sup>2</sup>, Q. Qin<sup>2</sup>, X. Hu<sup>1</sup>, D. Zhou<sup>1</sup>, M. Uchiyama<sup>2</sup>, Y. Kudo<sup>3</sup>, S. Fukuoka<sup>3</sup>, C. Xu<sup>2</sup>, H. Ebihara<sup>2</sup>, A. Wang<sup>2</sup>, P. Jiang<sup>2</sup>, B. Jiang<sup>2</sup>, B. Mu<sup>2</sup>, H. Chen<sup>1</sup>, J. Yang<sup>2</sup>, T. Da<sup>2</sup>, A. Suess<sup>2</sup>*  
<sup>1</sup>OmniVision Technologies, Shanghai, China; <sup>2</sup>OmniVision Technologies, Santa Clara, CA  
<sup>3</sup>OmniVision Technologies, Yokohama, Japan

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**5.2 DS1 1.22µm 35.6Mpixel RGB Hybrid Event-Based Vision Sensor with 4.88µm-Pitch Event Pixels and up to 10K Event Frame Rate by Adaptive Control on Event Sparsity**  
*K. Kodama<sup>1</sup>, Y. Sato<sup>1</sup>, Y. Yorikado<sup>1</sup>, R. Berner<sup>2</sup>, K. Mizoguchi<sup>1</sup>, T. Miyazaki<sup>1</sup>, M. Tsukamoto<sup>1</sup>, Y. Matoba<sup>1</sup>, H. Shinozaki<sup>1</sup>, A. Niwa<sup>1</sup>, T. Yamaguchi<sup>1</sup>, C. Brandl<sup>2</sup>, H. Wakabayashi<sup>1</sup>, Y. Oike<sup>1</sup>*  
<sup>1</sup>Sony Semiconductor Solutions, Atsugi, Japan  
<sup>2</sup>Sony Advanced Visual Sensing, Schlieren, Switzerland

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**5.3 DS1 A 2.97µm-Pitch Event-Based Vision Sensor with Shared Pixel Front-End Circuitry and Low-Noise Intensity Readout Mode**  
*A. Niwa<sup>1</sup>, F. Mochizuki<sup>1</sup>, R. Berner<sup>2</sup>, T. Maruyama<sup>1</sup>, T. Terano<sup>1</sup>, K. Takamiya<sup>1</sup>, Y. Kimura<sup>1</sup>, K. Mizoguchi<sup>1</sup>, T. Miyazaki<sup>1</sup>, S. Kaizu<sup>1</sup>, H. Takahashi<sup>1</sup>, A. Suzuki<sup>1</sup>, C. Brandl<sup>2</sup>, H. Wakabayashi<sup>1</sup>, Y. Oike<sup>1</sup>*  
<sup>1</sup>Sony Semiconductor Solutions, Kanagawa, Japan  
<sup>2</sup>Sony Advanced Visual Sensing, Zurich, Switzerland

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**5.4 A 0.64µm 4-Photodiode 1.28µm 50MPixel CMOS Image Sensor with 0.98e- Temporal Noise and 20Ke- Full-Well Capacity Employing Quarter-Ring Source-Follower**  
*H. Kim, Y. H. Kim, S. Moon, H. Kim, B. Yoo, J. Park, S. Kim, J-M. Koo, S. Seo, H. J. Shin, Y. Choi, J. Kim, K. Kim, J-H. Seo, S. Lim, T. Jung, H. Park, S. Jung, J. Ko, K. Lee, J. Ahn, J. Yim*  
Samsung Electronics, Hwasung, Korea

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**5.5 A 16.4kPixel 3.08-to-3.86THz Digital Real-Time CMOS Image Sensor with 73dB Dynamic Range**  
*M. Liu<sup>1</sup>, Z. Cai<sup>1</sup>, S. Zhou<sup>2</sup>, M-K. Law<sup>3</sup>, J. Liu<sup>1</sup>, J. Ma<sup>4</sup>, N. Wu<sup>1</sup>, L. Liu<sup>1</sup>*  
<sup>1</sup>Chinese Academy of Sciences, Beijing, China; <sup>2</sup>Tianjin University, Tianjin, China  
<sup>3</sup>University of Macau, Macau, China; <sup>4</sup>Zhejiang University, Hangzhou, China

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**5.6 DS1 A 400×200 600fps 117.7dB-DR SPAD X-Ray Detector with Seamless Global Shutter and Time-Encoded Extrapolation Counter**  
*B. Park<sup>1</sup>, B. Ahn<sup>1</sup>, H-S. Cho<sup>2</sup>, J. Jeong<sup>3</sup>, K. Hwang<sup>3</sup>, T. Kim<sup>3</sup>, M-J. Lee<sup>2</sup>, Y. Chae<sup>1</sup>*  
<sup>1</sup>Yonsei University, Seoul, Korea; <sup>2</sup>Korea Institute of Science and Technology, Seoul, Korea  
<sup>3</sup>Rayence, Hwaseong, Korea

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**5.7 55pW/pixel Peak Power Imager with Near-Sensor Novelty/Edge Detection and DC-DC Converter-Less MPPT for Purely Harvested Sensor Nodes**  
*K. A. Ahmed\*, H. Okuhara\*, M. Alioto*, National University of Singapore, Singapore, Singapore  
\*Equally Credited Authors (ECAs)

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**5.8 DS1 Dual-Port CMOS Image Sensor with Regression-Based HDR Flux-to-Digital Conversion and 80ns Rapid-Update Pixel-Wise Exposure Coding**  
*R. Gulve, R. Rangel, A. Barman, D. Nguyen, M. Wei, M. A. Sakr, X. Sun, D. B. Lindell, K. N. Kutulakos, R. Genov*, University of Toronto, Toronto, Canada

Conclusion 5:15 PM

Advanced Wireline Links and Techniques

Session Chair: *Friedel Gerfers*, Technische Universität Berlin, Berlin, Germany

Session Co-Chair: *Takashi Takemoto*, Hitachi, Sapporo, Japan

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6.1 A 112Gb/s Serial Link Transceiver With 3-tap FFE and 18-tap DFE Receiver for up to 43dB Insertion Loss Channel in 7nm FinFET Technology

*B. Zhang<sup>1</sup>, A. Vasani<sup>1</sup>, A. Sinha<sup>2</sup>, A. Nilchi<sup>1</sup>, H. Tong<sup>1</sup>, L. Rao<sup>1</sup>, K. Khanoyan<sup>1</sup>, H. Hatamkhani<sup>1</sup>, X. Yang<sup>1</sup>, X. Meng<sup>1</sup>, A. Wong<sup>2</sup>, J. Kim<sup>2</sup>, P. Jing<sup>2</sup>, Y. Sun<sup>2</sup>, A. Nazemi<sup>1</sup>, D. Liu<sup>2</sup>, A. Brewster<sup>1</sup>, J. Cao<sup>1</sup>, A. Mamtaz<sup>1</sup>*

<sup>1</sup>Broadcom, Irvine, CA

<sup>2</sup>Broadcom, San Jose, CA

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6.2 A 4.63pJ/b 112Gb/s DSP-Based PAM-4 Transceiver for a Large-Scale Switch in 5nm FinFET

DS2

*H. Park<sup>\*1</sup>, M. Abdullatif<sup>\*1</sup>, E. Chen<sup>1</sup>, A. Elmallah<sup>1</sup>, Q. Nehal<sup>1</sup>, M. Gandara<sup>1</sup>, T-B. Liu<sup>2</sup>, A. Khashaba<sup>1</sup>, J. Lee<sup>1</sup>, C-Y. Kuan<sup>2</sup>, D. Ramachandran<sup>1</sup>, R-B. Sun<sup>2</sup>, A. Atharav<sup>1</sup>, Y. Chun<sup>1</sup>, M. Zhang<sup>1</sup>, D-F. Weng<sup>2</sup>, C-H. Tsa<sup>2</sup>, C-H. Chang<sup>2</sup>, C-S. Peng<sup>2</sup>, S-T. Hsu<sup>2</sup>, T. Ali<sup>1</sup>*

<sup>1</sup>MediaTek, Irvine, CA

<sup>2</sup>MediaTek, Hsinchu, Taiwan

\*Equally Credited Authors (ECAs)

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6.3 A 0.43pJ/b 200Gb/s 5-Tap Delay-Line-Based Receiver FFE with Low-Frequency Equalization in 28nm CMOS

*B. Ye, G. Wu, W. Gai, K. Sheng, Y. He*, Peking University, Beijing, China

Break 3:00 PM

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6.4 A 4nm 32Gb/s 8Tb/s/mm Die-to-Die Chiplet Using NRZ Single-Ended Transceiver With Equalization Schemes And Training Techniques

*K. Seong, D. Park, G. Bae, H. Lee, Y. Suh, W. Oh, H. Lee, J. Kim, T. Lee, G. Mo, S. Jung, D. Choi, B-J. Yoo, S. Park, H-G. Rhew, J. Shin*

Samsung Electronics, Hwasung, Korea

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6.5 A 37.8dB Channel Loss 0.6µs Lock Time CDR with Flash Frequency Acquisition in 5nm FinFET

*C-K. Kao, S-C. Hung, T-H. Yeh, C-Y. Hsiao*, MediaTek, Hsinchu, Taiwan

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6.6 A 0.83pJ/b 52Gb/s PAM-4 Baud-Rate CDR with Pattern-Based Phase Detector for Short-Reach Applications

*S. Park, Y. Choi, J. Sim, J. Choi, H. Park, Y. Kwon, C. Kim*, Korea University, Seoul, Korea

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6.7 A 128Gb/s PAM-4 Transmitter with Programmable-Width Pulse Generator and Pattern-Dependent Pre-Emphasis in 28nm CMOS

*K. Sheng, W. Gai, Z. Feng, H. Niu, B. Ye, H. Zhou*, Peking University, Beijing, China

5:00 PM

6.8 A 100Gb/s 1.6V<sub>ppd</sub> PAM-8 Transmitter with High-Swing 3+1 Hybrid FFE Taps in 40nm

*J. Yang<sup>\*</sup>, E. Song<sup>\*</sup>, S. Hong, D. Lee, S. Lee, H. Im, T. Shin, J. Han*

Hanyang University, Seoul, Korea

\*Equally Credited Authors (ECAs)

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# Demonstration Session 1, Monday February 20<sup>th</sup>, 5:00-7:00 PM

This year, the Demonstration Session extending in selected regular papers, both Academic and Industrial, will take place on Monday February 20<sup>th</sup>, and Tuesday February 21<sup>st</sup>, from 5 pm until 7 pm in the Golden Gate Hall. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2023, as noted by the symbol **DS1**

## ISSCC 2022 Demo Award Winners Presenting at ISSCC 2023

- 6.1 A 1.41pJ/b 224Gb/s PAM-4 SerDes Receiver with 31dB Loss Compensation
- 32.1 BatDrone: A 9.83M-focal-points/s 7.76 $\mu$ s-Latency Ultrasound Imaging System with On-Chip Per-Voxel RX Beamfocusing for 7m-Range Drone Applications

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- 2.1 “Zen 4”: The AMD 5nm 5.7GHz x86-64 Microprocessor Core
- 2.3 Amorphica: 4-Replica 512 Fully Connected Spin 336MHz Metamorphic Annealer with Programmable Optimization Strategy and Compressed-Spin-Transfer Multi-Chip Extension
- 2.7 MetaVRain: A 133mW Real-Time Hyper-Realistic 3D-NeRF Processor with 1D-2D Hybrid-Neural Engines for Metaverse on Mobile Devices
- 3.6 A 12/13.56MHz Crystal Oscillator with Binary-Search-Assisted Two-Step Injection Achieving 5.0nJ Startup Energy and 45.8 $\mu$ s Startup Time
- 3.7 A 16MHz XO with 17.5 $\mu$ s Startup Time Under 10<sup>4</sup>ppm- $\Delta$ F Injection Using Automatic Phase-Error Correction Technique
- 4.1 A 16GHz, 41kHz<sub>rms</sub> Frequency Error, Background-Calibrated, Duty-Cycled FMCW Charge-Pump PLL
- 5.1 A 3-Wafer-Stacked Hybrid 15MPixel CIS + 1MPixel EVS with 4.6GEvent/s Readout, In-Pixel TDC and On-Chip ISP and ESP Function
- 5.2 1.22 $\mu$ m 35.6Mpixel RGB Hybrid Event-Based Vision Sensor with 4.88 $\mu$ m-Pitch Event Pixels and up to 10K Event Frame Rate by Adaptive Control on Event Sparsity
- 5.3 A 2.97 $\mu$ m-Pitch Event-Based Vision Sensor with Shared Pixel Front-End Circuitry and Low-Noise Intensity Readout Mode
- 5.6 A 400 $\times$ 200 600fps 117.7dB-DR SPAD X-Ray Detector with Seamless Global Shutter and Time-Encoded Extrapolation Counter
- 5.8 Dual-Port CMOS Image Sensor with Regression-Based HDR Flux-to-Digital Conversion and 80ns Rapid-Update Pixel-Wise Exposure Coding
- 11.1 A Scalable Heterogeneous Integrated Two-Stage Vertical Power Delivery Architecture for High Performance Computing
- 11.5 A 21W 94.8%-Efficient Reconfigurable Single Inductor Multi-Stage Hybrid DC-DC Converter
- 11.6 A 42W Reconfigurable Bidirectional Power Delivery Voltage-Regulating Cable
- 16.2 A 28nm 53.8TOPS/W 8b Sparse Transformer Accelerator with In-Memory Butterfly Zero Skipper for Unstructured-Pruned NN and CIM-Based Local-Attention-Reusable Engine
- 18.1 A W-Band Transceiver Array with 2.4GHz LO Synchronization Enabling Full Scalability for FMCW Radar
- 21.3 A CMOS Multi-Functional Biosensor Array for Rapid Low-Concentration Analyte Detection with On-Chip DEP-Assisted Active Enrichment and Manipulation with No External Electrodes
- 21.4 A 263 GHz 32-channel EPR-on-a-chip injection-locked VCO-array
- 21.5 An LTE-Harvesting BLE-to-WiFi Backscattering Chip for Single-Device RFID-Like Interrogation
- 22.2 A 28nm 2D/3D Unified Sparse Convolution Accelerator with Block-Wise Neighbor Searcher for Large-Scaled Voxel-Based Point Cloud Network
- 22.5 C-DNN: A 24.5-85.8TOPS/W Complementary-Deep-Neural-Network Processor with Heterogeneous CNN/SNN Core Architecture and Forward-Gradient-Based Sparsity Generation

## EE2:

**Integrated Circuits in an Interconnected World**

**Organizers:** Alicia Klinefelter, *NVIDIA, Durham, NC*  
Deeksha Lal, *pSemi, Raleigh, NC*

**Co-Organizers:** Elnaz Ansari, *Meta, Menlo Park, CA*  
Zeynep Deniz, *IBM, Yorktown Heights, NY*  
Najme Ebrahimi, *University of Florida, Gainesville, FL*  
Dina El-Damak, *German University in Cairo, Cairo, Egypt*  
Preet Garcha, *TI, Dallas, TX*  
Ulkuhan Guler, *WPI, Worcester, MA*  
Awani Khodkumbhe, *UC Berkeley, Berkeley, CA*  
Kwantae Kim, *University/ETH Zürich, Zürich, Switzerland*  
Shalini Lal, *pSemi, Raleigh, NC*  
Jiamin Li, *SUSTech, Shenzhen, China*  
Kazuko Nishimura, *Panasonic, Moriguchi, Japan*  
Michella Rustom, *USC, Los Angeles, CA*  
Trudy Stetzler, *Halliburton, Houston, TX*  
Rabia Yazicigil Kirby, *Boston University, Boston, MA*  
Farhana Sheikh, *Intel, Hillsboro, OR*  
Kathy Wilcox, *AMD, Boxborough, MA*  
Alice Wang, *Everactive, Plano, TX*

**Moderator:** Maryam Rofougaran, *Movandi, Irvine, CA*

Data-centric applications such as automotive, IoT, and machine learning primarily depend on IC connectivity to meet the demands of high-bandwidth and energy-efficient communication. Product requirement diversity continues to grow, and IC components now face a bottleneck in system performance and power, particularly due to their interconnects. To ensure communication capabilities that meet the demands of emerging applications with ever-increasing features, additional research and focus is needed. This panel focuses on connectivity for the next generation of communication systems and brings together expert panelists to share their perspectives on topics in IC connectivity across wireless, wireline, chip-to-chip, and optical link communications.

**Panelists:** Kyeongha Kwon, *KAIST, Daejeon, South Korea*  
Angad Rekhi, *NVIDIA, Santa Clara, CA*  
Asako Toda, *Intel, San Jose, CA*  
Hua Wang, *ETH Zürich, Zürich, Switzerland*

## EE3:

**The Path to Sustainable IC Ecosystems**

**Organizers:** Yvain Thonnart, *CEA-List, Grenoble, France*  
Rahul Rao, *IBM India, Bangalore, India*

**Co-Organizers:** Mutsumi Hamaguchi, *Sharp, Tenri, Japan*  
Renzhi Liu, *Intel, Hillsboro, OR*  
Yongpan Liu, *Tsinghua University, Beijing, China*

**Champion:** Alicia Klinefelter, *Nvidia, Durham, NC*

**Moderator:** Massimo Alioto, *National University of Singapore, Singapore*

Sustainability has become a major concern in our lives in general, and all the way to IC design. It widened from energy management to include greenhouse gas emissions and pressure on natural resources all along the product lifecycle. These challenges must be taken into account early in product design phases, to rethink system architecture and circuit techniques to favor frugality and reuse and minimize the impact of manufacturing. A deep restructuration of the IC ecosystem to integrate eco-design and reuse will need to arise, either from top-down political intervention or company-driven initiatives. How do we facilitate an economically viable path to sustainable IC ecosystem? Will this come from market incentives or are government regulations required? With a growing awareness of this challenge, several initiatives have already emerged for sustainable electronics, coming from research labs, companies, citizens, or governments. This panel confronts these approaches and explores their potential to create this economy viable path via market incentive or government regulation, for a sustainable value chain all over the product lifecycle.

**Panelists:** Carole-Jean Wu, *Meta, Cambridge, MA*  
Yogesh Ramadass, *Texas Instruments, Santa Clara, CA*  
Marcus Pan, *SRC, Durham, NC*  
Todd Brady, *Intel, Chandler, AZ*  
Jo De Boeck, *imec, Leuven, Belgium*  
Andreia Cathelin, *STMicroelectronics, Crolles, France*



SRAM Compute-In-Memory

Session Chair: *Kyu-Hyoun (KH) Kim*, IBM T. J. Watson, Yorktown Heights, NY  
Session Co-Chair: *Violante Moschiano*, Intel, Avezzano, Italy

8:30 AM

7.1 **A 22nm 832kb Hybrid-Domain Floating-Point SRAM In-Memory-Compute Macro with 16.2-70.2TFLOPS/W for High-Accuracy AI-Edge Devices**

*P-C. Wu<sup>\*1</sup>, J-W. Su<sup>\*1,2</sup>, L-Y. Hong<sup>1</sup>, J-S. Ren<sup>1</sup>, C-H. Chien<sup>1</sup>, H-Y. Chen<sup>1</sup>, C-E. Ke<sup>1</sup>, H-M. Hsiao<sup>2</sup>, S-H. L<sup>2</sup>, S-S. Sheu<sup>2</sup>, W-C. Lo<sup>2</sup>, S-C. Chang<sup>2</sup>, C-C. Lo<sup>1</sup>, R-S. Liu<sup>1</sup>, C-C. Hsieh<sup>1</sup>, K-T. Tang<sup>1</sup>, M-F. Chang<sup>1</sup>*

<sup>1</sup>National Tsing Hua University, Hsinchu, Taiwan

<sup>2</sup>Industrial Technology Research Institute, Hsinchu, Taiwan, <sup>\*</sup>Equally Credited Authors (ECAs)

9:00 AM

7.2 **A 28nm 64kb 31.6-TFLOPS/W Digital-Domain Floating-Point-Computing-Unit and Double-bit 6T-SRAM Computing-in-Memory Macro for Floating-Point CNNs**

*A. Guo, X. Si, X. Chen, F. Dong, X. Pu, D. Li, Y. Zhou, L. Ren, Y. Xue, X. Dong, H. Gao, Y. Zhang, J. Zhang, Y. Kong, T. Xiong, B. Wang, H. Cai, W. Shan, J. Yang*, Southeast University, Nanjing, China

9:30 AM

7.3 **A 28nm 38-to-102-TOPS/W 8b Multiply-Less Approximate Digital SRAM Compute-In-Memory Macro for Neural-Network Inference**

*Y. He<sup>1</sup>, H. Diao<sup>2</sup>, C. Tang<sup>1</sup>, W. Jia<sup>1</sup>, X. Tang<sup>2</sup>, Y. Wang<sup>2</sup>, J. Yue<sup>3</sup>, X. Li<sup>1</sup>, H. Yang<sup>1</sup>, H. Jia<sup>1</sup>, Y. Liu<sup>1</sup>*

<sup>1</sup>Tsinghua University, Beijing, China; <sup>2</sup>Peking University, Beijing, China

<sup>3</sup>Chinese Academy of Sciences, Beijing, China

Break 10:00 AM

10:15 AM

7.4 **A 4nm 6163-TOPS/W/b 4790-TOPS/mm<sup>2</sup>/b SRAM Based Digital-Computing-in-Memory Macro Supporting Bit-Width Flexibility and Simultaneous MAC and Weight Update**

*H. Mori<sup>1</sup>, W-C. Zhao<sup>1</sup>, C-E. Lee<sup>1</sup>, C-F. Lee<sup>1</sup>, Y-H. Hsu<sup>1</sup>, C-K. Chuang<sup>1</sup>, T. Hashizume<sup>2</sup>, H-C. Tung<sup>1</sup>, Y-Y. Liu<sup>1</sup>, S-R. Wu<sup>1</sup>, K. Akarvardar<sup>3</sup>, T-L. Chou<sup>1</sup>, H. Fujiwara<sup>1</sup>, Y. Wang<sup>1</sup>, Y-D. Chih<sup>1</sup>, Y-H. Chen<sup>1</sup>, H-J. Liao<sup>1</sup>, T-Y. J. Chang<sup>1</sup>*, <sup>1</sup>TSMC, Hsinchu, Taiwan; <sup>2</sup>TSMC, Yokohama, Japan

<sup>3</sup>TSMC, San Jose, CA

10:45 AM

7.5 **A 28nm Horizontal-Weight-Shift and Vertical-Feature-Shift-Based Separate-Wordline 6T-SRAM Computation-in-Memory Unit-Macro for Edge Depthwise Neural-Networks**

*B. Wang, C. Xue, Z. Feng, Z. Zhang, H. Liu, L. Ren, X. Li, A. Yin, T. Xiong, Y. Xue, S. He, Y. Kong, Y. Zhou, A. Guo, X. Si, J. Yang*, Southeast University, Nanjing, China

11:00 AM

7.6 **A 70.85-86.27-TOPS/W PVT-Insensitive 8b Word-Wise ACIM with Post Processing Relaxation**

*S-E. Hsieh<sup>1</sup>, C-H. Wei<sup>1</sup>, C-X. Xue<sup>1</sup>, H-W. Lin<sup>1</sup>, W-H. Tu<sup>1</sup>, E-J. Chang<sup>1</sup>, K-T. Yang<sup>1</sup>, P-H. Chen<sup>1</sup>, W-N. Liao<sup>1</sup>, L. L. Low<sup>2</sup>, C-D. Lee<sup>1</sup>, A-C. Lu<sup>1</sup>, J. Liang<sup>1</sup>, C-C. Cheng<sup>1</sup>, T-H. Kang<sup>1</sup>*

<sup>1</sup>MediaTek, Hsinchu, Taiwan; <sup>2</sup>MediaTek, Singapore, Singapore

11:15 AM

7.7 **CV-CIM: A 28nm XOR-derived Similarity-aware Computation-In-Memory For Cost Volume Construction**

*Z. Yue, Y. Wang, H. Wang, Y. Wang, R. Guo, L. Tang, L. Liu, S. Wei, Y. Hu, S. Yin*  
Tsinghua University, Beijing, China

11:30 AM

7.8 **A 22nm Delta-Sigma Computing-In-Memory ( $\Delta\Sigma$ CIM) SRAM Macro with Near-Zero-Mean Outputs and LSB-First ADCs Achieving 21.38TOPS/W for 8b-MAC Edge AI Processing**

*P. Chen<sup>\*1</sup>, M. Wu<sup>\*1</sup>, W. Zhao<sup>1</sup>, J. Cui<sup>1</sup>, Z. Wang<sup>1,2</sup>, Y. Zhang<sup>3</sup>, Q. Wang<sup>3</sup>, J. Ru<sup>1</sup>, L. Shen<sup>1</sup>, T. Jia<sup>1</sup>, Y. Ma<sup>1</sup>, L. Ye<sup>1,2</sup>, R. Huang<sup>1</sup>*, <sup>1</sup>Peking University, Beijing, China

<sup>2</sup>Advanced Institute of Information Technology of Peking University, Hangzhou, China

<sup>3</sup>Nano Core Chip Electronic Technology, Hangzhou, China, <sup>\*</sup>Equally Credited Authors (ECAs)

11:45 AM

7.9 **CTLE-Ising: A 1440-Spin Continuous-Time Latch-Based Ising Machine with One-Shot Fully-Parallel Spin Updates Featuring Equalization of Spin States**

*J. Bae<sup>\*</sup>, W. Oh<sup>\*</sup>, J. Koo, B. Kim*

University of California, Santa Barbara, CA, <sup>\*</sup>Equally Credited Authors (ECAs)

Conclusion 12:15 PM

GHz-to-millimeter Wave Frequency Generation

Session Chair: *Swaminathan Sankaran*, Texas Instruments, Dallas, TX  
Session Co-Chair: *Mona Hella*, Rensselaer Polytechnic Institute, Troy, NY

8:30 AM

- 8.1 **A 11.5-to-14.3GHz 192.8dBc/Hz FoM at 1MHz Offset Dual-Core Enhanced Class-F VCO with Common-Mode-Noise Self-Cancellation and Isolation Technique**  
*Q. Wu, W. Deng, H. Jia, H. Liu, S. Zhang, Z. Wang, B. Chi*  
Tsinghua University, Beijing, China

8:45 AM

- 8.2 **A 22.4-to-26.8GHz Dual-Path-Synchronized Quad-Core Oscillator Achieving -138dBc/Hz PN and 193.3dBc/Hz FoM at 10MHz Offset from 25.8GHz**  
*X. Zhan<sup>1</sup>, J. Yin<sup>1</sup>, P.-I. Mak<sup>1</sup>, R. P. Martins<sup>1,2</sup>*  
<sup>1</sup>University of Macau, Macau, China  
<sup>2</sup>Instituto Superior Tecnico/University of Lisboa, Lisboa, Portugal

9:00 AM

- 8.3 **A 28GHz Scalable Inter-Core-Shaping Multi-Core Oscillator with DM/CM-Configured Coupling Achieving 193.3dBc/Hz FoM and 205.5dBc/Hz FoM<sub>A</sub> at 1MHz Offset**  
*Y. Shu, Z. Deng, X. Luo*  
University of Electronic Science and Technology of China, Chengdu, China

9:30 AM

- 8.4 **An 83.3-to-104.7GHz Harmonic-Extraction VCO Incorporating Multi-Resonance, Multi-Core, and Multi-Mode (3M) Techniques Achieving -124dBc/Hz Absolute PN and 190.7dBc/Hz FoM<sub>T</sub>**  
*H. Guo<sup>1</sup>, Y. Chen<sup>1</sup>, Y. Huang<sup>1</sup>, P.-I. Mak<sup>1</sup>, R. P. Martins<sup>1,2</sup>*  
<sup>1</sup>University of Macau, Macau, China  
<sup>2</sup>Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

Break 10:00 AM

Highlighted Chip Releases: Digital and Machine Learning Processors

Session Chair: *Alicia Klinefelter*, NVIDIA, Durham, NC  
Session Co-Chair: *Vivek De*, Intel, Beaverton, OR

10:15 AM

- 9.1 **A 7nm ML Training Processor with Wave Clock Distribution**  
*T. C. Fischer<sup>1</sup>, A. K. Nivarti<sup>1</sup>, R. Ramachandran<sup>1</sup>, R. Bharti<sup>1</sup>, D. Carson<sup>1</sup>, A. Lawrendra<sup>1</sup>, V. Mudgal<sup>1</sup>, V. Santhosh<sup>1</sup>, S. Shukla<sup>2</sup>, T.-C. Tsai<sup>1</sup>*  
<sup>1</sup>Tesla, Palo Alto, CA  
<sup>2</sup>Tesla, Austin, TX

10:45 AM

- 9.2 **A 1mW Always-on Computer Vision Deep Learning Neural Decision Processor**  
*D. Garrett, Y.-S. Park, S. Kim, J. Sharma, W. Huang, M. Shaghaghi, V. Parthasarathy, S. Gibellini, S. Bailey, M. Moturi, P. Vorenkamp, K. Busch, J. Holleman, B. Javid, A. Yousefi, M. Judy, A. Gupta*  
Syntiant, Irving, CA

11:15 AM

- 9.3 **NVLink-C2C: A Coherent Off Package Chip-to-Chip Interconnect with 40Gbps/pin Single-ended Signaling**  
*Y. Wei<sup>1</sup>, Y. C. Huang<sup>2</sup>, H. Tang<sup>1</sup>, N. Sankaran<sup>1</sup>, I. Chadha<sup>1</sup>, D. Dai<sup>1</sup>, O. Oluwole<sup>1</sup>, V. Balan<sup>1</sup>, E. Lee<sup>1</sup>*  
<sup>1</sup>Nvidia, Santa Clara, CA  
<sup>2</sup>Nvidia, Hsinchu, Taiwan

11:45 AM

- 9.4 **An In-Depth Look at the Intel IPU E2000**  
*B. Burres<sup>\*1</sup>, N. Sundar<sup>\*2</sup>, Y. Li<sup>\*3</sup>*  
<sup>1</sup>Intel, Hudson, MA  
<sup>2</sup>Intel, Santa Clara, CA  
<sup>3</sup>Intel, Portland, OR  
<sup>\*</sup>Equally Credited Authors (ECAs)

Conclusion 12:15 PM

Pipelined and Noise-Shaping ADCs

Session Chair: *Nima Maghari*, University of Florida, Gainesville, FL  
Session Co-Chair: *Ping Gui*, Southern Methodist University, Dallas, TX

8:30 AM

10.1 A 1.8GHz 12b Pre-Sampling Pipelined ADC with Reference Buffer and OP Power Relaxations

*S-E. Hsieh, T-C. Wu, C-C. Hou*  
MediaTek, Hsinchu, Taiwan

9:00 AM

10.2 A Single-Channel 2.6GS/s 10b Dynamic Pipelined ADC with Time-Assisted Residue Generation Scheme Achieving Intrinsic PVT Robustness

*J. Hao<sup>1,2</sup>, M. Zhang<sup>1</sup>, Y. Zhang<sup>1,2</sup>, S. Liu<sup>2</sup>, Z. Zhu<sup>2</sup>, Y. Zhu<sup>1</sup>, C-H. Chan<sup>1</sup>, R. P. Martins<sup>1,3</sup>*  
<sup>1</sup>University of Macau, Macau, China  
<sup>2</sup>Xidian University, Xi'an, China  
<sup>3</sup>Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

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10.3 A Single-Channel 12b 2GS/s PVT-Robust Pipelined ADC with Critically Damped Ring Amplifier and Time-Domain Quantizer

*Y. Cao<sup>1</sup>, M. Zhang<sup>1</sup>, Y. Zhu<sup>1</sup>, C-H. Chan<sup>1</sup>, R. P. Martins<sup>1,2</sup>*  
<sup>1</sup>University of Macau, Macau, China  
<sup>2</sup>Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

Break 10:00 AM

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10.4 A Rail-to-Rail 12MS/s 91.3dB SNDR 94.1dB DR Two-Step SAR ADC with Integrated Input Buffer Using Predictive Level-Shifting

*M. Li<sup>1</sup>, C. Y. Lee<sup>1</sup>, A. ElShater<sup>1</sup>, Y. Miyahara<sup>2</sup>, K. Sobue<sup>2</sup>, K. Tomioka<sup>2</sup>, U-K. Moon<sup>1</sup>*  
<sup>1</sup>Oregon State University, Corvallis, OR  
<sup>2</sup>Asahi Kasei Microdevices, Atsugi, Japan

10:45 AM

10.5 A 25MHz-BW 77.2dB-SNDR 2<sup>nd</sup>-Order Gain-Error-Shaping and NS Pipelined SAR ADC Based on a Quantization-Prediction-Unrolled Scheme

*H. Zhang<sup>1</sup>, Y. Zhu<sup>1</sup>, C-H. Chan<sup>1</sup>, R. P. Martins<sup>1,2</sup>*  
<sup>1</sup>University of Macau, Macau, China  
<sup>2</sup>Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

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10.6 A 150kHz-BW 15-ENOB Incremental Zoom ADC with Skipped Sampling and Single Buffer Embedded Noise-Shaping SAR Quantizer

*Z. Wang<sup>1</sup>, L. Jie<sup>2</sup>, Z. Kong<sup>1</sup>, M. Zhan<sup>2</sup>, Y. Zhong<sup>2</sup>, Y. Wang<sup>1</sup>, X. Tang<sup>1</sup>*  
<sup>1</sup>Peking University, Beijing, China  
<sup>2</sup>Tsinghua University, Beijing, China

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10.7 A Single-Channel 70dB-SNDR 100MHz-BW 4<sup>th</sup>-Order Noise-Shaping Pipeline SAR ADC with Residue Amplifier Error Shaping

*Y. Zhang<sup>\*1,2</sup>, J. Hao<sup>1,2</sup>, S. Liu<sup>2</sup>, Z. Zhu<sup>2</sup>, Y. Zhu<sup>1</sup>, C-H. Chan<sup>\*1</sup>, R. P. Martins<sup>1,3</sup>*  
<sup>1</sup>University of Macau, Macau, China  
<sup>2</sup>Xidian University, Xi'an, China  
<sup>3</sup>Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal  
<sup>\*</sup>Equally Credited Authors (ECAs)

Conclusion 12:15 PM

USB and Compute Power Delivery

Session Chair: *Harish Krishnamurthy, Intel, Hillsboro, OR*  
Session Co-Chair: *Chan-Hong Chern, TSMC, Hsinchu, Taiwan*

8:30 AM

**11.1 A Scalable Heterogeneous Integrated Two-Stage Vertical Power Delivery Architecture for High Performance Computing**

DS1

*C. Hardy<sup>1</sup>, H. Pham<sup>1</sup>, M. M. Jatlaoui<sup>2</sup>, F. Voiron<sup>2</sup>, T. Xie<sup>1</sup>, P-H. Chen<sup>1</sup>, S. Jha<sup>1</sup>, P. Mercier<sup>1</sup>, H-P. Le<sup>1</sup>*  
<sup>1</sup>University of California, San Diego, CA; <sup>2</sup>Murata, Caen, France

9:00 AM

**11.2 A 12-1 Quad-Output Switched-Capacitor Buck Converter with Shared DC Capacitors Achieving 90.4% Peak Efficiency and 48mA/mm<sup>3</sup> Power Density at 85% Efficiency**

*T. Hu<sup>1</sup>, M. Huang<sup>1</sup>, Y. Lu<sup>1</sup>, R. P. Martins<sup>1,2</sup>*  
<sup>1</sup>University of Macau, Macau, China; <sup>2</sup>Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

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**11.3 A 1.8W High-Frequency SIMO Converter Featuring Digital Sensor-Less Computational Zero-Current Operation and Non-Linear Duty-Boost**

*S. Kim<sup>1</sup>, H. K. Krishnamurthy<sup>1</sup>, S. Sofer<sup>2</sup>, S. Weng<sup>1</sup>, S. Wolf<sup>2</sup>, A. Ravi<sup>1</sup>, K. Ravichandran<sup>1</sup>, O. Degan<sup>2</sup>, J. W. Tschanz<sup>1</sup>, V. De<sup>1</sup>, <sup>1</sup>Intel, Hillsboro, OR; <sup>2</sup>Intel, Haifa, Israel*

9:45 AM

**11.4 A Double Step-down Dual-output Converter with Cross Regulation of 0.025mV/mA and Improved Current Balance**

*W-C. Hung<sup>1</sup>, C-W. Chen<sup>1</sup>, Y-W. Huang<sup>1</sup>, A. Chen<sup>1</sup>, Z-Y. Yang<sup>1</sup>, K-H. Chen<sup>1</sup>, K-L. Zheng<sup>1,2</sup>, Y-H. Lin<sup>3</sup>, S-R. Lin<sup>3</sup>, T-Y. Tsa<sup>3</sup>, W-C. Huang<sup>1</sup>*  
<sup>1</sup>National Yang Ming Chiao Tung University, Hsinchu, Taiwan  
<sup>2</sup>Chip-GaN Power Semiconductor, Hsinchu, Taiwan; <sup>3</sup>Realtek Semiconductor, Hsinchu, Taiwan

Break 10:00 AM

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**11.5 A 21W 94.8%-Efficient Reconfigurable Single Inductor Multi-Stage Hybrid DC-DC Converter**

DS1

*C. Hardy, H-P. Le, University of California, San Diego, CA*

10:45 AM

**11.6 A 42W Reconfigurable Bidirectional Power Delivery Voltage-Regulating Cable**

DS1

*Z. Tong<sup>1</sup>, J. Huang<sup>1</sup>, Y. Lu<sup>1</sup>, R. P. Martins<sup>1,2</sup>*  
<sup>1</sup>University of Macau, Macau, China; <sup>2</sup>Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

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**11.7 A Wide 0.1-10 Conversion-Ratio Symmetric Hybrid Buck-Boost Converter for USB PD Bidirectional Conversion**

*C. Lin<sup>1</sup>, C-S. Hung<sup>1</sup>, S-Y. Li<sup>1</sup>, Y-T. Hsu<sup>1</sup>, K-H. Chen<sup>1</sup>, K-L. Zheng<sup>1,2</sup>, Y-H. Lin<sup>3</sup>, S-R. Lin<sup>3</sup>, T-Y. Tsa<sup>3</sup>*  
<sup>1</sup>National Yang Ming Chiao Tung University, Hsinchu, Taiwan  
<sup>2</sup>Chip-GaN Power Semiconductor, Hsinchu, Taiwan; <sup>3</sup>Realtek Semiconductor, Hsinchu, Taiwan

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**11.8 A 5A 94.5% Peak Efficiency 9~16V-to-1V Dual-Path Series-Capacitor Converter with Full Duty Range and Low V-A Metric**

*X. Yang, L. Zhao, M. Zhao, Z. Tan, Y. Ding, W. Li, W. Qu, Zhejiang University, Hangzhou, China*

11:45 AM

**11.9 A Compact 12V-to-1V 91.8% Peak Efficiency Hybrid Resonant Switched-Capacitor Parallel Inductor (ReSC-PL) Buck Converter**

*G. Cai<sup>1</sup>, Y. Lu<sup>1</sup>, R. P. Martins<sup>1,2</sup>*  
<sup>1</sup>University of Macau, Macau, China; <sup>2</sup>Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

12:00 PM

**11.10 A 12V-Input 1V-1.8V-Output 93.7% Peak Efficiency Dual-Inductor Quad-Path Hybrid DC-DC Converter**

*W-L. Zeng<sup>1,2</sup>, G. Cai<sup>1</sup>, C-F. Lee<sup>1</sup>, C-S. Lam<sup>1</sup>, Y. Lu<sup>1</sup>, S-W. Sin<sup>1</sup>, R. P. Martins<sup>1,3</sup>*  
<sup>1</sup>University of Macau, Macau, China  
<sup>2</sup>Zhuhai UM Science & Technology Research Institute, Zhuhai, China  
<sup>3</sup>Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

Conclusion 12:15 PM

High Performance Optical Receivers

Session Chair: *Byungsub Kim*, POSTECH, Pohang, Korea

Session Co-Chair: *Thomas Toiff*, Cisco Systems, Gattikon, Switzerland

8:30 AM

- 12.1 A 0.96pJ/b 7×50Gb/s-per-Fiber WDM Receiver with Stacked 7nm CMOS and 45nm Silicon Photonic Dies**  
*M. Raji<sup>1</sup>, C. Xie<sup>1</sup>, A. Bekele<sup>1</sup>, A. Chou<sup>1</sup>, W. Zhang<sup>1</sup>, Y. Cao<sup>1</sup>, J. W. Kim<sup>1</sup>, N. Narang<sup>2</sup>, H. Zhao<sup>2</sup>, Y. Wang<sup>2</sup>, K. H. Tan<sup>2</sup>, W. Lin<sup>1</sup>, J. Im<sup>1</sup>, D. Mahashin<sup>1</sup>, S. Asuncion<sup>1</sup>, P. Upadhyaya<sup>1</sup>, Y. Frans<sup>1</sup>*  
<sup>1</sup>AMD, San Jose, CA; <sup>2</sup>AMD, Singapore, Singapore

9:00 AM

- 12.2 A 7 pA/√Hz Asymmetric Differential TIA for 100Gb/s PAM-4 Links with -14dBm Optical Sensitivity in 16nm CMOS**  
*K. Lakshmikummar<sup>\*1</sup>, A. Kurylak<sup>\*1</sup>, R. K. Nandwana<sup>\*1</sup>, B. Das<sup>1</sup>, J. Pampanin<sup>1</sup>, M. Brubaker<sup>1</sup>, P. K. Hanumolu<sup>2</sup>*, <sup>1</sup>CISCO Systems, Allentown, PA; <sup>2</sup>University of Illinois, Urbana, IL  
*\*Equally Credited Authors (ECAs)*

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- 12.3 A Carrier Phase Recovery Loop for a 3.2pJ/bit 24Gb/s QPSK Coherent Optical Receiver**  
*A. Abdelrahman<sup>1</sup>, M. G. Ahmed<sup>1,2</sup>, M. A. Khalil<sup>1</sup>, M. B. Younis<sup>1</sup>, K-S. Park<sup>1</sup>, P. K. Hanumolu<sup>1</sup>*  
<sup>1</sup>University of Illinois, Urbana, IL; <sup>2</sup>now at Ain Shams University, Cairo, Egypt

Break 10:00 AM

Ideas for the Future

Session Chair: *Sudip Shekhar*, University of British Columbia, Vancouver, Canada

Session Co-Chair: *Daniel Morris*, Meta, Menlo Park, CA

10:15 AM

- 13.1 Crystalline Oxide Semiconductor-Based 3D Bank Memory System for Endpoint Artificial Intelligence with Multiple Neural Networks Facilitating Context Switching and Power Gating**  
*Y. Yakubo<sup>1</sup>, K. Furutani<sup>1</sup>, K. Toyotaka<sup>1</sup>, H. Katagiri<sup>1</sup>, M. Fujita<sup>1</sup>, M. Kozuma<sup>1</sup>, Y. Ando<sup>1</sup>, Y. Kurokawa<sup>1</sup>, T. Nakura<sup>2</sup>, S. Yamazaki<sup>1</sup>*  
<sup>1</sup>Semiconductor Energy Laboratory, Atsugi, Japan; <sup>2</sup>Fukuoka University, Fukuoka, Japan

10:45 AM

- 13.2 A 47nW Mixed-Signal Voice Activity Detector (VAD) Featuring a Non-Volatile Capacitor-ROM, a Short-Time CNN Feature Extractor and an RNN Classifier**  
*J. Lin<sup>1</sup>, K-F. Un<sup>1</sup>, W-H. Yu<sup>1</sup>, P-I. Mak<sup>1</sup>, R. P. Martins<sup>1,2</sup>*  
<sup>1</sup>University of Macau, Macau, China  
<sup>2</sup>Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

11:15 AM

- 13.3 A Triturated Sensing System**  
*N. Miura<sup>1</sup>, K. Naruse<sup>1</sup>, J. Shiomi<sup>1</sup>, Y. Midoh<sup>1</sup>, T. Hirose<sup>1</sup>, T. Okidono<sup>2</sup>, T. Miki<sup>2</sup>, M. Nagata<sup>2</sup>*  
<sup>1</sup>Osaka University, Suita, Japan; <sup>2</sup>Kobe University, Kobe, Japan

11:30 AM

- 13.4 A Self-Programming PUF Harvesting the High-Energy Plasma During Fabrication**  
*K. Naruse, T. Ueda, J. Shiomi, Y. Midoh, N. Miura*  
Osaka University, Suita, Japan

11:45 AM

- 13.5 Subtractive Photonic Waveguide-Coupled Photodetectors in 180nm Bulk CMOS**  
*C. Ives, A. Hajimiri*  
California Institute of Technology, Pasadena, CA

12:00 PM

- 13.6 A Silicon Photonic Reconfigurable Optical Analog Processor (SiROAP) with a 4×4 Optical Mesh**  
*M. J. Shawon, V. Saxena*  
University of Delaware, Newark, DE

Conclusion 12:15 PM

Digital Techniques for Clocking and Power Management

Session Chair: *Arijit Raychowdhury, Georgia Institute of Technology, Atlanta, GA*

Session Co-Chair: *Eric Fang, Mediatek, Hsinchu City, Taiwan*

1:30 PM

14.1 A Fractional-N Digital MDLL with Injection Error Scrambling and Background Third-Order DTC Delay Equalizer Achieving -67dBc Fractional Spur

*Q. Zhang<sup>1</sup>, H-C. Cheng<sup>1</sup>, S. Su<sup>1,2</sup>, M. S-W. Chen<sup>1</sup>*

<sup>1</sup>University of Southern California, Los Angeles, CA; <sup>2</sup>University of Waterloo, Waterloo, Canada

2:00 PM

14.2 A 10-to-300MHz Fractional Output Divider with -80dBc Worst-Case Fractional Spurs Using Auxiliary-PLL-Based Background 0th/1st/2nd-Order DTC INL Calibration

*Y. Yang, W. Deng, A. Yan, H. Jia, J. Gong, Z. Wang, B. Chi, Tsinghua University, Beijing, China*

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14.3 A Digital Low-Dropout (LDO) Linear Regulator with Adaptive Transfer Function Featuring 125A/mm<sup>2</sup> Power Density and Autonomous Bypass Mode

*M. Zelikson, K. Luria, L. Gil, Y. Brown, V. Goldenbeg, D. Kasif, E. Hlees, A. Vinichuk*

Intel, Haifa, Israel

2:45 PM

14.4 A Monolithic 26A/mm<sup>2</sup> I<sub>max</sub>, 88.5% Peak-Efficiency Continuously Scalable Conversion-Ratio Switched-Capacitor DC-DC Converter

*N. Butzen<sup>1</sup>, H. Krishnamurthy<sup>1</sup>, Z. Ahmed<sup>1</sup>, S. Weng<sup>1</sup>, K. Ravichandran<sup>1</sup>, M. Zelikson<sup>2</sup>, J. Tschanz<sup>1</sup>, J. Douglas<sup>3</sup>, <sup>1</sup>Intel, Hillsboro, OR; <sup>2</sup>Intel, Haifa, Israel; <sup>3</sup>Intel, Chandler, AZ*

Break 3:00 PM

IOT & Security

Session Chair: *Chiraag Juvekar, Apple, Mountain View, CA*

Session Co-Chair: *Ingrid Verbauwhede, KU Leuven, Leuven, Belgium*

3:15 PM

15.1 A Self-Powered SoC with Distributed Cooperative Energy Harvesting and Multi-Chip Power Management for System-in-Fiber

*X. Liu<sup>1</sup>, D. S. Truesdell<sup>1</sup>, O. Faruqe<sup>1</sup>, L. Parameswaran<sup>2</sup>, M. Rickley<sup>2</sup>, A. Kopansk<sup>2</sup>, L. Cantley<sup>2</sup>, A. Coon<sup>2</sup>, M. Bernasconi<sup>2</sup>, T. Wang<sup>2</sup>, B. H. Calhoun<sup>1</sup>*

<sup>1</sup>University of Virginia, Charlottesville, VA; <sup>2</sup>MIT Lincoln Laboratory, Lexington, MA

3:45 PM

DS2 15.2 A 2.19μW Self-Powered SoC with Integrated Multimodal Energy Harvesting, Dual-Channel up to -92dBm WRX and Energy-Aware Subsystem

*C. J. Lukas<sup>1</sup>, F. B. Yahya<sup>1</sup>, K-K. Huang<sup>2</sup>, J. Boley<sup>2</sup>, D. S. Truesdell<sup>1</sup>, J. Breiholz<sup>1</sup>, A. Wokhlu<sup>2</sup>, K. Craig<sup>1</sup>, J. K. Brown<sup>3</sup>, A. Fitting<sup>2</sup>, W. Moore<sup>2</sup>, A. Shih<sup>2</sup>, A. Wang<sup>2</sup>, A. Grave<sup>2</sup>, D. D. Wentzloff<sup>3</sup>, B. H. Calhoun<sup>1</sup>*

<sup>1</sup>Everactive, Charlottesville, VA; <sup>2</sup>Everactive, Santa Clara, CA; <sup>3</sup>Everactive, Ann Arbor, MI

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15.3 A 33kDMIPS 6.4W Vehicle Communication Gateway Processor Achieving 10Gbps/W Network Routing, 40ms CAN Bus Start-Up and 1.4mW Standby Power

*K. Shimada, K. Sano, K. Fukuoka, H. Morita, M. Daito, T. Kamei, H. Hamasaki, Y. Shimazaki*

Renesas Electronics, Tokyo, Japan

4:45 PM

15.4 A 28nm 68MOPS 0.18μJ/Op Paillier Homomorphic Encryption Processor with Bit-Serial Sparse Ciphertext Computing

*G. Shi<sup>1</sup>, Z. Tan<sup>1</sup>, D. Cao<sup>2</sup>, J. Cai<sup>1</sup>, W. Zhang<sup>3</sup>, Y. Wu<sup>3</sup>, K. Ma<sup>1</sup>*

<sup>1</sup>Tsinghua University, Beijing, China; <sup>2</sup>Xi'an JiaoTong University, Xi'an, China

<sup>3</sup>Polar Bear Tech, Xi'an, China

5:15 PM

DS2 15.5 A 100Gbps Fault-Injection Attack Resistant AES-256 Engine with 99.1-to-99.99% Error Coverage in Intel 4 CMOS

*R. Kumar<sup>1</sup>, A. Varna<sup>2</sup>, C. Tokunaga<sup>1</sup>, S. Taneja<sup>1</sup>, V. De<sup>1</sup>, S. Mathew<sup>1</sup>*

<sup>1</sup>Intel, Hillsboro, OR; <sup>2</sup>Intel, Chandler, AZ

Conclusion 5:30 PM

Efficient Compute-In-Memory-Based Processors for ML

Session Chair: *Jae-sun Seo*, Arizona State University, Tempe, AZ

Session Co-Chair: *Yongpan Liu*, Tsinghua University, Beijing, China

1:30 PM

16.1 **MuTICIM: A 28nm 2.24μJ/Token Attention-Token-Bit Hybrid Sparse Digital CIM-Based Accelerator for Multimodal Transformers**

*F. Tu, Z. Wu, Y. Wang, W. Wu, L. Liu, Y. Hu, S. Wei, S. Yin*

Tsinghua University, Beijing, China

2:00 PM

16.2 **A 28nm 53.8TOPS/W 8b Sparse Transformer Accelerator with In-Memory Butterfly Zero Skipper for Unstructured-Pruned NN and CIM-Based Local-Attention-Reusable Engine**

DS1

*S. Liu<sup>1</sup>, P. Li<sup>1</sup>, J. Zhang<sup>1</sup>, Y. Wang<sup>1</sup>, H. Zhu<sup>1</sup>, W. Jiang<sup>1</sup>, S. Tang<sup>2</sup>, C. Chen<sup>1,3</sup>, Q. Liu<sup>1</sup>, M. Liu<sup>1</sup>*

<sup>1</sup>Fudan University, Shanghai, China

<sup>2</sup>BIRENTECH, Shanghai, China; <sup>3</sup>Peng Cheng Laboratory, Shenzhen, China

2:30 PM

16.3 **A 28nm 16.9-300TOPS/W Computing-in-Memory Processor Supporting Floating-Point NN Inference/Training with Intensive-CIM Sparse-Digital Architecture**

*J. Yue<sup>1</sup>, C. He<sup>1</sup>, Z. Wang<sup>1</sup>, Z. Cong<sup>1</sup>, Y. He<sup>2</sup>, M. Zhou<sup>2</sup>, W. Sun<sup>2</sup>, X. Li<sup>2</sup>, C. Dou<sup>1</sup>, F. Zhang<sup>1</sup>, H. Yang<sup>2</sup>, Y. Liu<sup>2</sup>, M. Liu<sup>1</sup>*

<sup>1</sup>Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China

<sup>2</sup>Tsinghua University, Beijing, China

Break 3:00 PM

3:15 PM

16.4 **TensorCIM: A 28nm 3.7nJ/Gather and 8.3TFLOPS/W FP32 Digital-CIM Tensor Processor for MCM-CIM-Based Beyond-NN Acceleration**

*F. Tu, Y. Wang, Z. Wu, W. Wu, L. Liu, Y. Hu, S. Wei, S. Yin*

Tsinghua University, Beijing, China

3:45 PM

16.5 **DynaPlasia: An eDRAM In-Memory-Computing-Based Reconfigurable Spatial Accelerator with Triple-Mode Cell for Dynamic Resource Switching**

*S. Kim, Z. Li, S. Um, W. Jo, S. Ha, J. Lee, S. Kim, D. Han, H.-J. Yoo*

Korea Advanced Institute of Science and Technology, Daejeon, Korea

4:15 PM

16.6 **A Nonvolatile AI-Edge Processor with 4MB SLC-MLC Hybrid-Mode ReRAM Compute-in-Memory Macro and 51.4-251TOPS/W**

*W.-H. Huang<sup>\*1</sup>, T.-H. Wen<sup>\*1,2</sup>, J.-M. Hung<sup>\*1</sup>, W.-S. Khwa<sup>\*2</sup>, Y.-C. Lo<sup>1</sup>, C.-J. Jhang<sup>1,2</sup>, H.-H. Hsu<sup>1</sup>, Y.-H. Chin<sup>1</sup>, Y.-C. Chen<sup>1</sup>, C.-C. Lo<sup>1</sup>, R.-S. Liu<sup>1</sup>, K.-T. Tang<sup>1</sup>, C.-C. Hsieh<sup>1</sup>, Y.-D. Chih<sup>3</sup>, T.-Y. Chang<sup>3</sup>, M.-F. Chang<sup>1,2</sup>*

<sup>1</sup>National Tsing Hua University, Hsinchu, Taiwan; <sup>2</sup>TSMC Corporate Research, Hsinchu, Taiwan

<sup>3</sup>TSMC, Hsinchu, Taiwan; <sup>\*</sup>Equally Credited Authors (ECAs)

4:45 PM

16.7 **A 40-310TOPS/W SRAM-Based All-Digital Up to 4b In-Memory Computing Multi-Tiled NN Accelerator in FD-SOI 18nm for Deep-Learning Edge Applications**

*G. Desoli<sup>\*1</sup>, N. Chawla<sup>\*2</sup>, T. Boesch<sup>\*3</sup>, M. Ayodhyawasi<sup>\*2</sup>, H. Rawat<sup>2</sup>, H. Chawla<sup>2</sup>, A. VS<sup>2</sup>, P. Zambotti<sup>4</sup>, A. Sharma<sup>2</sup>, C. Cappetta<sup>1</sup>, M. Rossi<sup>1</sup>, A. De Vita<sup>1</sup>, F. Girardi<sup>1</sup>*

<sup>1</sup>STMicroelectronics, Cornaredo, Italy; <sup>2</sup>STMicroelectronics, Noida, India

<sup>3</sup>STMicroelectronics, Geneva, Switzerland; <sup>4</sup>STMicroelectronics, Agrate, Italy

<sup>\*</sup>Equally Credited Authors (ECAs)

Conclusion 5:15 PM

High-Speed Data Converters

Session Chair: *John Keane*, Keysight Technologies, Santa Clara, CA

Session Co-Chair: *Ying-Zu Lin*, Mediatek, HsinChu, Taiwan

1:30 PM

**17.1 A 2×-Interleaved 9b 2.8GS/s 5b/cycle SAR ADC with Linearized Configurable V2T Buffer Achieving >50dB SNDR at 3GHz Input**

DS2

*H. Zhao<sup>1</sup>, M. Zhang<sup>1</sup>, Y. Zhu<sup>1</sup>, C-H. Chan<sup>1</sup>, R. P. Martins<sup>1,2</sup>*

<sup>1</sup>University of Macau, Macao, China

<sup>2</sup>Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

2:00 PM

**17.2 An 8b 1.0-to-1.25GS/s 0.7-to-0.8V Single-Stage Time-Based Gated-Ring-Oscillator ADC with 2× Interpolating Sense-Amplifier-Latches**

*A. S. Yonar<sup>1,2</sup>, P. A. Francese<sup>1</sup>, M. Brändli<sup>1</sup>, M. Kossel<sup>1</sup>, M. Prathapan<sup>1</sup>, T. Morfi<sup>1</sup>, A. Ruffino<sup>1</sup>, T. Jang<sup>2</sup>*

<sup>1</sup>IBM Zurich Research Laboratory, Zurich, Switzerland

<sup>2</sup>ETH Zürich, Zurich, Switzerland

2:30 PM

**17.3 A 14b 16GS/s Time-Interleaving Direct-RF Synthesis DAC with T-DEM Achieving -70dBc IM3 up to 7.8GHz in 7nm**

*W-H. Tseng<sup>\*1</sup>, W. Lin<sup>\*1</sup>, C-W. Hsu<sup>1</sup>, C-Y. Huang<sup>1</sup>, Y-S. Lin<sup>1</sup>, H-Y. Huang<sup>1</sup>, H. Chen<sup>1</sup>, S-H. Liao<sup>1</sup>,*

*K-D. Chen<sup>1</sup>, J. Strange<sup>2</sup>, G. Manganaro<sup>3</sup>*

<sup>1</sup>MediaTek, HsinChu, Taiwan; <sup>2</sup>MediaTek, Kent, United Kingdom; <sup>3</sup>MediaTek, Woburn, MA

\*Equally Credited Authors (ECAs)

Break 3:00 PM

3:15 PM

**17.4 A 750mW 24GS/s 12b Time-Interleaved ADC for Direct RF Sampling in Modern Wireless Systems**

*S. Santhosh Kumar<sup>1</sup>, M. Kudo<sup>1</sup>, V. Cretu<sup>1</sup>, A. Morineau<sup>1</sup>, A. Matsuda<sup>2</sup>, M. Yoshida<sup>2</sup>, M. Marutan<sup>2</sup>,*

*A. H. Maniyar<sup>1</sup>, J. Kumar<sup>1</sup>*

<sup>1</sup>Socionext Europe, Maidenhead, United Kingdom

<sup>2</sup>Socionext, Yokohama, Japan

3:45 PM

**17.5 A 10mW 10-ENOB 1GS/s Ring-Amp-Based Pipelined TI-SAR ADC with Split MDAC and Switched Reference Decoupling Capacitor**

*M. Zhan, L. Jie, N. Sun*

Tsinghua University, Beijing, China

4:15 PM

**17.6 A 7b 4.5GS/s 4× Interleaved SAR ADC with Fully On-Chip Background Timing Skew Calibration**

DS2

*Y-H. Wang, S-J. Chang*

National Cheng Kung University, Tainan, Taiwan

4:45 PM

**17.7 A 3mW 2.7GS/s 8b Subranging ADC with Multiple-Reference-Embedded Comparators**

*J-C. Wang, T-H. Kuo*

National Cheng Kung University, Tainan, Taiwan

5:00 PM

**17.8 A Single-Channel 10GS/s 8b >36.4dB SNDR Time-Domain ADC Featuring Loop-Unrolled Asynchronous Successive Approximation in 28nm CMOS**

*Q. Chen<sup>1</sup>, Y. Liang<sup>\*1</sup>, C. C. Boon<sup>1</sup>, Q. Liu<sup>2</sup>*

<sup>1</sup>Nanyang Technological University, Singapore, Singapore

<sup>2</sup>Kun Gao Xinxin Technologies, Singapore, Singapore

\*Equally Credited Authors (ECAs)

Conclusion 5:15 PM



**mm-Wave & sub-THz for Wireless and Sensing**Session Chair: *Jane Gu, University of California, Davis, Davis, CA*Session Co-Chair: *Giuseppe Gramegna, imec, Leuven, Belgium*

1:30 PM

**18.1 A W-Band Transceiver Array with 2.4GHz LO Synchronization Enabling Full Scalability for FMCW Radar****DS1***J. Zhang, A. Singhvi, S. S. Ahmed, A. Arbabian, Stanford University, Stanford, CA*

2:00 PM

**18.2 A 128Gb/s 1.95pJ/b D-Band Receiver with Integrated PLL and ADC in 22nm FinFET***A. Agrawal<sup>1</sup>, A. Whitcombe<sup>2</sup>, W. Shin<sup>3</sup>, R. Bhat<sup>1</sup>, S. Kundu<sup>1</sup>, P. Sagazio<sup>1</sup>, H. Chandrakumar<sup>1</sup>, T. Brown<sup>1</sup>, B. Carlton<sup>1</sup>, C. Hul<sup>4</sup>, S. Callender<sup>1</sup>, S. Pellerano<sup>1</sup>*<sup>1</sup>Intel, Hillsboro, OR; <sup>2</sup>Intel, Santa Clara, CA; <sup>3</sup>now with Apple, Sunnyvale, CA<sup>4</sup>now with Amazon, Redmond, WA

2:30 PM

**18.3 71-to-89GHz 12Gb/s Double-Edge-Triggered Quadrature RFDAC with LO Leakage Suppression Achieving 20.5dBm Peak Output Power and 20.4% System Efficiency***B. Yang, Z. Deng, H. J. Qian, X. Luo**University of Electronic Science and Technology of China, Chengdu, China*

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**18.4 A 4×4 607GHz Harmonic Injection-Locked Receiver Array Achieving 4.4pW/√Hz NEP in 28nm CMOS***A. De Vroede, P. Reynaert, KU Leuven ESAT-MICAS, Heverlee, Belgium*

Break 3:00 PM

**5G and Satcom: Receivers and Transmitters**Session Chair: *Venumadhav Bhagavatula, Samsung Semiconductor, San Jose, CA*Session Co-Chair: *Alireza Zolfaghari, Broadcom, Irvine, CA*

3:15 PM

**19.1 A 300MHz-BW, 27-to-38dBm In-Band OIP3 sub-7GHz Receiver for 5G Local Area Base Station Applications***M. A. Montazerolghaem, L. C. N. de Vreede, M. Babaie**Delft University of Technology, Delft, The Netherlands*

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**19.2 An Interferer-Tolerant Harmonic-Resilient Receiver with >+10dBm 3<sup>rd</sup>-Harmonic Blocker P<sub>1dB</sub> for 5G NR Applications***S. Araei, S. Mohin, N. Reiskarimian, Massachusetts Institute of Technology, Cambridge, MA*

4:15 PM

**19.3 A 2.95mW/element Ka-band CMOS Phased-Array Receiver Utilizing On-Chip Distributed Radiation Sensors in Low-Earth-Orbit Small Satellite Constellation***X. Fu<sup>1</sup>, D. You<sup>1</sup>, X. Wang<sup>1</sup>, M. Ide<sup>1</sup>, Y. Zhang<sup>1</sup>, J. Sakamaki<sup>1</sup>, A. A. Fadila<sup>1</sup>, Z. Li<sup>1</sup>, Y. Wang<sup>1</sup>, J. Sudo<sup>2</sup>, M. Higaki<sup>2</sup>, S. Inoue<sup>2</sup>, T. Eishima<sup>2</sup>, T. Tomura<sup>1</sup>, J. Pang<sup>1</sup>, H. Sakai<sup>1</sup>, K. Okada<sup>1</sup>, A. Shirane<sup>1</sup>*<sup>1</sup>Tokyo Institute of Technology, Tokyo, Japan; <sup>2</sup>Axelspace, Tokyo, Japan

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**19.4 A Small-Satellite-Mounted 256-Element Ka-Band CMOS Phased-Array Transmitter Achieving 63.8dBm EIRP Under 26.6W Power Consumption Using Single/Dual Circular Polarization Active Coupler****DS2***D. You<sup>1</sup>, X. Fu<sup>1</sup>, X. Wang<sup>1</sup>, Y. Gao<sup>1</sup>, W. Wang<sup>1</sup>, J. Sakamaki<sup>1</sup>, H. Herdian<sup>1</sup>, S. Kato<sup>1</sup>, M. Ide<sup>1</sup>, Y. Zhang<sup>1</sup>, A. A. Fadila<sup>1</sup>, Z. Li<sup>1</sup>, C. Wang<sup>1</sup>, Y. Wang<sup>1</sup>, J. Sudo<sup>2</sup>, M. Higaki<sup>2</sup>, N. Kawaguchi<sup>2</sup>, M. Nitta<sup>2</sup>, S. Inoue<sup>2</sup>, T. Eishima<sup>2</sup>, T. Tomura<sup>1</sup>, J. Pang<sup>1</sup>, H. Sakai<sup>1</sup>, K. Okada<sup>1</sup>, A. Shirane<sup>1</sup>*<sup>1</sup>Tokyo Institute of Technology, Tokyo, Japan; <sup>2</sup>Axelspace, Tokyo, Japan

Conclusion 5:15 PM

GaN Power Conversion

Session Chair: *Patrik Arno, ST Microelectronics, Grenoble, France*

Session Co-Chair: *Saurav Bandyopadhyay, Texas Instruments, Dallas, TX*

1:30 PM

**20.1 A High Common-Mode Transient Immunity GaN-on-SOI Gate Driver for High dV/dt SiC Power Switch**

DS2

*S.-Y. Li<sup>1</sup>, W.-C. Hung<sup>1</sup>, T.-W. Wang<sup>1</sup>, Y.-T. Hsu<sup>1</sup>, K.-H. Chen<sup>1</sup>, K.-L. Zheng<sup>1,2</sup>, Y.-H. Lin<sup>3</sup>, S.-R. Lin<sup>3</sup>, T.-Y. Tsa<sup>3</sup>*

<sup>1</sup>National Yang Ming Chiao Tung University, Hsinchu, Taiwan

<sup>2</sup>Chip-GaN Power Semiconductor, Hsinchu, Taiwan

<sup>3</sup>Realtek Semiconductor, Hsinchu, Taiwan

2:00 PM

**20.2 A Condition-Adaptive  $\Delta f^3$ -EMI Control GaN Switching Regulator With Modulation Frequency Envelope Tracking For Full-Spectrum Automotive CISPR 25 Compliance**

*L. Du<sup>1</sup>, D. Yan<sup>1,2</sup>, D. B. Ma<sup>1</sup>*

<sup>1</sup>University of Texas at Dallas, Richardson, TX

<sup>2</sup>Texas Instruments, Dallas, TX

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**20.3 A GaN Gate Driver with On-Chip Adaptive On-time Controller and Negative Current Slope Detector**

*S.-Y. Lin<sup>1</sup>, S.-Y. Lin<sup>1</sup>, S.-H. Hung<sup>1</sup>, T.-W. Wang<sup>1</sup>, C.-H. Li<sup>1</sup>, C.-L. Go<sup>1</sup>, S.-C. Huang<sup>1</sup>, K.-H. Chen<sup>1</sup>, K.-L. Zheng<sup>1,2</sup>, Y.-H. Lin<sup>3</sup>, S.-R. Lin<sup>3</sup>, T.-Y. Tsa<sup>3</sup>*

<sup>1</sup>National Yang Ming Chiao Tung University, Hsinchu, Taiwan

<sup>2</sup>Chip-GaN Power Semiconductor, Hsinchu, Taiwan

<sup>3</sup>Realtek Semiconductor, Hsinchu, Taiwan

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**20.4 Multiple-Phase Accelerated Current Control in Bidirectional Energy Transfer of Automotive High-Voltage and Low-Voltage Batteries**

*T.-W. Wang<sup>1</sup>, S.-Y. Li<sup>1</sup>, S.-H. Hung<sup>1</sup>, T.-Y. Wu<sup>1</sup>, C.-Y. Chen<sup>1</sup>, P.-J. Chiu<sup>1</sup>, K.-H. Chen<sup>1</sup>, K.-L. Zheng<sup>1,2</sup>, Y.-H. Lin<sup>3</sup>, T.-Y. Tsa<sup>3</sup>, S.-R. Lin<sup>3</sup>*

<sup>1</sup>National Yang Ming Chiao Tung University, Hsinchu, Taiwan

<sup>2</sup>Chip-GaN Power Semiconductor, Hsinchu, Taiwan

<sup>3</sup>Realtek Semiconductor, Hsinchu, Taiwan

Break 3:00 PM

Emerging Sensing Systems and IOT

Session Chair: *Kaushik Sengupta*, Princeton University, Princeton, NJ  
Session Co-Chair: *Milin Zhang*, Tsinghua University, Beijing, China

3:15 PM

21.1 A 65nm CMOS Living-Cell Dynamic Fluorescence Sensor with 1.05fA Sensitivity at 600/700nm Wavelengths

*F. Aghlmand<sup>1</sup>, C. Hu<sup>1,2</sup>, S. Sharma<sup>1</sup>, K. K. Pochana<sup>1</sup>, R. M. Murray<sup>1</sup>, A. Emami<sup>1</sup>*

<sup>1</sup>California Institute of Technology, Pasadena, CA

<sup>2</sup>Texas A&M University, College Station, TX

3:45 PM

21.2 A 22μW Peak Power Multimodal Electrochemical Sensor Interface IC for Bioreactor Monitoring

*Q. Lin<sup>1</sup>, W. Sijbers<sup>1</sup>, C. Avdikou<sup>1</sup>, D. Gomez<sup>1,2</sup>, D. Biswas<sup>1</sup>, S. Sneha<sup>3</sup>, A. Malissov<sup>3</sup>, B. Tacca<sup>3</sup>, N. V. Helleputte<sup>1</sup>*

<sup>1</sup>imec, Leuven, Belgium

<sup>2</sup>Now with MPS Spain, Barcelona, Spain

<sup>3</sup>imec - Holst Centre, Eindhoven, The Netherlands

4:00 PM

21.3 A CMOS Multi-Functional Biosensor Array for Rapid Low-Concentration Analyte Detection with On-Chip DEP-Assisted Active Enrichment and Manipulation with No External Electrodes

DS1

*D. Lee<sup>1</sup>, D. Jung<sup>2</sup>, F. Jiang<sup>1</sup>, G. V. June<sup>3</sup>, J. Park<sup>4</sup>, H. Liu<sup>1</sup>, Y. Kong<sup>1</sup>, Y. Kim<sup>1</sup>, J. Wang<sup>1</sup>, H. Wang<sup>1,3</sup>*

<sup>1</sup>ETH Zürich, Zurich, Switzerland

<sup>2</sup>Qualcomm, San Jose

<sup>3</sup>Georgia Institute of Technology, Atlanta, GA

<sup>4</sup>Apple, San Diego, CA

4:15 PM

21.4 A 263GHz 32-Channel EPR-on-a-Chip Injection-Locked VCO-Array

DS1

*A. Chu<sup>\*1</sup>, M. Kern<sup>\*1</sup>, K. Khan<sup>1</sup>, K. Lips<sup>2</sup>, J. Anders<sup>1,3</sup>*

<sup>1</sup>University of Stuttgart, Stuttgart, Germany

<sup>2</sup>Helmholtz-Zentrum Berlin für Materialien und Energie, Berlin, Germany

<sup>3</sup>Institute for Microelectronics Stuttgart (IMS CHIPS), Stuttgart, Germany

\*Equally Credited Authors (ECAs)

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21.5 An LTE-Harvesting BLE-to-WiFi Backscattering Chip for Single-Device RFID-Like Interrogation

DS1

*S-K. Kuo<sup>\*</sup>, M. Dunna<sup>\*</sup>, H. Lu, A. Agarwal, D. Bharadia, P. P. Mercier*

University of California, San Diego, CA

\*Equally Credited Authors (ECAs)

5:00 PM

21.6 ASIL-D Compliant Battery Monitoring IC with High Measurement Accuracy and Robust Communication

*J-K. Lee<sup>1,2</sup>, S. Woo<sup>2</sup>, W. Jeong<sup>2</sup>, K-S. Oh<sup>2</sup>, D. Kim<sup>2</sup>, Y. Ko<sup>2</sup>, J-Y. Jeon<sup>2</sup>, J. Lee<sup>2</sup>, Y-S. Son<sup>2</sup>, S-G. Lee<sup>1</sup>, K. Kwon<sup>1</sup>*

<sup>1</sup>Korea Advanced Institute of Science and Technology, Daejeon, Korea

<sup>2</sup>Autosilicon, Daejeon, Korea

Conclusion 5:30 PM

# TIMETABLE OF ISSCC 2023 SESSIONS

## ISSCC 2023 • SUNDAY FEBRUARY 19<sup>TH</sup> • Q&A IN-PERSON TUTORIALS

### Tutorials

|   |  |   |
|---|--|---|
| <b>10:00 AM - T1:</b> Fundamentals of Frequency References                    | <b>10:20 AM - T2:</b> Bridging RF and Power:<br>An Introduction to Envelope Tracking Systems and Building Blocks | <b>10:40 AM - T3:</b> Fundamentals of Data Converters   |
| <b>11:00 AM - T4:</b> Automotive System Design                                | <b>11:20 AM - T5:</b> All-Digital PLLs: From Fundamental Concepts to Future Trends                               | <b>11:40 AM - T6:</b> Solid-State CMOS LiDAR Sensors  |
| <b>1:00 PM - T7:</b> Fundamentals of Ultra-Low Voltage Embedded Memory Design | <b>1:20 PM - T8:</b> Role of Current-Mode Passive Mixers and N-Path Filters in RF Receivers                      | <b>1:40 PM - T9:</b> Physical-Layer Security for Latency- and Energy-Constrained Integrated Systems |
| <b>2:00 PM - T10:</b> The Art of mm-Wave Design and Layout                    | <b>2:20 PM - T11:</b> Digital Equalization and Timing Recovery Techniques for ADC-DSP Based Highspeed Links      | <b>2:40 PM - T12:</b> Extending Processor Cores for Machine Learning                                |

## ISSCC 2023 • SUNDAY FEBRUARY 19<sup>TH</sup>

### Forums

|         |  |  |   |
|---------|--|--|---|
| 8:00 AM | <b>F1:</b> Transceivers for Exascale: Towards Tbps/mm and Sub-pJ/bit | <b>F2:</b> The Power Behind Electrical Vehicles – Accelerating the Future of Automotive Technology | <b>F3:</b> Efficient Wireless Power Amplification and Linearization |
|---------|--|--|---|

### Events Below in Bold Box are Included with your Conference Registration

#### Evening Events

|  |   |   |
|--|---|---|
|  | <b>3:00 - 5:00 PM:</b> Mentoring Session / Networking Bingo Event | <b>8:00 PM – EE1:</b> Student Research Preview: Short Presentations with Poster Session |
|--|---|---|

## ISSCC 2023 • MONDAY FEBRUARY 20<sup>TH</sup> • PAPER SESSIONS

|  |   |  |                                      |  |  |
|--|---|--|--------------------------------------|--|--|
| 8:30 AM  | Session 1: Plenary Session                          |  |                                      |  |  |
| 1:30 PM  | Session 2:<br>Digital Processors                    | Session 3:<br>Amplifiers and Oscillators | Session 4:<br>Frequency Synthesizers | Session 5:<br>Image Sensors                | Session 6:<br>Advanced Wireline Links and Techniques |
| 12noon to 7:00 PM – Book Displays • 5:00 PM to 7:00 PM – Demonstration Session • 5:15 PM – Author Interviews • Social Hour |   |  |                                      |  |  |
| Evening Events   |   |  |                                      |  |  |
| 8:00 PM  | EE2: Integrated Circuits in an Interconnected World |  |                                      | EE3: The Path to Sustainable IC Ecosystems |  |

## ISSCC 2023 • TUESDAY FEBRUARY 21<sup>ST</sup> • PAPER SESSIONS

|  |  |  |  |  |  |
|--|--|--|--|--|--|
| 8:30 AM  | <b>Session 7:</b><br>SRAM Compute-In-Memory                                | <b>Session 8:</b><br>GHz-to-Millimeter Wave Frequency Generation                           | <b>Session 10:</b><br>Pipelined and Noise-Shaping ADCs | <b>Session 11:</b><br>USB and Compute Power Delivery                               | <b>Session 12:</b><br>High Performance Optical Receivers |
|  |  | <b>Session 9:</b><br>Highlighted Chip Releases:<br>Digital and Machine Learning Processors |  |  | <b>Session 13:</b><br>Ideas for the Future               |
| 1:30 PM  | <b>Session 14:</b><br>Digital Techniques for Clocking and Power Management | <b>Session 16:</b><br>Efficient Compute-In-Memory Based Processors for ML                  | <b>Session 17:</b><br>High-Speed Data Converters       | <b>Session 18:</b><br>mm-Wave & sub-THz for Wireless and Sensing                   | <b>Session 20:</b><br>GaN Power Conversion               |
|  | <b>Session 15:</b><br>IOT & Security                                       |  |  | <b>Session 19:</b><br>5G and Satcom: Receivers and Transmitters                    | <b>Session 21:</b><br>Emerging Sensing Systems and IOT   |
| 10:00 AM to 7:00 PM – Book Displays • 5:00 PM to 7:00 PM – Demonstration Session • 5:15 PM – Author Interviews |  |  |  |  |  |
| Evening Events   |  |  |  |  |  |
| 8:00 PM  | <b>EE4:</b> The Smartest Designer in The Universe, Post-Pandemic!          |  |  | <b>EE5:</b> What will be the Essential Skills for IC Designers in the Next Decade? |  |

## ISSCC 2023 • WEDNESDAY FEBRUARY 22<sup>ND</sup> • PAPER SESSIONS

|   |   |   |   |   |  |
|---|---|---|---|---|--|
| 8:30 AM   | <b>Session 22:</b><br>Heterogenous ML Accelerators                | <b>Session 23:</b><br>Analog Sensor Interfaces    | <b>Session 24:</b><br>THz Signal Generation                                 | <b>Session 26:</b><br>Display and User Interaction Technologies   | <b>Session 28:</b><br>High-Density Memories and High-Speed Interface |
|   |   |   | <b>Session 25:</b><br>RF Transceiver Building Blocks                        | <b>Session 27:</b><br>Innovations from Outside the (ISSCC) Box    |  |
| 1:30 PM   | <b>Session 29:</b><br>Digital Accelerators and Circuit Techniques | <b>Session 30:</b><br>Power Management Techniques | <b>Session 31:</b><br>Energy-Efficient Radios for UWB, BMI, and IoT Systems | <b>Session 32:</b><br>Intelligent Biomedical Circuits and Systems | <b>Session 33:</b><br>Non-Volatile Memory and Compute-In-Memory      |
|   |   |   |   |   | <b>Session 34:</b><br>Cryo-CMOS for Quantum Computing                |
| 10:00 AM to 3:00 PM – Book Displays • 5:15 PM – Author Interviews |   |   |   |   |  |

## ISSCC 2023 • THURSDAY FEBRUARY 23<sup>RD</sup>

|         |   |   |   |  |   |
|---------|---|---|---|--|---|
| 8:00 AM | <b>Short Course:</b><br>Principles of Quantum Computing and the Application of Cryoelectronics to Qubit Control and Readout | <b>F4:</b><br>Advancing Technologies for Extended Reality (XR) to Make the “Metaverse” Possible | <b>F5:</b><br>Extreme Data Converters and Their Peripherals | <b>F6:</b><br>The Future of Heterogeneous Multi-Core Architectures for AI and Other Specialized Processing | <b>F7:</b><br>Advanced Circuits and Technologies for Wearable and Implantable Devices |
|---------|---|---|---|--|---|

## Demonstration Session 2, Tuesday, February 21<sup>st</sup>, 5:00-7:00 PM

This year, the Demonstration Session extending in selected regular papers, both Academic and Industrial, will take place on Monday February 20<sup>th</sup>, and Tuesday February 21<sup>st</sup>, from 5 pm until 7 pm in the Golden Gate Hall. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2023, as noted by the symbol **DS2**

- 6.2 A 4.63pJ/b 112Gb/s DSP-Based PAM-4 Transceiver for a Large-Scale Switch in 5nm FinFET
- 15.2 A 2.19 $\mu$ W Self-Powered SoC with Integrated Multimodal Energy Harvesting, Dual-Channel up to -92dBm WRX and Energy-Aware Subsystem
- 15.5 A 100Gbps Fault-Injection Attack Resistant AES-256 Engine with 99.1-to-99.99% Error Coverage in Intel 4 CMOS
- 17.1 A 2 $\times$ -Interleaved 9b 2.8GS/s 5b/cycle SAR ADC with Linearized Configurable V2T Buffer Achieving >50dB SNDR at 3GHz Input
- 17.6 A 7b 4.5GS/s 4 $\times$  Interleaved SAR ADC with Fully On-Chip Background Timing Skew Calibration
- 19.4 A Small-Satellite-Mounted 256-Element Ka-Band CMOS Phased-Array Transmitter Achieving 63.8dBm EIRP Under 26.6W Power Consumption Using Single/Dual Circular Polarization Active Coupler
- 20.1 A High Common-Mode Transient Immunity GaN-on-SOI Gate Driver for High dV/dt SiC Power Switch
- 22.6 ANP-I: A 28nm 1.5pJ/SOP Asynchronous Spiking Neural Network Processor Enabling Sub-0.1 $\mu$ J/Sample On-Chip Learning for Edge-AI Applications
- 22.7 DL-VOPU: An Energy-Efficient Domain-Specific Deep-Learning-Based Visual Object Processing Unit Supporting Multi-Scale Semantic Feature Extraction for Mobile Object Detection/Tracking Applications
- 22.8 A 0.81mm<sup>2</sup> 740 $\mu$ W Real-Time Speech Enhancement Processor Using Multiplier-Less PE Arrays for Hearing Aids in 28nm CMOS
- 23.6 A 2.98pJ/Conversion 0.0023mm<sup>2</sup> Dynamic Temperature Sensor with Fully On-Chip Corrections
- 25.5 A 1-to-5GHz All-Passive Frequency-Translational 4th-Order N-path Filter with Low-Power Clock Boosting for High Linearity and Relaxed P<sub>dc</sub>-Frequency Trade-Off
- 29.1 A 32.5mW Mixed-Signal Processing-in-Memory-Based k-SAT Solver in 65nm CMOS with 74.0% Solvability for 30-Variable 126-Clause 3-SAT Problems
- 29.2 Snap-SAT: A One-Shot Energy-Performance-Aware All-Digital Compute-in-Memory Solver for Large-Scale Hard Boolean Satisfiability Problems
- 29.5 A 73.53TOPS/W 14.74TOPS Heterogeneous RRAM In-Memory and SRAM Near-Memory SoC for Hybrid Frame and Event-Based Target Tracking
- 29.8 A Sub-0.8pJ/b 16.3Gbps/mm<sup>2</sup> Universal Soft-Detection Decoder Using ORBGRAND in 40nm CMOS
- 30.4 A 3.7V-to-1kV Chip-Cascaded Switched-Capacitor Converter with Auxiliary Boost Achieving >96% Reactive Power Efficiency for Electrostatic Drive Applications
- 30.10 Single Chip, Qi Compliant, 40W Wireless Power Transmission Controller using RMS Coil Current Sensing and Adaptive ZVS for 4dB EMI and up to 1.7% Efficiency Improvements
- 31.5 A Passive Bidirectional BLE Tag Demonstrating Battery-Free Communication in Tablet/Smartphone-to-Tag, Tag-to-Tablet/Smartphone, and Tag-to-Tag Modes
- 32.1 A Behind-The-Ear Patch-Type Mental Healthcare Integrated Interface with 275-Fold Input Impedance Boosting and Adaptive Multimodal Compensation Capabilities
- 32.2 A Stimulus-Scattering-Free Pixel-Sharing Sub-Retinal Prosthesis SoC with 35.8dB Dynamic Range Time-Based Photodiode Sensing and Per-Pixel Dynamic Voltage Scaling
- 32.6 SciCNN: A 0-Shot-Retraining Patient-Independent Epilepsy-Tracking SoC
- 33.3 A 9Mb HZO-based Embedded FeRAM Macro with a 1012-Cycle Endurance, a 5ns Read and a 7ns Write Time using ECC-Assisted Data Refresh and an Offset-Canceled Sense Amplifier
- 34.1 THz Cryo-CMOS Backscatter Transceiver: A Contactless 4 Kelvin-300 Kelvin Data Interface

## EE4:

## The Smartest Designer in the Universe, Post-Pandemic!

- Organizer:** Denis Daly, *Apple, Cambridge, MA*
- Co-Organizers:** Shuhei Amakawa, *Hiroshima University, Higashihiroshima, Japan*  
 Negar Reiskarimian, *MIT, Cambridge, MA*  
 Vito Giannini, *Uhnder, Austin, TX*
- Champion:** Tim Piessens, *ICsense, Leuven, Belgium*
- Moderator:** Bram Nauta, *University of Twente, Enschede, The Netherlands*

At ISSCC 2020 there was a battle of epic proportions between industry, academia and students to determine who was the smartest designer in the universe. Industry came out victorious. Now, at ISSCC 2023, as we return to an in-person conference, academia and students have their chance to get their revenge and set the record straight. In this interactive quiz show, three teams representing industry, academia and students will compete for the honor and the prestigious title: "The Smartest Designer in the Universe". In several rounds, the contestants will solve questions and puzzles covering all parts of electrical engineering. They will baffle you with their knowledge, surprise you with their wit and entertain you with their to the point remarks. This all topped with a gentle sauce of irony since the smartest designer in the universe should be smart enough to appreciate the special relativity of it all. Join this session not only to support your own team but enroll in the game. Everybody will be able to actively participate using an app.

**Team Academia:**

Kofi Makinwa, *Delft University of Technology, Delft, The Netherlands*  
 Azita Emami, *Caltech, Pasadena, CA*  
 Howard Luong, *HKUST, Hong Kong, China*

**Team Industry:**

Farhana Sheikh, *Intel, Hillsboro, OR*  
 Rozi Roufoogaran, *NXP, Irvine, CA*  
 Subhashish Mukherjee, *Texas Instruments, Bangalore, Karnataka, India*

## EE5:

## What will be the Essential Skills for IC Designers in the Next Decade?

- Organizer:** Mozghan Mansuri, *Intel, Hillsboro, OR*
- Co-Organizers:** Wei-Zen Chen, *National Yang Ming Chiao Tung University, Hsinchu, Taiwan*  
 Byungsub Kim, *Pohang University of Science and Technology, Pohang, Korea*  
 Visvesh Sathe, *Georgia Institute of Technology, Atlanta, GA*  
 Giuseppe Gramegna, *imec, Leuven, Belgium*
- Moderator:** Mozghan Mansuri, *Intel, Hillsboro, OR*

Based on emerging trends in design methodology such as AI for IC design and verification, this session of academic and industry leaders will predict and discuss how future design automation will change the way IC designers work in the next decade. Will more and more of IC design be automated by then? Is our field shrinking? Are we attracting and training enough students to learn IC design to meet potential industry needs? Join this special evening topic session to get the perspective of industry and academic leaders in IC design.

**Panelists:** Mike Flynn, *University of Michigan, Ann Arbor, MI*  
 Hoi-Jun Yoo, *KAIST, Daejeon, Korea*  
 Alvin Loke, *NXP Semiconductors, San Diego, CA*  
 Laura Smith, *AMD, Austin, TX*

Heterogeneous ML Accelerator

Session Chair: *Rangharajan Venkatesan, NVIDIA, Santa Clara, CA*

Session Co-Chair: *Sophia Shao, UC Berkeley, Berkeley, CA*

8:30 AM

22.1 **A 12.4TOPS/W @ 136GOPS AI-IoT System-on-Chip with 16 RISC-V, 2-to-8b Precision-Scalable DNN Acceleration and 30%-Boost Adaptive Body Biasing**

*F. Conti<sup>1</sup>, D. Rossi<sup>1</sup>, G. Paulin<sup>2</sup>, A. Garofalo<sup>1</sup>, A. Di Mauro<sup>2</sup>, G. Rutishauer<sup>2</sup>, G. Ottavi<sup>1</sup>, M. Eggmann<sup>2</sup>, H. Okuhara<sup>1</sup>, V. Huard<sup>3</sup>, O. Montfort<sup>3</sup>, L. Jure<sup>3</sup>, N. Exibard<sup>3</sup>, P. Gouedo<sup>3</sup>, M. Louvat<sup>3</sup>, E. Botte<sup>3</sup>, L. Benini<sup>1,2</sup>*, <sup>1</sup>University of Bologna, Bologna, Italy; <sup>2</sup>ETH Zürich, Zürich, Switzerland

<sup>3</sup>Dolphin Design, Meylan, France

9:00 AM

22.2 **A 28nm 2D/3D Unified Sparse Convolution Accelerator with Block-Wise Neighbor Searcher for Large-Scaled Voxel-Based Point Cloud Network**

*W. Sun<sup>1</sup>, X. Feng<sup>2</sup>, C. Tang<sup>2</sup>, S. Fan<sup>2</sup>, Y. Yang<sup>2</sup>, J. Yue<sup>3</sup>, Z. Du<sup>4</sup>, W. Zhao<sup>4</sup>, H. Yang<sup>2</sup>, Y. Liu<sup>2</sup>*

<sup>1</sup>Tsinghua Shenzhen International Graduate School, Shenzhen, China

<sup>2</sup>Tsinghua University, Beijing, China; <sup>3</sup>Chinese Academy of Sciences, Beijing, China

<sup>4</sup>Pi2star Technology, Beijing, China

9:30 AM

22.3 **A 127.8TOPS/W Arbitrarily Quantized 1-to-8b Scalable-Precision Accelerator for General-Purpose Deep Learning with Reduction of Storage, Logic and Latency Waste**

*S. Moon<sup>1</sup>, H-G. Mun<sup>1</sup>, H. Son<sup>2</sup>, J-Y. Sim<sup>1</sup>*

<sup>1</sup>Pohang University of Science and Technology, Pohang, Korea

<sup>2</sup>Gyeongsang National University, Jinju, Korea

Break 10:00 AM

10:15 AM

22.4 **A 28nm 11.2TOPS/W Hardware-Utilization-Aware Neural-Network Accelerator with Dynamic Dataflow**

*C-Y. Du<sup>1</sup>, C-F. Tsa<sup>2</sup>, W-C. Chen<sup>3</sup>, L-Y. Lin<sup>3</sup>, N-S. Chang<sup>3</sup>, C-P. Lin<sup>3</sup>, C-S. Chen<sup>3</sup>, C-H. Yang<sup>1</sup>*

<sup>1</sup>National Taiwan University, Taipei, Taiwan; <sup>2</sup>Delta Electronics, Taipei, Taiwan

<sup>3</sup>Taiwan Semiconductor Research Institute, Hsinchu, Taiwan

10:45 AM

22.5 **C-DNN: A 24.5-85.8TOPS/W Complementary-Deep-Neural-Network Processor with Heterogeneous CNN/SNN Core Architecture and Forward-Gradient-Based Sparsity Generation**

*S. Kim, S. Kim, S. Hong, S. Kim, D. Han, H-J. Yoo*

Korea Advanced Institute of Science and Technology, Daejeon, Korea

11:15 AM

22.6 **ANP-I: A 28nm 1.5pJ/SOP Asynchronous Spiking Neural Network Processor Enabling Sub-0.1μJ/Sample On-Chip Learning for Edge-AI Applications**

*J. Zhang<sup>1</sup>, D. Huo<sup>1</sup>, J. Zhang<sup>1</sup>, C. Qian<sup>1</sup>, Q. Liu<sup>1</sup>, L. Pan<sup>1</sup>, Z. Wang<sup>1</sup>, N. Qiao<sup>2</sup>, K-T. Tang<sup>3</sup>, H. Chen<sup>1</sup>*

<sup>1</sup>Tsinghua University, Beijing, China; <sup>2</sup>SynSense, Chengdu, China

<sup>3</sup>National Tsing Hua University, Hsinchu, Taiwan

11:30 AM

22.7 **DL-VOPU: An Energy-Efficient Domain-Specific Deep-Learning-based Visual Object Processing Unit Supporting Multi-Scale Semantic Feature Extraction for Mobile Object Detection/Tracking Applications**

*Y. Gong, T. Zhang, H. Guo, X. Liu, J. Zheng, H. Wu, C. Jia, L. Que, L. Zhou, L. Chang, J. Zhou*

University of Electronic Science and Technology of China, Chengdu, China

11:45 AM

22.8 **A 0.81mm<sup>2</sup> 740μW Real-Time Speech Enhancement Processor Using Multiplier-Less PE Arrays for Hearing Aids in 28nm CMOS**

*S. Park, S. Lee, J. Park, H-S. Choi, D. Jeon*, Seoul National University, Seoul, Korea

12:00 PM

22.9 **A 12nm 18.1TFLOPs/W Sparse Transformer Processor with Entropy-Based Early Exit, Mixed-Precision Predication and Fine-Grained Power Management**

*T. Tambe<sup>1</sup>, J. Zhang<sup>1</sup>, C. Hooper<sup>1</sup>, T. Jia<sup>2</sup>, P. N. Whatmough<sup>1,3</sup>, J. Zuckerman<sup>4</sup>, M. Cassel Dos Santos<sup>4</sup>, E. J. Loscalzo<sup>4</sup>, D. Giri<sup>4</sup>, K. Shepard<sup>4</sup>, L. Carloni<sup>4</sup>, A. Rush<sup>5</sup>, D. Brooks<sup>1</sup>, G-Y. Wei<sup>1</sup>*

<sup>1</sup>Harvard University, Cambridge, MA; <sup>2</sup>Peking University, Beijing, China; <sup>3</sup>ARM, Boston, MA

<sup>4</sup>Columbia University, New York, NY; <sup>5</sup>Cornell University, New York, NY

Conclusion 12:15 PM

Analog Sensor Interfaces

Session Chair: *Chinwuba Ezekwe, Robert Bosch, Sunnyvale, CA*

Session Co-Chair: *Minkyu Je, KAIST, Daejeon, Korea*

8:30 AM

23.1 **A 7.9fJ/Conversion-Step and 37.12aF<sub>rms</sub> Pipelined-SAR Capacitance-to-Digital Converter with kT/C Noise Cancellation and Incomplete-Settling-Based Correlated Level Shifting**

*J. Gao<sup>1</sup>, L. Shen<sup>1</sup>, H. Li<sup>1</sup>, S. Ye<sup>1</sup>, J. Li<sup>1</sup>, X. Xu<sup>1</sup>, J. Cui<sup>1</sup>, Y. Gao<sup>1</sup>, R. Huang<sup>1</sup>, L. Ye<sup>1,2</sup>*

<sup>1</sup>Peking University, Beijing, China

<sup>2</sup>Advanced Institute of Information Technology of Peking University, Hangzhou, China

9:00 AM

23.2 **A 40A Shunt-Based Current Sensor with ±0.2% Gain Error from -40°C to 125°C and Self-Calibration**

*Z. Tang<sup>1</sup>, N. G. Toth<sup>1</sup>, R. Zamparetti<sup>1</sup>, T. Nezuka<sup>2</sup>, Y. Furuta<sup>2</sup>, K. A. A. Makinwa<sup>1</sup>*

<sup>1</sup>Delft University of Technology, Delft, The Netherlands

<sup>2</sup>MIRISE Technologies, Aichi, Japan

9:30 AM

23.3 **A 51A Hybrid Magnetic Current Sensor with a Dual Differential DC Servo Loop and 43mA<sub>rms</sub> Resolution in a 5MHz Bandwidth**

*A. Jouyaeian<sup>1</sup>, Q. Fan<sup>1</sup>, M. Motz<sup>2</sup>, U. Ausserlechner<sup>2</sup>, K. A. A. Makinwa<sup>1</sup>*

<sup>1</sup>Delft University of Technology, Delft, The Netherlands

<sup>2</sup>Infineon Technologies, Villach, Austria

Break 10:00 AM

10:15 AM

23.4 **A Closed-Loop 12bit CMOS-Integrated Stress Sensor System with 4bit Adjustable Sensitivity from 178 to 11kPa/LSB at up to 22.5kS/s and 5bit Dynamic Range Adjustment**

*K. Allinger<sup>1</sup>, M. Kuhl<sup>2</sup>*

<sup>1</sup>Hamburg University of Technology, Hamburg, Germany

<sup>2</sup>University of Freiburg - IMTEK, Freiburg, Germany

10:45 AM

23.5 **A Sub-1V 810nW Capacitively-Biased BJT-Based Temperature Sensor with an Inaccuracy of ±0.15°C (3σ) from -55°C to 125°C**

*Z. Tang<sup>1</sup>, S. Pan<sup>1,2</sup>, K. A. A. Makinwa<sup>1</sup>*

<sup>1</sup>Delft University of Technology, Delft, The Netherlands

<sup>2</sup>Tsinghua University, Beijing, China

11:15 AM

23.6 **A 2.98pJ/conversion 0.0023mm<sup>2</sup> Dynamic Temperature Sensor with Fully On-Chip Corrections**

DS2

*Y. Shen, H. Li, E. Cantatore, P. Harpe*

Eindhoven University of Technology, Eindhoven, The Netherlands

11:45 AM

23.7 **A BJT-Based Temperature Sensor with ±0.1°C (3σ) Inaccuracy from -55°C to 125°C and a 0.85pJ·K<sup>-2</sup> Resolution FoM Using Continuous-Time Readout**

*N. G. Toth<sup>\*1</sup>, Z. Tang<sup>1</sup>, T. Someya<sup>1,3</sup>, S. Pan<sup>\*1,2</sup>, K. A. A. Makinwa<sup>1</sup>*

<sup>1</sup>Delft University of Technology, Delft, The Netherlands

<sup>2</sup>Tsinghua University, Beijing, China

<sup>3</sup>now with SiTime, Tokyo, Japan

\*Equally Credited Authors (ECAs)

Conclusion 12:15 PM



THz Signal Generation

Session Chair: *Ruonan Han*, Massachusetts Institute of Technology, Cambridge, MA

Session Co-Chair: *Yves Baeyens*, Nokia - Bell Labs, Murray Hill, NJ

8:30 AM

24.1 A 0.64-to-0.69THz Beam-Steerable Coherent Source with 9.1dBm Radiated Power and 30.8dBm Lensless EIRP in 65nm CMOS

*L. Gao, C. H. Chan*, City University of Hong Kong, Hong Kong, China

9:00 AM

24.2 A 264-to-287GHz, -2.5dBm Output Power, and -92dBc/Hz 1MHz-Phase-Noise CMOS Signal Source Adopting a 75fs<sub>rms</sub> Jitter D-Band Cascaded Sub-Sampling PLL

*B-T. Moon, S-G. Lee, J. Choi*

Korea Advanced Institute of Science and Technology, Daejeon, Korea

9:30 AM

24.3 A 200-to-350GHz SiGe BiCMOS Frequency Doubler with Slotline-Based Mode-Decoupling Harmonic Tuning Technique Achieving 1.1-to-4.7dBm Output Power

*S. Li<sup>1</sup>, X. Li<sup>1,2</sup>, H. Wu<sup>1</sup>, W. Chen<sup>1</sup>*

<sup>1</sup>Tsinghua University, Beijing, China; <sup>2</sup>Sanechips Technology, Shenzhen, China

Break 10:00 AM

RF Transceiver Building Blocks

Session Chair: *Jeffrey Walling*, Virginia Tech, Blacksburg, VA

Session Co-Chair: *Hongtao Xu*, Fudan University, Shanghai, China

10:15 AM

25.1 A 4.1W Quadrature Doherty Digital Power Amplifier with 33.6% Peak PAE in 28nm Bulk CMOS

*J. Li<sup>1</sup>, Y. Yin<sup>1</sup>, H. Chen<sup>2</sup>, J. Lin<sup>1</sup>, Y. Li<sup>1</sup>, X. Jia<sup>1</sup>, Z. Hu<sup>1</sup>, X. Zhang<sup>2</sup>, H. Xu<sup>1</sup>*

<sup>1</sup>Fudan University, Shanghai, China; <sup>2</sup>South China University of Technology, Guangzhou, China

10:45 AM

25.2 A 19.7-to-43.8GHz Power Amplifier with Broadband Linearization Technique in 28nm Bulk CMOS

*W. Zeng<sup>1</sup>, L. Gao<sup>1</sup>, N. Sun<sup>1</sup>, H. Xu<sup>2</sup>, Q. Xue<sup>1</sup>, X. Zhang<sup>1</sup>*

<sup>1</sup>South China University of Technology, Guangzhou, China; <sup>2</sup>Fudan University, Shanghai, China

11:15 AM

25.3 A 4.8dB NF, 70-to-86GHz Deep-Noise-Canceling LNA Using Asymmetric Compensation Transformer and 4-to-1 Hybrid-Phase Combiner in 40nm CMOS

*C. Han<sup>\*</sup>, J. Zhou<sup>\*</sup>, Z. Deng, Y. Shu, X. Luo*

University of Electronic Science and Technology of China, Chengdu, China

<sup>\*</sup>Equally Credited Authors (ECAs)

11:45 AM

25.4 A 4b RFDAC at 8GS/s for FMCW Chirps with 4GHz Bandwidth in 10μs

*S. K. Sireesh<sup>1,2</sup>, S. H. Abkenar<sup>1,2</sup>, N. Christoffers<sup>1</sup>, C. Wagner<sup>1</sup>, T. Brandt<sup>1</sup>, A. Stelzer<sup>2</sup>*

<sup>1</sup>Infineon Technologies, Linz, Austria; <sup>2</sup>Johannes Kepler University, Linz, Austria

12:00 PM

DS2 25.5 A 1-to-5GHz All-Passive Frequency-Translational 4th-Order N-path Filter with Low-Power Clock Boosting for High Linearity and Relaxed P<sub>dc</sub>-Frequency Trade-Off

*A. Nagulu<sup>1</sup>, M. Yi<sup>1</sup>, Y. Zhuang<sup>1</sup>, S. Garikapati<sup>2</sup>, H. Krishnaswamy<sup>2</sup>*

<sup>1</sup>Washington University in St. Louis, St. Louis, MO; <sup>2</sup>Columbia University, New York, NY

Conclusion 12:15 PM

Display and User Interaction Technologies

Session Chair: *Joonsung Bae*, Kangwon National University, Chuncheon, Korea

Session Co-Chair: *Johan Vanderhaegen*, Google, Cupertino, CA

8:30 AM

26.1 A Source-Driver IC Including Power-Switching Fast-Slew-Rate Buffer and 8Gb/s Effective 3-Tap DFE Receiver Achieving 4.9mV DVRMS and 17V/ $\mu$ s Slew Rate for 8K Displays and Beyond

*K. Ryu<sup>\*</sup>, J.-Y. Jeong<sup>\*</sup>, J.-P. Lim, K.-H. Lee, K. Kim, Y. Kwon, S. Yoo, S. Kim, H.-W. Lim, J.-Y. Lee*

Samsung Electronics, Hwaseong, Korea

<sup>\*</sup>Equally Credited Authors (ECAs)

9:00 AM

26.2 Virtual Rotating Gesture Recognizable Touch Readout IC for 1.26" Circular Touch Screen Panel

*S. Ko<sup>1</sup>, J. Lee<sup>1</sup>, J. Ham<sup>1</sup>, B. So<sup>2</sup>, D. Cho<sup>2</sup>, H. Kim<sup>2</sup>, B. Kim<sup>2</sup>, W. Sim<sup>2</sup>, G. Youm<sup>2</sup>*

<sup>1</sup>Kwangwoon University, Seoul, Korea

<sup>2</sup>Zinitix, Suwon, Korea

9:30 AM

26.3 A 45.8dB-SNR 120fps 100pF-Load Self-Capacitance Touch-Screen Controller with Enhanced In-Band Common Noise Immunity Using Noise Antenna Reference

*S. Byun, H. Lee, T.-G. Song, J. Lee, J. Baek, G. Ha, S. Baek, Y. Kim, W. Jung, H.-W. Lim, S. Kim, J.-Y. Lee*

Samsung Electronics, Hwaseong, Korea

Break 10:00 AM

Innovations from Outside the (ISSCC) Box

Session Chair: *Ali Hajimiri*, Caltech, Pasadena, CA

Session Co-Chair: *Firooz Aflatouni*, University of Pennsylvania, Philadelphia, PA

10:15 AM

27.1 Some Recent Progress in Bioelectronics

*J. Rogers*

Northwestern University, Evanston, IL

10:45 AM

27.2 The Tall Thin Molecular Programmer

*E. Winfree*

California Institute of Technology, Pasadena, CA

11:15 AM

27.3 The Promise of 2-D Materials for Scaled Digital and Analog Applications

*D. Verreck, P. Wambacq, M. Van de Put, Z. Ahmed, Q. Smets, A. Afzal, R. Dufloy, X. Wu, G. Mirabelli, R. Chen, I. Asselberghs, G. Sankar Kar*

imec, Leuven, Belgium

11:45 AM

27.4 Inverse Designed, Densely Integrated Classical and Quantum Photonics

*J. Vuckovic<sup>1</sup>, G. H. Ahn<sup>2</sup>, K. Van Gasse<sup>1</sup>, M. Guidry<sup>1</sup>, H. Kwon<sup>1</sup>, J. Lu<sup>1</sup>, D. Lukin<sup>1</sup>, A. Piggott<sup>1</sup>, N. Sapr<sup>1</sup>, L. Su<sup>1</sup>, J. Skarda<sup>1</sup>, R. Trivedi<sup>1</sup>, D. Vercruysse<sup>1</sup>, A. White<sup>1</sup>, J. Yang<sup>1</sup>, K. Yang<sup>1</sup>*

<sup>1</sup>Stanford University, Stanford, CA

<sup>2</sup>Stanford University, stanford, CA

Conclusion 12:15 PM

High-Density Memories and High-Speed Interfaces

Session Chair: *Seung-Jae Lee*, Samsung, Hwaseong, Korea

Session Co-Chair: *Dongkyun Kim*, SK hynix, Icheon, Korea

8:30 AM

28.1 A 1.67Tb 5b/Cell Flash Memory Fabricated in a 192-Layer Floating-Gate 3D-NAND Technology and Featuring a 23.3Gb/mm<sup>2</sup> Bit Density

*A. Khakifirooz<sup>1</sup>, E. Anaya<sup>2</sup>, S. Balasubrahmanyam<sup>2</sup>, G. Bennett<sup>1</sup>, D. Castro<sup>2</sup>, J. Egler<sup>2</sup>, K. Fan<sup>2</sup>, R. Ferdous<sup>1</sup>, K. Ganapathi<sup>1</sup>, O. Guzman<sup>2</sup>, C. W. Ha<sup>1</sup>, R. Haque<sup>2</sup>, V. Harish<sup>2</sup>, M. Jalalifar<sup>2</sup>, O. W. Jungroth<sup>2</sup>, S-T. Kang<sup>1</sup>, G. Karbasian<sup>1</sup>, J-Y. Kim<sup>1</sup>, S. L<sup>2</sup>, A. S. Madraswala<sup>2</sup>, S. Maddukur<sup>2</sup>, A. Mohammed<sup>1</sup>, S. Mookiah<sup>2</sup>, S. Nagabhushan<sup>2</sup>, B. Ngo<sup>2</sup>, D. Patel<sup>2</sup>, S. K. Poosarla<sup>2</sup>, N. V. Prabhu<sup>2</sup>, C. Quiroga<sup>2</sup>, S. Rajwade<sup>1</sup>, A. Rahman<sup>2</sup>, J. Shah<sup>2</sup>, R. S. Shenoy<sup>1</sup>, E. Tachie Menson<sup>2</sup>, A. Tankasala<sup>1</sup>, S. K. Thirumala<sup>1</sup>, S. Upadhyay<sup>2</sup>, K. Upadhyayula<sup>2</sup>, A. Velasco<sup>2</sup>, N. K. B. Vemula<sup>2</sup>, B. Venkataramaiah<sup>2</sup>, J. Zhou<sup>1</sup>, B. M. Pathak<sup>2</sup>, P. Kalavade<sup>1</sup>*, <sup>1</sup>Intel, Santa Clara, CA; Intel, Folsom, CA

9:00 AM

28.2 A High Performance 1Tb 3b/Cell 3D-NAND Flash with 194MB/s Write Throughput on over 300 Layers

*B. Kim, S. Lee, B. Hah, K. Park, Y. Park, K. Jo, Y. Noh, H. Seol, H. Lee, J. Shin, S. Choi, Y. Jung, S. Ahn, Y. Park, S. Oh, M. Kim, S. Kim, H. Park, T. Lee, H. Won, M. Kim, C. Koo, Y. Choi, S. Choi, S. Park, D. Youn, J. Lim, W. Park, H. Hur, K. Kwean, H. Choi, W. Jeong, S. Chung, J. Choi, S. Cha* SK hynix Semiconductor, Icheon, Korea

9:30 AM

28.3 A 4nm 16Gb/s/pin Single-Ended PAM4 Parallel Transceiver with Switching-Jitter Compensation and Transmitter Optimization

*J. Jin, S-M. Lee, K. Min, S. Ju, J. Lim, H. Chae, K. Kang, Y. Hong, Y. Jeong, S-H. Kim, J. Lee, J. Kim* Samsung Electronics, Hwaseong, Korea

Break 10:00 AM

10:15 AM

28.4 A 4nm 1.15TB/s HBM3 Interface with Resistor-Tuned Offset-Calibration and In-Situ Margin-Detection

*K. Chae, J. Park, J. Song, B. Koo, J. Oh, S. Yi, W. Lee, D. Kim, T. Yeo, K. Kang, S. Park, E. Kim, S. Jung, S. Park, S. Park, M. Noh, H. Rhew, J. Shin*, Samsung Electronics, Hwaseung, Korea

10:45 AM

28.5 A 900μW, 1–4GHz Input-Jitter-Filtering Digital-PLL-Based 25%-Duty-Cycle Quadrature-Clock Generator for Ultra-Low-Power Clock Distribution in High-Speed DRAM Interfaces

*Y. Shin<sup>\*</sup>, Y. Jo<sup>\*</sup>, J. Kim, J. Lee, J. Kim, J. Choi*

Korea Advanced Institute of Science and Technology, Daejeon, Korea

<sup>\*</sup>Equally Credited Authors (ECAs)

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28.6 A 32Gb/s/pin 0.51pJ/b Single-Ended Resistor-Less Impedance-Matched Transmitter with T-Coil-Based Edge-Boosting Equalizer in 40nm CMOS

*J-H. Park<sup>1</sup>, H. Lee<sup>1</sup>, H. Cho<sup>1</sup>, S. Lee<sup>1</sup>, K-H. Lee<sup>1</sup>, H-G. Ko<sup>2</sup>, D-K. Jeong<sup>1</sup>*

<sup>1</sup>Seoul National University, Seoul, Korea; <sup>2</sup>ONE Semiconductor, Gyeonggi, Korea

11:15 AM

28.7 A 1.1V 6.4Gb/s/pin 24Gb DDR5 SDRAM with Highly Accurate Duty Corrector and NBTI Tolerant DLL

*D. Kwon, H. S. Jeong, J. Choi, W. Kim, J. W. Kim, J. Yoon, J. Choi, S. Lee, H. N. Rie, J-I. Lee, J. Lee, T. Jang, J. Kim, S. Kang, J. Shin, Y. Loh, C. Y. Lee, J. Woo, H. Yu, C. Bae, R. Oh, Y-S. Sohn, C. Yoo, J. Lee*, Samsung Electronics, Hwaseong, Korea

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28.8 A 1.1V 16Gb DDR5 DRAM with Probabilistic-Aggressor Tracking, a Refresh Management Function, Per-Row Hammer Tracking, a Multi-Step Precharge, and Core-Bias-Voltage Modulation for Security and Reliability Enhancement

*W. Kim, C. Jung, S. Yoo, D. Hong, J. Hwang, J. Yoon, O. Jung, J. Choi, S. Hyun, M. Kang, S. Lee, D. Kim, S. Ku, D. Choi, N. Joo, S. Yoon, J. Noh, B. Go, C. Kim, S. Hwang, M. Hwang, S-M. Yi, H. Kim, S. Heo, Y. Jang, K. Jang, S. Chu, Y. Oh, K. Kim, J. Kim, S. Kim, J. Hwang, S. Park, J. Lee, I. Jeong, J. Cho, J. Kim*, SK hynix Semiconductor, Icheon, Korea

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Digital Accelerators and Circuit Techniques

Session Chair: *Mingoo Seok*, Columbia University, New York, NY

Session Co-Chair: *Kazuki Fukuoka*, Renesas Electronics, Tokyo, Japan

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29.1 **A 32.5mW Mixed-Signal Processing-in-Memory-Based k-SAT Solver in 65nm CMOS with 74.0% Solvability for 30-Variable 126-Clause 3-SAT Problems**

DS2

*D. Kim, N. Mizanur Rahman, S. Mukhopadhyay*, Georgia Institute of Technology, Atlanta, GA

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29.2 **Snap-SAT: A One-Shot Energy-Performance-Aware All-Digital Compute-in-Memory Solver for Large-Scale Hard Boolean Satisfiability Problems**

DS2

*S. Xie, M. Yang, S. A. Lanham, Y. Wang, M. Wang, S. Oruganti, J. P. Kulkarni*  
University of Texas, Austin, TX

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29.3 **A 8.09TOPS/W Neural Engine Leveraging Bit-Sparsified Sign-Magnitude Multiplications and Dual Adder Trees**

*H. An, Y. Chen, Z. Fan, Q. Zhang, P. Abillama, H-S. Kim, D. Blaauw, D. Sylvester*  
University of Michigan, Ann Arbor, MI

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29.4 **Wafer-Level Stacking of High-Density Capacitors to Enhance the Performance of a Large Multicore Processor for Machine Learning Applications**

*S. Felix<sup>1</sup>, S. Morton<sup>2</sup>, S. Stacey<sup>1</sup>, J. Walsh<sup>1</sup>*

<sup>1</sup>Graphcore, Bristol, United Kingdom; <sup>2</sup>Graphcore, Adelaide, Australia

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29.5 **A 73.53TOPS/W 14.74TOPS Heterogeneous RRAM In-Memory and SRAM Near-Memory SoC for Hybrid Frame and Event-Based Target Tracking**

DS2

*M. Chang<sup>\*1</sup>, A. S. Lele<sup>\*1</sup>, S. D. Spetalnick<sup>1</sup>, B. Crafton<sup>1</sup>, S. Konno<sup>1</sup>, Z. Wan<sup>1</sup>, A. Bhat<sup>1</sup>, W-S. Khwa<sup>2</sup>, Y-D. Chih<sup>3</sup>, M-F. Chang<sup>2</sup>, A. Raychowdhury<sup>1</sup>*

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<sup>3</sup>TSMC Design Technology, Hsinchu, Taiwan; <sup>\*</sup>Equally Credited Authors (ECAs)

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29.6 **A 1.5 $\mu$ W End-to-End Keyword Spotting SoC with Content-Adaptive Frame Sub-Sampling and Fast-Settling Analog Frontend**

*J-H. Seol<sup>1,2</sup>, H. Yang<sup>1</sup>, R. Rothe<sup>1</sup>, Z. Fan<sup>1</sup>, Q. Zhang<sup>1</sup>, H-S. Kim<sup>1</sup>, D. Blaauw<sup>1</sup>, D. Sylvester<sup>1</sup>*

<sup>1</sup>University of Michigan, Ann Arbor, MI; <sup>2</sup>Samsung Electronics, Hwasung, Korea

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29.7 **CCSA: A 394TOPS/W Mixed-Signal GPS Accelerator with Charge-Based Correlation Computing for Signal Acquisition**

*J. Li<sup>1</sup>, W. He<sup>1</sup>, B. Zhang<sup>2</sup>, L. Qi<sup>1</sup>, G. He<sup>1</sup>, M. Seok<sup>2</sup>*

<sup>1</sup>Shanghai Jiao Tong University, Shanghai, China; <sup>2</sup>Columbia University, New York, NY

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29.8 **A Sub-0.8pJ/b 16.3Gbps/mm<sup>2</sup> Universal Soft-Detection Decoder Using ORBGRAND in 40nm CMOS**

DS2

*A. Riaz<sup>1</sup>, A. Yasar<sup>1</sup>, F. Ercan<sup>1</sup>, W. An<sup>2</sup>, J. Ngo<sup>1</sup>, K. Galligan<sup>3</sup>, M. Medard<sup>2</sup>, K. R. Duffy<sup>3</sup>, R. T. Yazicigil<sup>1</sup>*

<sup>1</sup>Boston University, Boston, MA; <sup>2</sup>Massachusetts Institute of Technology, Cambridge, MA

<sup>3</sup>Maynooth University, Maynooth, Ireland

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29.9 **An 8T eNVS RAM Macro in 22nm FDSOI Standard Logic with Simultaneous Full-Array Data Restore for Secure IoT Devices**

*S. Nouri, S. S. Iyer*, University of California, Los Angeles, CA

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Power Management Techniques

Session Chair: *Xun Liu, The Chinese University of Hong Kong, Shenzhen, China*

Session Co-Chair: *Gael Pillonnet, CEA-Leti, Grenoble, France*

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30.1 **A Scalable N-Step Equal Split SSHI Piezoelectric Energy Harvesting Circuit Achieving 1170% Power Extraction Improvement and 22nA Quiescent Current with a 1μH-to-10μH Low Q Inductor**

*Y-W. Jeong, S-J. Lee, J-H. Kim, M-J. Cho, H-S. Kim, S-U. Shin*  
Ulsan National Institute of Science and Technology, Ulsan, Korea

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30.2 **A 93.2%-Efficiency Multi-Input Bipolar Energy Harvester with 17.9X MPPT Loss Reduction**

*Z-Y. Yang<sup>1</sup>, A. Chen<sup>1</sup>, C-W. Chen<sup>1</sup>, W-C. Hung<sup>1</sup>, K-H. Chen<sup>1</sup>, K-L. Zheng<sup>1,2</sup>, Y-H. Lin<sup>3</sup>, S-R. Lin<sup>3</sup>, T-Y. Tsa<sup>3</sup>*

<sup>1</sup>National Yang Ming Chiao Tung University, Hsinchu, Taiwan

<sup>2</sup>Chip-GaN Power Semiconductor, Hsinchu, Taiwan; <sup>3</sup>Realtek Semiconductor, Hsinchu, Taiwan

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30.3 **A Bias-Flip Rectifier with a Duty-Cycle-Based MPPT Algorithm for Piezoelectric Energy Harvesting with 98% Peak MPPT Efficiency and 738% Energy-Extraction Enhancement**

*X. Yue, S. Javvaji, Z. Tang, K. A. Makinwa, S. Du*; Delft University of Technology, Delft, The Netherlands

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30.4 **A 3.7V-to-1kV Chip-Cascaded Switched-Capacitor Converter with Auxiliary Boost Achieving >96% Reactive Power Efficiency for Electrostatic Drive Applications**

DS2

*Y. Li, B. Mabetha, J. T. Stauth*; Dartmouth College, Hanover, NH

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30.5 **A 95.3% 5V-to-32V Wide Range 3-Level Current Mode Boost Converter with Fully State-based Phase Selection Achieving Simultaneous High-Speed  $V_{CF}$  Balancing and Smooth Transition**

*S-J. Lee<sup>1</sup>, Y-W. Jeong<sup>1</sup>, M-J. Cho<sup>1</sup>, J-H. Kim<sup>1</sup>, H-S. Kim<sup>1</sup>, J-S. Bang<sup>2</sup>, S-U. Shin<sup>1</sup>*

<sup>1</sup>Ulsan National Institute of Science and Technology, Ulsan, Korea; <sup>2</sup>Samsung Electronics, Hwaseong, Korea

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30.6 **A 98.6%-Peak-Efficiency 1.47A/mm<sup>2</sup>-Current-Density Buck-Boost Converter with Always Reduced Conduction Loss**

*J. Jin<sup>1</sup>, Y. Zhou<sup>1</sup>, C. Chen<sup>1</sup>, X. Han<sup>1</sup>, W. Xu<sup>2</sup>, L. Cheng<sup>1,2</sup>*

<sup>1</sup>University of Science and Technology of China, Hefei, China; <sup>2</sup>Hefei CLT Microelectronics, Hefei, China

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30.7 **A Continuously Scalable-Conversion-Ratio SC Converter with Reconfigurable VCF Step for High Efficiency over an Extended VCR Range**

*Y. Wang<sup>1,2</sup>, M. Huang<sup>1</sup>, Y. Lu<sup>1</sup>, R. P. Martins<sup>1,3</sup>*

<sup>1</sup>University of Macau, Macau, China; <sup>2</sup>Zhuhai UM Science & Technology Research Institute, Zhuhai, China

<sup>3</sup>Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

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30.8 **3D Wireless Power Transfer with Noise Cancellation Technique for -62dB Noise Suppression and 90.1%-Efficiency**

*F. Huang<sup>1</sup>, H-Y. Tsai<sup>1</sup>, C-Y. Huang<sup>1</sup>, Y-C. Luo<sup>1</sup>, C-H. Li<sup>1</sup>, S-C. Huang<sup>1</sup>, Y-H. Kao<sup>1</sup>, K-H. Chen<sup>1</sup>, K-L. Zheng<sup>1,2</sup>, Y-H. Lin<sup>3</sup>, S-R. Lin<sup>3</sup>, T-Y. Tsa<sup>3</sup>*

<sup>1</sup>National Yang Ming Chiao Tung University, Hsinchu, Taiwan

<sup>2</sup>Chip-GaN Power Semiconductor, Hsinchu, Taiwan; <sup>3</sup>Realtek Semiconductor, Hsinchu, Taiwan

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30.9 **A 90%-Efficiency 40.68MHz Single-Stage Dual-Output Regulating Rectifier with ZVS and Synchronous PFM Control for Wireless Powering**

*Z. Luo, J. Liu, H. Lee*, University of Texas at Dallas, Richardson, TX

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30.10 **Single Chip, Qi Compliant, 40W Wireless Power Transmission Controller using RMS Coil Current Sensing and Adaptive ZVS for 4dB EMI and up to 1.7% Efficiency Improvements**

DS2

*F. Neri<sup>1</sup>, G. Mehas<sup>2</sup>, F. Di Fazio<sup>1</sup>, G. Figliozzi<sup>1</sup>, J. Menart<sup>1</sup>, M. Augustyniak<sup>1</sup>, T. Aca<sup>2</sup>, A. Bavis<sup>2</sup>*

<sup>1</sup>Renesas Electronics, Zürich, Switzerland; <sup>2</sup>Renesas Electronics, San Jose, CA

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Energy-Efficient Radios for UWB, BMI, and IoT Systems

Session Chair: *Negar Reiskarimian, Massachusetts Institute of Technology, Cambridge, MA*

Session Co-Chair: *Jan Prummel, Renesas Electronics, s-Hertogenbosch, The Netherlands*

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31.1 A Quadrature Uncertain-IF IR-UWB Transceiver with Twin-OOK Modulation

*B. Wang, W. Rhee, Z. Wang*

Tsinghua University, Beijing, China

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31.2 A Fully Integrated IEEE 802.15.4/4z-Compliant 6.5-to-8GHz UWB System-on-Chip RF Transceiver Supporting Precision Positioning in a CMOS 28nm Process

*W. Kim<sup>1</sup>, H-G. Seok<sup>1</sup>, G. Lee<sup>1</sup>, S. Kim<sup>1</sup>, J-K. Lee<sup>1</sup>, C. Kim<sup>1</sup>, W. Kim<sup>1</sup>, W. Jung<sup>1</sup>, Y. Cho<sup>1</sup>, S. Bae<sup>1</sup>, J. Cho<sup>1</sup>, H. Na<sup>1</sup>, B. Kang<sup>1</sup>, H. Han<sup>1</sup>, H. Son<sup>1</sup>, C. Ahn<sup>1</sup>, H. Kang<sup>1</sup>, S. Jung<sup>1</sup>, H. Sung<sup>1</sup>, Y. Kim<sup>1</sup>, D. Kim<sup>1</sup>, D. Kim<sup>1</sup>, J-S. Paek<sup>1,2</sup>, S. Oh<sup>1</sup>, J. Lee<sup>1</sup>, S. Kwak<sup>1</sup>, J. Kim<sup>1</sup>*

<sup>1</sup>Samsung Electronics, Hwaseong, Korea

<sup>2</sup>now at Pusan National University, Pusan, Korea

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31.3 A 1.8Gb/s, 2.3pJ/bit, Crystal-Less IR-UWB Transmitter for Neural Implants

*J. Lei<sup>1</sup>, X. Liu<sup>2</sup>, W. Song<sup>1</sup>, H. Huang<sup>1</sup>, X. Ma<sup>2</sup>, J. We<sup>2</sup>, M. Zhang<sup>1</sup>*

<sup>1</sup>Tsinghua University, Beijing, China

<sup>2</sup>Beijing Ningju Technology, Beijing, China

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31.4 A 128-Channel 2mmx2mm Battery-Free Neural Dielet Merging Simultaneous Multi-Channel Transmission Through Multi-Carrier Orthogonal Backscatter

*C. Yang, Z. Zhang, L. Zhang, Y. Zhang, Z. Li, Y. Luo, G. Pan, B. Zhao*

Zhejiang University, Hangzhou, China

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31.5 A Passive Bidirectional BLE Tag Demonstrating Battery-Free Communication in DS2 Tablet/Smartphone-to-Tag, Tag-to-Tablet/Smartphone, and Tag-to-Tag Modes

*Z. Chang<sup>\*1</sup>, Q. Xiao<sup>\*1,2</sup>, W. Wang<sup>1,2</sup>, Y. Luo<sup>1</sup>, B. Zhao<sup>1</sup>*

<sup>1</sup>Zhejiang University, Hangzhou, China

<sup>2</sup>Microaiot, Hangzhou, China

<sup>\*</sup>Equally Credited Authors (ECAs)

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31.6 A ULP Long-Range Active-RF Tag with Automatic Antenna-Interface Calibration Achieving 20.5% TX Efficiency at -22dBm EIRP, and -60.4dBm Sensitivity at 17.8nW RX Power

*Z. Yang<sup>1</sup>, J. Yin<sup>1</sup>, W-H. Yu<sup>1</sup>, H. Zhang<sup>1</sup>, P-I. Mak<sup>1</sup>, R. P. Martins<sup>1,2</sup>*

<sup>1</sup>University of Macau, Macau, China

<sup>2</sup>Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

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31.7 A 0.7-to-2.5GHz Sliding Digital-IF Quadrature Digital Transmitter Achieving >40% System Efficiency for Multi-Mode NB-IoT/BLE Applications

*C. Hu, D. Zheng, Y. Yin, J. Lin, Y. Li, W. Li, H. Xu*

Fudan University, Shanghai, China

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31.8 A 0.4-to-0.95GHz Distributed N-Path Noise-Cancelling Ultra-Low-Power RX with Integrated Passives Achieving -85dBm/100kb/s Sensitivity, -41dB SIR and 174dB RX FoM in 22nm CMOS

*H. Bialek, M. Johnston, A. Natarajan*

Oregon State University, Corvallis, OR

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Intelligent Biomedical Circuits and Systems

Session Chair: *Jun-Chau Chien*, National Taiwan University, Taipei, Taiwan

Session Co-Chair: *Mahsa Shooran*, EPFL, Geneva, Switzerland

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**32.1 A Behind-The-Ear Patch-Type Mental Healthcare Integrated Interface with 275-Fold Input Impedance Boosting and Adaptive Multimodal Compensation Capabilities**

DS2

*H. Kim<sup>1</sup>, M. Kim<sup>1</sup>, K. Lee<sup>2</sup>, S. Cho<sup>1</sup>, C. S. Park<sup>1</sup>, S. Song<sup>3</sup>, D. S. Keum<sup>4</sup>, D. P. Jang<sup>3</sup>, J. J. Kim<sup>1</sup>*

<sup>1</sup>Ulsan National Institute of Science and Technology, Ulsan, Korea

<sup>2</sup>Samsung Electronics, Hwaseong, Korea

<sup>3</sup>Hanyang University, Seoul, Korea

<sup>4</sup>SOSO H&C, Daegu, Korea

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**32.2 A Stimulus-Scattering-Free Pixel-Sharing Sub-Retinal Prosthesis SoC with 35.8dB Dynamic Range Time-Based Photodiode Sensing and Per-Pixel Dynamic Voltage Scaling**

DS2

*K. Eom<sup>1</sup>, M. Park<sup>1</sup>, H-S. Lee<sup>1</sup>, S-B. Ku<sup>1</sup>, N. Kim<sup>2</sup>, S. Cha<sup>3</sup>, Y. S. Goo<sup>3</sup>, S. Kim<sup>2</sup>, S-W. Kim<sup>4</sup>, H-M. Lee<sup>1</sup>*

<sup>1</sup>Korea University, Seoul, Korea

<sup>2</sup>Daegu Gyeongbuk Institute of Science and Technology, Daegu, Korea

<sup>3</sup>Chungbuk National University, Cheongju, Korea

<sup>4</sup>Korea University Guro Hospital, Seoul, Korea

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**32.3 A 1V 136.6dB-DR 4kHz-BW  $\Delta\Sigma$  Current-to-Digital Converter with a Truncation-Noise-Shaped Baseline-Servo-Loop in 0.18 $\mu$ m CMOS**

*T. Seol, S. Lee, G. Kim, S. Kim, E. Kim, S. Baik, J. Kung, J-W. Choi, A. K. George, J. Lee*

Daegu Gyeongbuk Institute of Science and Technology, Daegu, Korea

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**32.4 A 1V-Supply 1.85V<sub>pp</sub>-Input-Range 1kHz-BW 181.9dB-FOM<sub>DR</sub> 179.4dB-FOM<sub>SNDR</sub> 2<sup>nd</sup>-Order Noise-Shaping SAR-ADC with Enhanced Input Impedance in 0.18 $\mu$ m CMOS**

*G. Kim, S. Lee, T. Seol, S. Baik, Y. Shin, G. Kim, J-H. Yoon, A. K. George, J. Lee*

Daegu Gyeongbuk Institute of Science and Technology, Daegu, Korea

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**32.5 A 384-Channel Online-Spike-Sorting IC Using Unsupervised Geo-OSort Clustering and Achieving 0.0013mm<sup>2</sup>/Ch and 1.78 $\mu$ W/Ch**

*Y. Chen<sup>1,2</sup>, B. Tacca<sup>1</sup>, Y. Chen<sup>1</sup>, D. Biswas<sup>1</sup>, G. Gielen<sup>1,3</sup>, F. Catthoor<sup>1,3</sup>, M. Verhelst<sup>1,3</sup>, C. Mora Lopez<sup>1</sup>*

<sup>1</sup>imec, Leuven, Belgium

<sup>2</sup>Fudan University, Shanghai, China

<sup>3</sup>KU Leuven, Leuven, Belgium

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**32.6 SciCNN: A 0-Shot-Retraining Patient-Independent Epilepsy-Tracking SoC**

DS2

*C-W. Tsai<sup>1,2</sup>, R. Jiang<sup>1</sup>, L. Zhang<sup>1,3</sup>, M. Zhang<sup>1,4</sup>, L. Wu<sup>1</sup>, J. Guo<sup>1</sup>, Z. Yan<sup>1</sup>, J. Yoo<sup>1,2</sup>*

<sup>1</sup>National University of Singapore, Singapore, Singapore

<sup>2</sup>The N.1 Institute for Health, Singapore, Singapore

<sup>3</sup>Apple, Cupertino, CA

<sup>4</sup>Huawei Technologies, Chengdu, China

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**32.7 Fascicle-Selective Bidirectional Peripheral Nerve Interface IC with 173dB FOM Noise-Shaping SAR ADCs and 1.38pJ/b Frequency-Multiplying Current-Ripple Radio Transmitter**

*J. Xu, J. Sales Filho, S. Nag, L. Long, C. Tejeiro, E. Hwang, G. O'Leary, Y. Huang, M. Kanchwala, M. Abdolrazzaghi, C. Tang, P. Liu, Y. Sui, X. Liu, G. Eleftheriades, J. Zariffa, R. Genov*

University of Toronto, Toronto, Canada

Conclusion 5:15 PM

Non-Volatile Memory and Compute-In-Memory

Session Chair: *Hidehiro Shiga*, KIOXIA, Yokohama, Japan

Session Co-Chair: *Takashi Ito*, Renesas, Kodaira-shi, Tokyo, Japan

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- 33.1 A 16nm 32Mb Embedded STT-MRAM with a 6ns Read Access Time, 1M-Cycle Write Endurance, 20-Year Retention at 150°C and MTJ-OTP Solutions for Magnetic Immunity**  
*P-H. Lee, C-F. Lee, Y-C. Shih, H-J. Lin, Y-A. Chang, C-H. Lu, Y-L. Chen, C-P. Lo, C-C. Chen, C-H. Kuo, T-L. Chou, C-Y. Wang, J. Wu, R. Wang, H. Chuang, Y. Wang, Y-D. Chih, T-Y. J. Chang*  
TSMC, Hsinchu, Taiwan

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- 33.2 A 22nm 8Mb 46.4-160.1-TOPS/W STT-MRAM Near-Memory-Computing Macro with 8b Precision for AI-Edge Devices**  
*Y-C. Chiu<sup>\*1</sup>, W-S. Khwa<sup>\*2</sup>, C-Y. Li<sup>1</sup>, F-L. Hsieh<sup>1</sup>, Y-A. Chien<sup>1</sup>, G-Y. Lin<sup>1</sup>, P-J. Chen<sup>1</sup>, T-H. Pan<sup>1</sup>, D-Q. You<sup>1</sup>, F-Y. Chen<sup>1</sup>, A. Lee<sup>1</sup>, C-C. Lo<sup>1</sup>, R-S. Liu<sup>1</sup>, C-C. Hsieh<sup>1</sup>, K-T. Tang<sup>1</sup>, Y-D. Chih<sup>3</sup>, T-Y. Chang<sup>3</sup>, M-F. Chang<sup>1,2</sup>*  
<sup>1</sup>National Tsing Hua University, Hsinchu, Taiwan  
<sup>2</sup>TSMC Corporate Research, Hsinchu, Taiwan  
<sup>3</sup>TSMC, Hsinchu, Taiwan  
<sup>\*</sup>Equally Credited Authors (ECAs)

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- 33.3 A 9Mb HZO-Based Embedded FeRAM Macro with a 1012-Cycle Endurance, a 5ns Read and a 7ns Write Time using ECC-Assisted Data Refresh and an Offset-Canceled Sense Amplifier**  
*J. Yang<sup>1</sup>, Q. Luo<sup>1</sup>, X. Xue<sup>2</sup>, H. Jiang<sup>3</sup>, Q. Wu<sup>2</sup>, Z. Han<sup>1</sup>, Y. Cao<sup>3</sup>, Y. Han<sup>3</sup>, C. Dou<sup>1</sup>, H. Lv<sup>1</sup>, Q. Liu<sup>2</sup>, M. Liu<sup>1,2</sup>*  
<sup>1</sup>Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China  
<sup>2</sup>Fudan University, Shanghai, China  
<sup>3</sup>Zhejiang Lab, Hangzhou, China

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- 33.4 A 28nm 2Mb 22.4-41.5TOPS/W STT-MRAM Computing-in-Memory Macro with a Refined Bit Cell for AI Inference**  
*H. Cai<sup>1</sup>, Z. Bian<sup>1</sup>, Y. Hou<sup>1</sup>, Y. Zhou<sup>1</sup>, J-L. Cui<sup>1</sup>, Y. Guo<sup>1</sup>, X. Tian<sup>1</sup>, B. Liu<sup>1</sup>, X. Si<sup>1</sup>, Z. Wang<sup>2</sup>, J. Yang<sup>1</sup>, W. Shan<sup>1</sup>*  
<sup>1</sup>Southeast University, Nanjing, China  
<sup>2</sup>Nanjing Prochip Electronic Technology, Nanjing, China

Break 3:00 PM



Cryo-CMOS for Quantum Computing

Session Chair: *Fabio Sebastiano*, Delft University of Technology, Delft, The Netherlands

Session Co-Chair: *Giorgio Ferrari*, Politecnico di Milano, Milano, Italy

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**34.1 THz Cryo-CMOS Backscatter Transceiver: A Contactless 4 Kelvin-300 Kelvin Data Interface**

DS2

*J. Wang, M. I. Ibrahim, I. B. Harris, N. M. Monroe, M. I. W. Khan, X. Yi, D. R. Englund, R. Han*  
Massachusetts Institute of Technology, Cambridge, MA

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**34.2 A 28nm Bulk-CMOS IC for Full Control of a Superconducting Quantum Processor Unit-Cell**

*J. Yoo<sup>1</sup>, Z. Chen<sup>1</sup>, F. Arute<sup>1</sup>, S. Montazeri<sup>1</sup>, M. Szalay<sup>1</sup>, C. Erickson<sup>1</sup>, E. Jeffrey<sup>1</sup>, R. Fatemi<sup>1</sup>, M. Giustina<sup>1</sup>, M. Ansmann<sup>1</sup>, E. Lucero<sup>1</sup>, J. Kelly<sup>1</sup>, J. C. Bardin<sup>1,2</sup>*

<sup>1</sup>Google Quantum AI, Goleta, CA; <sup>2</sup>University of Massachusetts, Amherst, MA

4:15 PM

**34.3 A Polar-Modulation Based Cryogenic Qubit State Controller in 28nm Bulk CMOS**

*Y. Guo<sup>1,2</sup>, Y. Li<sup>1</sup>, W. Huang<sup>1</sup>, S. Tan<sup>1</sup>, Q. Liu<sup>3</sup>, T. Li<sup>1,3</sup>, N. Deng<sup>1</sup>, Z. Wang<sup>1</sup>, Y. Zheng<sup>2</sup>, H. Jiang<sup>1</sup>*

<sup>1</sup>Tsinghua University, Beijing, China

<sup>2</sup>Nanyang Technological University, Singapore, Singapore

<sup>3</sup>Beijing Academy of Quantum Information Sciences, Beijing, China

4:45 PM

**34.4 A Cryogenic Controller IC for Superconducting Qubits with DRAG Pulse Generation by Direct Synthesis without Using Memory**

*K. Kang, D. Minn, J. Lee, H-J. Song, M. Lee, J-Y. Sim*

Pohang University of Science and Technology, Pohang, Korea

5:00 PM

**34.5 A Calibration-Free 12.8-16.5GHz Cryogenic CMOS VCO with 202dBc/Hz FoM for Classic-Quantum Interface**

*G. Zhang<sup>1</sup>, H. Lin<sup>2</sup>, C. Wang<sup>1</sup>*

<sup>1</sup>University of Electronic Science and Technology of China, Chengdu, China

<sup>2</sup>Chengdu Data Automation System Technologies, Chengdu, China

Conclusion 5:15 PM

## Principles of Quantum Computing and the Application of Cryoelectronics to Qubit Control and Readout

|                 |   |
|-----------------|---|
| <b>Time:</b>    | <b>Topic:</b>   |
| 8:00 AM         | Breakfast   |
| 8:25 AM         | Introduction by Chair, <b>Daniel Friedman</b><br><i>IBM Thomas J. Watson Research Center, Yorktown Heights, NY</i>  |
| <b>8:30 AM</b>  | <b>Introduction to Quantum Computing: Qubits, Gates, and Algorithms</b><br><b>William Oliver</b> , <i>Massachusetts Institute of Technology, Cambridge, MA</i>  |
| 10:00 AM        | Break   |
| <b>10:30 AM</b> | <b>Spin Qubits: Principles, Control/Readout Architectures, and Cryoelectronic Solutions</b><br><b>Sushil Subramanian</b> , <i>Intel, Hillsboro, OR</i>  |
| 12:15 PM        | Lunch   |
| <b>1:20 PM</b>  | <b>Superconducting Qubits: Principles, Control/Readout Architectures, and Cryoelectronic Solutions</b><br><b>David Frank</b> , <i>IBM, Yorktown Heights, NY</i>   |
| 2:50 PM         | Break   |
| <b>3:20 PM</b>  | <b>Cryoelectronics for Quantum Computing: Technology, Circuit Design, and Future Directions</b><br><b>Joseph Bardin</b> , <i>University of Massachusetts Amherst, Amherst, MA &amp; Google Quantum AI, Goleta, CA</i> |
| 4:50 PM         | Conclusion  |

### Introduction

Quantum computing is a paradigm that has the potential to transform problems that are computationally intractable today into solvable problems in the future. Significant advances in the last decade have demonstrated that quantum computers can be implemented, and further that the goal of demonstrating true performance advantages over traditional computing techniques on one or more problems with commercial value may be achieved in the not-so-distant future. Yet there remain many fundamental questions to be answered on the road to realizing a broad class of quantum computing systems, questions that span the entire range from devices to control electronics to systems design to algorithms. In this short course, we will first provide an introduction to quantum computing, including fundamentals of qubits, quantum gates, quantum circuits, and quantum algorithms. In the second and third talks, we will present approaches to using CMOS circuits at cryogenic temperatures to interact with spin qubits and superconducting qubits, respectively. In the final talk, we will describe approaches to technology/circuit co-design and co-optimization in the design of cryogenic circuits for quantum computing applications, and will then look forward toward future directions and challenges for quantum computing scaled system implementations.

### SC1:

#### Introduction to Quantum Computing: Qubits, Gates, and Algorithms

**William Oliver**, *Massachusetts Institute of Technology, Cambridge, MA*

Quantum computers are fundamentally different from conventional computers. They promise to address problems that are practically prohibitive and even impossible to solve using today's supercomputers. The challenge is building one that is large enough to be useful. In this short course, we will introduce quantum computing with a focus on the qubit modalities, single-qubit and two-qubit gates, and their use in quantum algorithms and error mitigation.

**William D. Oliver** is appointed Henry Ellis Warren (1894) Professor of Electrical Engineering and Computer Science, Professor of Physics, and Lincoln Laboratory Fellow at the Massachusetts Institute of Technology. He serves as the inaugural Director of the MIT Center for Quantum Engineering and as Associate Director of the MIT Research Laboratory of Electronics. Will's research interests and expertise include the materials, fabrication, design, and implementation of superconducting qubit processors, as well as the development of cryogenic packaging and control electronics for extensible quantum computing applications. He received his PhD in Electrical Engineering from Stanford University in 2003.

**SC2:****Spin Qubits:****Principles, Control/Readout Architectures, and Cryoelectronic Solutions***Sushil Subramanian, Intel, Hillsboro, OR*

Quantum computing offers a potential solution for problems intractable by classical computing. A large number of qubits, the fundamental units of quantum information, have to be controlled precisely for implementing practical applications, thereby posing challenging scalability requirements on all layers of the quantum computing stack. Spin qubits present a scalable solution at the device level due to their ease of integration and compatibility with standard semiconductor manufacturing. In this talk, we will explore spin-qubit physics and operation and discuss methods for spin-qubit control and readout. We will then introduce integrated cryo-CMOS for scalable control and present details of recent advances in qubit-controller SOC's.

**Sushil Subramanian** received the B.Tech. degree in electronics and electrical communication engineering from Indian Institute of Technology, Kharagpur, India, in 2009, and the M.S. and Ph.D. degrees in electrical engineering from the University of Southern California, Los Angeles, CA, in 2017, where he worked on fast-hopping frequency synthesizers and interference tolerant receivers. He is currently with Intel Labs, Intel Corporation, Hillsboro, OR, where he works on integrated circuits and systems for qubit control in quantum computers.

**SC3:****Superconducting Qubits:****Principles, Control/Readout Architectures, and Cryoelectronic Solutions***David Frank, IBM, Yorktown Heights, NY*

Superconducting qubits such as transmons are one of the most well-developed classes of quantum devices for building a quantum computer. We will describe the fabrication and operating principles of such qubits and discuss the requirements for their control and read-out electronics. In particular, the use of cryogenic CMOS circuits operating at 4 K is a promising approach to obtaining high-quality qubit control with reduced system complexity, and we will discuss the design and operation of such circuits.

**David Frank** received his B.S. from Caltech in 1977 and a Ph.D. in physics from Harvard University in 1983. He is a Research Staff Member at the IBM T. J. Watson Research Center. His studies have included III-V FETs, exploring the limits of scaling of silicon technology, and quantum computing. His recent work includes exploring uses of CMOS in quantum computing and concepts in quantum error correction. He has also worked on telegraph noise in nanoscale FETs, the modeling of innovative Si devices, low-power circuit design, and the analysis of CMOS scaling. Dr. Frank is an IEEE Fellow and was a co-recipient of the 2011 IEEE Cleo Brunetti award. He has authored or co-authored over 130 technical publications and holds 23 U.S. patents.

**SC4:****Cryoelectronics for Quantum Computing:  
Technology, Circuit Design, and Future Directions***Joseph Bardin, University of Massachusetts Amherst, Amherst, MA & Google Quantum AI, Goleta, CA*

In this talk, we give an overview of emerging IC technology for the readout and control of superconducting quantum processors. After a brief introduction, the talk will describe the prospect of using SiGe HBT-based LNAs for qubit readout, including a discussion of technology optimization for reducing noise. We then will discuss control ICs, including experimental challenges and characterization techniques using quantum control experiments. The talk will end with a discussion of open challenges.

**Joseph Bardin** is a Professor of ECE at UMass Amherst and a Research Scientist with the Google Quantum AI team. At UMass, he leads research in the area of low-temperature integrated circuits, with applications in radio astronomy and the quantum information sciences. At Google, he leads the team working on the development of integrated circuits for large-scale quantum computers.

Advancing Technologies for Extended Reality (XR)  
to Make the “Metaverse” Possible

- Organizers:** **Huichu Liu**, *Meta Agile Silicon Team, Menlo Park, CA*  
**Visvesh Sathe**, *Georgia Institute of Technology, Atlanta, GA*
- Committee:** **Kaushik Sengupta**, *Princeton University, Princeton, NJ*  
**Firooz Aflatouni**, *University of Pennsylvania, Philadelphia, PA*  
**Matteo Bassi**, *Infineon Technologies, Villach, Austria*  
**Sugako Otani**, *Renesas Electronics, Tokyo, Japan*
- Champions:** **Vivek De**, *Intel, Hillsboro, OR*  
**Makoto Nagata**, *Kobe University, Kobe, Japan*

Devices for “eXtended Reality” (XR), consisting of augmented (AR), virtual (VR) and mixed realities (MR), represent the next leap in human-computer interactions. Since XR systems include complex interactions between many sensors, processing and display while maintaining weight, form factor and battery constraints, advancing these technologies requires overcoming formidable barriers in multiple areas: computing, display technologies, low-power sensor, camera and telemetry for gesture recognition, thermal management, and packaging. In addition, these XR devices implement advanced machine-learning algorithms and rely on circuit, system, and software co-design to enable the desired immersive experience. This forum provides an overview of the key challenges and opportunities in the hardware design for XR devices and explores the necessary technology advancements to make the “Metaverse” possible.

Agenda

| Time     | Topic   |
|----------|---|
| 8:00 AM  | Breakfast   |
| 8:15 AM  | <b>Introduction</b><br><b>Huichu Liu</b> , <i>Meta Agile Silicon Team, Menlo Park, CA</i>   |
| 8:25 AM  | <b>Overview of Augmented Reality and Virtual Reality Applications, Silicon Challenges and Research Directions</b><br><b>Edith Beigné</b> , <i>Meta Platforms, Menlo Park, CA</i>  |
| 9:15 AM  | <b>Extended Reality: An End-to-End Systems View</b><br><b>Sarita Adve</b> , <i>University of Illinois at Urbana-Champaign, IL</i>   |
| 10:05 AM | Break   |
| 10:20 AM | <b>XR SoC Design and Implementation</b><br><b>Sungcheol Park</b> , <i>Samsung Electronics, Hwaseong, Korea</i>  |
| 11:10 AM | <b>Silicon Photonics: Augmented Reality and Beyond</b><br><b>Jelena Notaros</b> , <i>MIT, Boston, MA</i>  |
| 12:00 PM | Lunch   |
| 1:20 PM  | <b>mm-Wave Integrated Systems for High-Precision Sensing and Recognition in XR Devices</b><br><b>Vadim Issakov</b> , <i>Technische Universität Braunschweig, Braunschweig, Germany &amp; Infineon Technologies, Munich, Germany</i> |
| 2:10 PM  | <b>TinyML: Why it is Essential for Metaverse</b><br><b>Evgeni Gousev</b> , <i>Qualcomm, San Diego, CA</i>   |
| 3:00 PM  | Break   |
| 3:15 PM  | <b>XR Challenges and Success Factors</b><br><b>Johan Johansson</b> , <i>MediaTek, Stockholm, Sweden</i>   |
| 4:05 PM  | <b>Compact and Energy Efficient Packaging for XR Hardware</b><br><b>Kuo-Chung Yee</b> , <i>TSMC, Hsinchu, Taiwan</i>  |
| 4:55 PM  | Closing Remarks   |

Extreme Data Converters and Their Peripherals

- Organizer:** Jongwoo Lee, Samsung Electronics, Hwasung, Korea
- Committee:** Nan Sun, Tsinghua University, Beijing, China  
Nima Maghari, University of Florida, Gainesville, FL  
Dominique Morche, Département Architecture Conception et Logiciel Embarqué (DACLE), CEA-Leti, Grenoble, France  
Man-Kay Law, University of Macau, Taipa, Macau, China
- Champion:** Kostas Doris, NXP, Eindhoven, The Netherlands
- Moderator:** Kostas Doris, NXP, Eindhoven, The Netherlands

Data converters have undergone significant advances over the past decade. Their performance and application spaces have been greatly expanded. Nowadays, data converters can sample beyond 100GS/s, consume only several nW of power, and achieve an energy-efficiency approaching the theoretical limit. This forum will discuss design techniques that are pushing the data-converter applications into previously uncharted territories, including extremely high speed, high precision, and energy efficiency. In addition to the converters, the peripheral circuits, such as time and voltage references and driving amplifiers, are taking the spotlight in this forum.

Agenda

| Time     | Topic   |
|----------|---|
| 8:00 AM  | Breakfast   |
| 8:15 AM  | <b>Introduction</b><br>Jongwoo Lee, Samsung Electronics, Hwasung, Korea   |
| 8:25 AM  | <b>The Post-FoM Era of ADC: What Else Matters When Quantization is ‘Free’?</b><br>Matt Straayer, AMD, Buxborough, MA                                  |
| 9:15 AM  | <b>Design Techniques for Energy-Efficient Analog-to-Digital Converters</b><br>Youngchel Chae, Yonsei University, Seoul, Korea                         |
| 10:05 AM | Break   |
| 10:20 AM | <b>Continuous-Time Pipelined ADC: A Breed of Continuous-Time ADCs for Ultra-Wideband Conversion</b><br>Hajime Shibata, ADI, Toronto, Canada           |
| 11:10 AM | <b>Precision High Speed Converters</b><br>Sandeep Oswal, TI, Bengaluru, India   |
| 12:00 PM | Lunch   |
| 1:20 PM  | <b>High-Speed and High-Performance Continuous-Time Delta-Sigma ADCs</b><br>Lucien Breems, NXP, Eindhoven, The Netherlands                             |
| 2:10 PM  | <b>High Performance ADC Design in High-Speed Wireline Transceivers and 5G Wireless Transceivers</b><br>Ben Rhew, Samsung Electronics, Hwaseong, Korea |
| 3:00 PM  | Break   |
| 3:15 PM  | <b>Extremely Compact Data Converters for Future 3D Sensing</b><br>Satoshi Kondo, Toshiba, Kawasaki, Japan   |
| 4:05 PM  | <b>Panel Discussion</b><br>Moderator: Kostas Doris, NXP, Eindhoven, The Netherlands   |
| 4:55 PM  | Closing Remarks   |

The Future of Heterogeneous Multi-Core Architectures for AI and Other Specialized Processing

- Organizer:** Jun Deguchi, *Kioxia, Kawasaki, Japan*
- Committee:** Soojung Ryu, *Sapeon, Seongnam, Korea*  
Marian Verhelst, *KU Leuven, Heverlee, Belgium*  
Eric Wang, *TSMC, Hsinchu, Taiwan*  
Ru Huang, *Peking University, Beijing, China*  
Harish Krishnamurthy, *Intel, Hillsboro, OR*  
Ingrid Verbauwhede, *KU Leuven, Leuven, Belgium*
- Champions:** Fatih Hamzaoglu, *Intel, Hillsboro, OR*  
Yan Li, *Western Digital, Milpitas, CA*

The field of processor SoC design is increasingly moving to heterogeneous architectures, in which different processor types are combined in the same processing system. These processors range from various CPUs (power-efficient and high-performance cores) to GPUs, NPU's and ISP's. The trend towards increased heterogeneity is not yet saturated. Will we see even more heterogeneous systems in the future? What processor combinations are optimal for different target devices? What accelerators will we see added in the future? And how can such heterogeneous processing cores efficiently share data when the number of cores keeps going up, and still ensure coherency? With the introduction of chiplets, how can the benefits of heterogeneous multi-core architectures be expanded? This forum will bring together experts on multi-core processing systems and processor specialization to consider the future of heterogeneous many-core compute systems.

Agenda

| Time     | Topic  |
|----------|--|
| 8:00 AM  | Breakfast  |
| 8:15 AM  | <b>Introduction</b><br>Jun Deguchi, <i>Kioxia, Kawasaki, Japan</i>   |
| 8:25 AM  | <b>Scaling AI Computing Sustainably</b><br>Carole-Jean Wu, <i>Meta, Cambridge, MA</i>  |
| 9:15 AM  | <b>AI Accelerators: A Trade-off in Performance, Energy Efficiency, Flexibility, and Design Complexity</b><br>Michaela Blott, <i>AMD, Dublin, Ireland</i>   |
| 10:05 AM | Break  |
| 10:20 AM | <b>The Era of Domain-Specific Architecture: Heterogeneous NPU Cores in a Mobile SoC</b><br>Jun-Seok Park, <i>Samsung Electronics, Hwaseong, Korea</i>  |
| 11:10 AM | <b>Is an AI Accelerator All You Need? Overcoming Amdahl's Law with Tightly-Coupled Heterogeneous Accelerators</b><br>Angelo Garofalo, <i>ETH Zurich, Zurich, Switzerland</i>                                     |
| 12:00 PM | Lunch  |
| 1:20 PM  | <b>Meeting Future Performance Demands Through Packaging</b><br>Bryan Black, <i>Chipletz, Austin, TX</i>  |
| 2:10 PM  | <b>Co-Design of Programmable Hardware Accelerators and Compilers for Future Heterogeneous Computing Systems</b><br>Priyanka Raina, <i>Stanford University, Stanford, CA</i>                                      |
| 3:00 PM  | Break  |
| 3:15 PM  | <b>Universal Chiplet Interconnect Express (UCIe)<sup>TM</sup>: An Open Industry-Standard Chiplet Interconnect for Next-Generation Systems on a Package</b><br>Debendra Das Sharma, <i>Intel, Santa Clara, CA</i> |
| 4:05 PM  | <b>Memory Systems for AI Computers</b><br>Simon Knowles, <i>Graphcore, Bristol, United Kingdom</i>   |
| 4:55 PM  | Closing Remarks  |

Advanced Circuits and Technologies  
for Wearable and Implantable Devices

- Organizer:** **Sohmyung Ha**, *New York University Abu Dhabi, United Arab Emirates*
- Committee:** **Jiawei Xu**, *Fudan University, Shanghai, China*  
**Qinwen Fan**, *Delft University of Technology, Delft, The Netherlands*  
**Yan Lu**, *University of Macau, Taipa, Macao, China*  
**Mehdi Kiani**, *The Pennsylvania State University, University Park, PA*
- Champions:** **Makoto Ikeda**, *University of Tokyo, Tokyo, Japan*  
**Arun Natarajan**, *Oregon State University, Corvallis, OR*

Over the past decades, we have witnessed remarkable advances in wearable and implantable devices for diagnosing and treating a wide range of diseases and for vigilant healthcare monitoring. This forum will be a great venue to learn and discuss recent advances in system-level architectures, circuit techniques, and emerging technologies for various wearable and implantable applications. Presentations will include discussions of sensors, interface circuits, on-chip signal processing, powering, and communication for wearable and implantable devices.

Agenda

| <u>Time</u> | <u>Topic</u>  |
|-------------|---|
| 8:00 AM     | Breakfast   |
| 8:15 AM     | <b>Introduction</b><br><b>Sohmyung Ha</b> , <i>New York University Abu Dhabi, United Arab Emirates</i>  |
| 8:25 AM     | <b>Biopotential Sensing in Consumer Wearables</b><br><b>Yun-Shiang Shu</b> , <i>MediaTek, Hsinchu, Taiwan</i>   |
| 9:15 AM     | <b>Skin-Interfaced Wearable Electrochemical Biosensors</b><br><b>Wei Gao</b> , <i>California Institute of Technology, Pasadena, CA</i>                              |
| 10:05 AM    | Break   |
| 10:20 AM    | <b>Flexible and Integrated Power Sources for Wearable Devices</b><br><b>Ana Arias</b> , <i>University of California, Berkeley, CA</i>                               |
| 11:10 AM    | <b>Secure and Efficient Internet of Bodies (IoB) using Body as a ‘Wire’</b><br><b>Shreyas Sen</b> , <i>Purdue University, West Lafayette, IN</i>                    |
| 12:00 PM    | Lunch   |
| 1:20 PM     | <b>Hybrid Implantable Neural Systems: From Soft, Biomimetic Devices to Translational Interfaces</b><br><b>Stéphanie Lacour</b> , <i>EPFL, Lausanne, Switzerland</i> |
| 2:10 PM     | <b>Bioelectronics - Where Technology Meets Biology</b><br><b>Refet Firat Yazicioglu</b> , <i>Galvani Bioelectronics, London, United Kingdom</i>                     |
| 3:00 PM     | Break   |
| 3:15 PM     | <b>Towards Battery-Free Millimeter-Sized Bioelectronic Implants</b><br><b>Kaiyuan Yang</b> , <i>Rice University, Houston, TX</i>                                    |
| 4:05 PM     | <b>Neuron-Inspired Wireless Telemetry for Implantable Neural Interfaces</b><br><b>Yao-Hong Liu</b> , <i>imec, Eindhoven, The Netherlands</i>                        |
| 4:55 PM     | Closing Remarks   |

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# INTERNATIONAL TECHNICAL PROGRAM COMMITTEE

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# INTERNATIONAL TECHNICAL PROGRAM COMMITTEE

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# CONFERENCE INFORMATION

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## HOW TO REGISTER FOR ISSCC

**Online:** This is the only way to register and will give you immediate email confirmation of your events. Go to the ISSCC website at [www.isscc.org](http://www.isscc.org) and select the link to the Registration website.

**Payment Options:** Immediate payment can be made online via credit card. Alternative payment options are available including payment by check. Payment must be made within 10 days to hold your registration.

**Registrations received without full payment will not be processed until payment is received at YesEvents.** Please read the instructions on the Registration website.

## COVID 19 PROTOCOLS

The health and safety of our conference attendees is our top priority. The ISSCC 2023 conference Organizing Committee remains vigilant in monitoring the COVID-19 pandemic. The conference will follow CDC and State of California guidelines. ISSCC is planned as an in-person event but it also has an online offering. We look forward to you joining us in San Francisco, CA. If you don't feel comfortable participating in large gatherings, if your organization has travel restrictions, we encourage you to join us online.

## MASKS, VACCINATION, SANITIZERS

All participants are encouraged to wear an approved face covering at all times while inside the venue and while attending ISSCC. Face coverings may be removed when actively eating, drinking, or giving a presentation during a session.

Currently, proof of vaccination is no longer required in meetings in San Francisco. We will be monitoring that regulation and the ISSCC website will be updated as regulations change.

Hand sanitizing lotion will be available throughout the hotel and at the Registration desk.

## REGISTRATION DESK HOURS:

|                                |                           |
|--------------------------------|---------------------------|
| <b>Saturday, February 18:</b>  | <b>4:00 pm to 7:00 pm</b> |
| <b>Sunday, February 19:</b>    | <b>7:00 am to 8:30 pm</b> |
| <b>Monday, February 20:</b>    | <b>6:30 am to 3:00 pm</b> |
| <b>Tuesday, February 21:</b>   | <b>8:00 am to 3:00 pm</b> |
| <b>Wednesday, February 22:</b> | <b>8:00 am to 3:00 pm</b> |
| <b>Thursday, February 23:</b>  | <b>7:00 am to 2:00 pm</b> |

Students must present their Student ID at the Registration Desk to receive the student rates.

Those registering at the IEEE Member rate must provide their IEEE Membership number.

**Deadlines:** The deadline for registering at the Early Registration rates is 12:00 Midnight EST **Sunday January 8, 2023**. After January 8th, and before 12:00 Midnight EST **Monday January 23, 2023**, registrations will be processed **at the Late Registration rates**. **After January 23rd, you must register at the on-site rates.** You are urged to register early to obtain the lowest rates and ensure your participation in all aspects of ISSCC.

**Cancellations/Adjustments:** Prior to 12:00 Midnight EST **Monday January 23, 2023**, conference registration can be cancelled. Fees paid will be refunded (less a processing fee of \$75). Send an email to the registration contractor at [ISSCCinfo@yesevents.com](mailto:ISSCCinfo@yesevents.com) to cancel or make other adjustments.

**No refunds will be made after 12:00 Midnight EST January 23, 2023.** Paid registrants who do not attend the conference will have access to the on-demand material.

## IEEE MEMBERSHIP SAVES ON ISSCC REGISTRATION

Take advantage of reduced ISSCC fees by joining the Solid-State Circuits Society today, or by using your IEEE membership number. If you're an IEEE member and have forgotten your member number, simply phone IEEE at 1(800) 678-4333 and ask. IEEE membership staff will take about two minutes to look up your number for you. If you come to register on site without your membership card, you can phone IEEE then, too. Or you can request a membership number look-up by email by using the online form at: [www.ieee.org/aboutUhelp/member\\_support.html](http://www.ieee.org/aboutUhelp/member_support.html). If you're not an IEEE member, consider joining before you register to save on your fees. Join online at [www.ieee.org/join](http://www.ieee.org/join) any time and you'll receive your member number by email. If you join IEEE at the conference, you can also select a free Society membership. This offer is not available to existing IEEE members.

# CONFERENCE INFORMATION

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## SSCS MEMBERSHIP -

### A VALUABLE PROFESSIONAL RESOURCE FOR YOUR CAREER GROWTH

Get Connected! Stay Current! Invest in your Career! Membership in the Solid-State Circuits Society offers you the chance to explore solutions within a global community of colleagues in our field. Membership extends to you the opportunity to grow and share your knowledge, hone your expertise, expand or specialize your network of colleagues, advance your career, and give back to the profession and your local community.

### SSCS MEMBERSHIP DELIVERS:

- |                         |                                     |                            |
|-------------------------|-------------------------------------|----------------------------|
| Networking with peers   | - Educational development           | - Leadership opportunities |
| Tools for career growth | - Recognition for your achievements |                            |

We invite you to join or renew today to participate in exclusive educational events, access to leading research and best practice literature, and start your own career legacy by mentoring students and young professionals entering our field. It all starts with becoming a member of the Solid-State Circuits Society where you can:

-Connect with your Peers - valuable networking opportunities through our world-class conferences, publication offerings, social media extensions, and interactive educational opportunities.

-Keep up with the latest trends and cutting-edge developments in our industry - through our electronic newsletters, member magazine "Solid-State Circuits Magazine", and our award winning "Journal of Solid State Circuits".

-Access valuable career and educational tools - saving you both time and money with 24/7 access to our website and members-only professional development and educational material; Distinguished Lecturer Tours, Tutorials, and webinars by subject matter experts.

-Access exclusive SSCS Conference Digests for ISSCC, CICC, A-SSCC, ESSCIRC, and Symposium on VLSI Circuits.

-Access publications and EBooks - discounted access to vast online document libraries of journals, standards, and conference papers offer you one-third of the world's technical research to keep your knowledge current. Publications included in your SSCS membership are the "RFIC Virtual Journal" (RFVJ) and the "Journal on Exploratory Solid-State Computational Devices and Circuits" (JxCDC), Solid State Letters, and our newest Journal, the "Open Journal of Solid State Circuits" (OJ-SSC) an open access publication.

### SSCS MEMBERSHIP SAVES EVEN MORE ON ISSCC REGISTRATION

This year, SSCS members will again receive an exclusive benefit of a \$30 discount on the registration fee for ISSCC in addition to the IEEE discount. Also, the SSCS will again reward our members with a \$10 Starbucks gift card when they attend the Conference as an SSCS member in good standing.

Join or renew your membership with IEEE's Solid-State Circuits Society today at [sscs.ieee.org](http://sscs.ieee.org) - you will not want to miss out on the opportunities and benefits your membership will provide now and throughout your career.

### ITEMS INCLUDED IN REGISTRATION

**Technical Sessions:** Registration includes admission to all technical and evening sessions starting Sunday evening and continuing throughout Monday, Tuesday and Wednesday. ISSCC does not offer partial conference registrations.

**Technical Book Display:** Several technical publishers will have collections of professional books and textbooks for sale during the Conference. The Book Display will be open on Monday from Noon to 7:00 pm; on Tuesday from 10:00 am to 7:00 pm; and on Wednesday from 10:00 am to 3:00 pm.

**Demonstration Sessions:** Hardware demonstrations will support selected papers on Monday and Tuesday evenings.

**Author Interviews:** Author Interviews will be held Monday, Tuesday and Wednesday evenings. Authors from each day's papers will be available to discuss their work.

**Monday Social Hour:** Refreshments will be available starting at 5:15 pm.

**University Events:** Several universities are planning social events during the Conference. Check the University Events display at the conference for the list of universities, locations and times of these events.

**Publications:** Conference registration includes:

-**Papers Visuals:** The visuals from all papers presented will be available by download.

-**Demonstration Session Guidebook:** A descriptive guide to the Demonstration Session will be available by download.

-**Note:** Instructions will be provided for access to all downloads. Downloads will be available both during the Conference and for a limited time afterwards.

# CONFERENCE INFORMATION

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## OPTIONAL EVENTS

**Educational Events:** Many educational events are available at ISSCC for an additional fee. There are twelve 90-minute Tutorials that will be available virtually, not in person at the conference, there is an in-person Q&A. The forums and Short Course will be live, in-person. There will be three all-day Forums on Sunday. There are four additional all-day Forums on Thursday as well as an all-day Short Course. The Forums and Short Course include breakfast, lunch and break refreshments. See the schedule for details of the topics and times.

## OPTIONAL PUBLICATIONS

**ISSCC 2023 Publications:** The following ISSCC 2023 digital publications can be purchased in advance or on site:

**2023 ISSCC Download USB:** All of the downloads included in conference registration, (regular papers and presentations) **(mailed in March)**

**2023 Tutorials USB:** All of the 90 minute Tutorials **(mailed in June)**.

**2023 Short Course USB:** **(mailed in June)**.

The Short Course and Tutorial USBs contain audio and written English transcripts synchronized with the presentation visuals. In addition, the USBs contain a pdf file of the presentations and pdf files of key reference material.

**Earlier ISSCC Publications:** Selected publications from earlier conferences can be purchased. There are several ways to purchase this material:

**-Items listed on the registration website** can be purchased with registration and picked up at the conference.

**-Visit the ISSCC Publications Desk.** This desk is located in the registration area and has the same hours as conference registration. With payment by cash, check or credit card, you can purchase materials at this desk. See the posted list at the Conference for titles and prices.

**-Visit the ISSCC website** at [www.isscc.org](http://www.isscc.org) and click on the link "SHOP/Shop ISSCC/Shop Now" where you can order online or download an order form to mail, email or fax. For a small shipping fee, this material will be sent to you immediately and you will not have to wait until you attend the Conference to get it.

## HOW TO MAKE HOTEL RESERVATIONS

**Online:** ISSCC participants are urged to make their hotel reservations at the San Francisco Marriott Marquis online. Go to the conference website and click on the Hotel Reservation link. **Conference room rates are \$306 for a single/double (per night plus tax).** In addition, ISSCC attendees booked in the ISSCC group receive **in-room Internet access for free.** All online reservations require the use of a credit card. Online reservations are confirmed immediately. You should print the page containing your confirmation number and reservation details and bring it with you when you travel to ISSCC. **Telephone:** Call 877- 622-3056 (US) or 415-896-1600 and ask for "Reservations." When making your reservation, identify the group as ISSCC 2022 to get the group rate.

**Hotel Deadline:** Reservations must be received at the San Francisco Marriott Marquis no later than 5 pm Pacific Time January 29, 2023 to obtain the special ISSCC rates. A limited number of rooms are available at these rates. **Once this limit is reached or after January 29th, the group rates may no longer be available and reservations will be filled at the best available rate.** Changes: Before the hotel deadline, your reservation can be changed by calling the telephone numbers above. After the hotel deadline, call the Marriott Marquis at 415-896-1600 (ask for "Reservations"). Have your hotel confirmation number ready.

## IEEE NON-DISCRIMINATION POLICY

IEEE is committed to the principle that all persons shall have equal access to programs, facilities, services, and employment without regard to personal characteristics not related to ability, performance, or qualifications as determined by IEEE policy and/or applicable laws.

# CONFERENCE INFORMATION

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## EVENT PHOTOGRAPHY

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## TAKING PICTURES, VIDEOS OR AUDIO RECORDINGS DURING ANY OF THE SESSIONS IS NOT PERMITTED

## REFERENCE INFORMATION

|                         |   |  |
|-------------------------|---|--|
| Conference Website:     | www.isscc.org   |  |
| ISSCC Email:            | ISSCC@ieee.org  |  |
| Registration questions: | ISSCCinfo@yesevents.com   |  |
| Hotel Information:      | San Francisco Marriott Marquis<br>780 Mission Street<br>San Francisco, CA 94103     | Phone: 415-896-1600                      |
| Press Information:      | Kenneth C. Smith<br>University of Toronto<br>Email: lcfujino@aol.com                | Phone: 416-418-3034                      |
| Registration:           | YesEvents<br>PO Box 3024<br>Westminster, MD 21158<br>Email: issccinfo@yesevents.com | Phone: 800-937-8728<br>Fax: 410-559-2236 |

### Hotel Transportation

Visit the ISSCC website "Registration/Transportation from Airport" page for helpful travel information and links. You can get a map and driving directions from the hotel website at:  
[www.marriott.com/hotels/travel/sfodt-san-francisco-marriott-marquis/](http://www.marriott.com/hotels/travel/sfodt-san-francisco-marriott-marquis/)

### Next ISSCC Dates and Location:

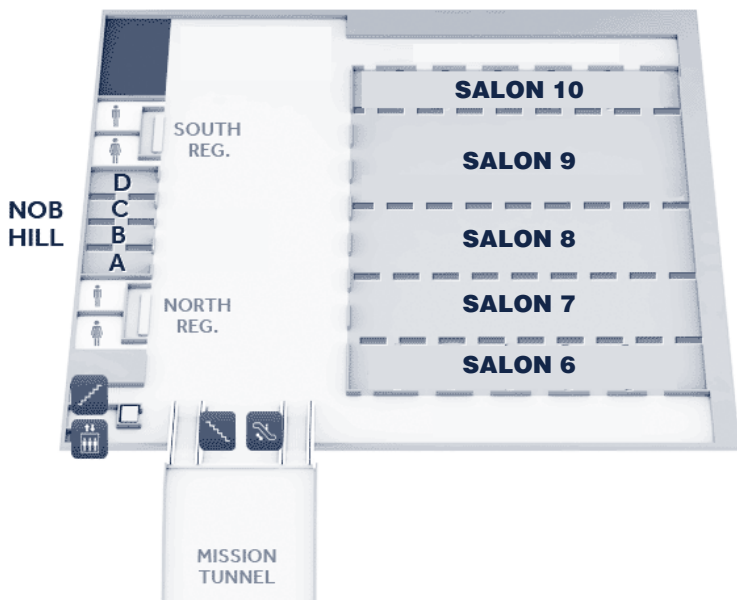
ISSCC 2024 will be held on February 18-22, 2024  
at the San Francisco Marriott Marquis Hotel.

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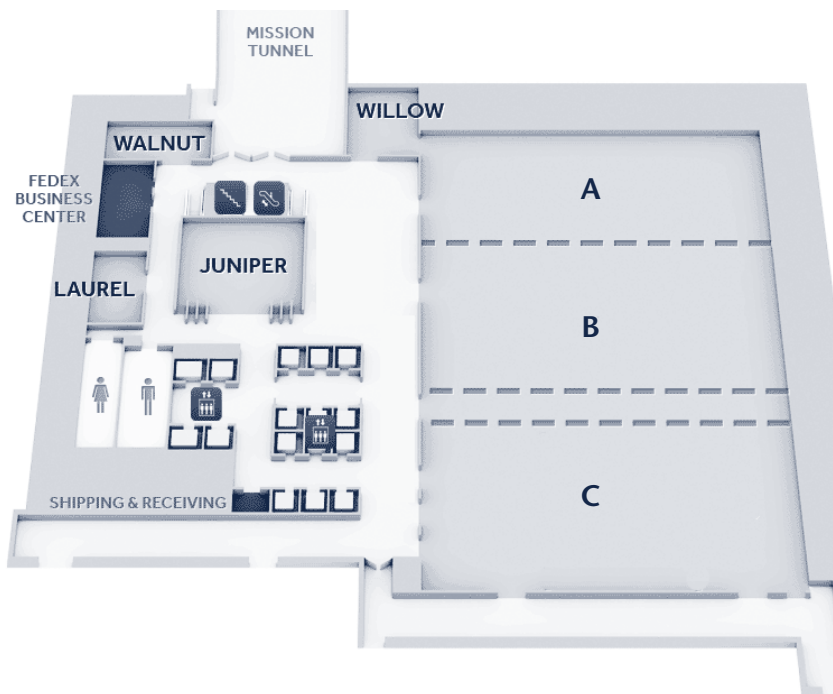
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|------------------------------------|-------------------|
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| Data Converters:                   | Jan Westra        |
| Digital Architectures & Systems:   | Thomas Burd       |
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**ISSCC 2023 ADVANCE PROGRAM**