IEEE SOLID-STATE CIRCUITS SOCIETY

ADVANCE PROGRAM

2017 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

FEBRUARY 5, 6, 7, 8, 9

CONFERENCE THEME:

INTELLIGENT CHIPS FOR A SMART WORLD

SAN FRANCISCO
MARRIOTT MARQUIS HOTEL

5-DAY PROGRAM

SUNDAY ALL-DAY

2 FORUMS: IC REGULATORS FOR SoC AND IoT; FREQUENCY GENERATION FOR WLs AND WLn

10 TUTORIALS: mm-WAVE SYNTHESIZERS; NAND FLASH TRENDS; PHYSIOLOGICAL-READOUT CIRCUITS; LOW-ENERGY PROCESSORS FOR DEEP LEARNING; TIME-BASED CIRCUITS; SIGNAL INTEGRITY FOR Gb/s LINKS; DIGITAL-INTENSIVE PLLS; CLASS-D AMPLIFIERS; IC mm-WAVE TX/RX SPATIAL FILTERING; CELL AND BRAIN INTERFACING

2 EVENING EVENTS ON GRADUATE STUDENT RESEARCH IN PROGRESS, INTELLIGENT MACHINES

THURSDAY ALL-DAY

4 FORUMS: FUTURE COMPUTATIONAL PARADIGMS: DEEP LEARNING TO NEUROMORHISM; WIRELESS TRANSCEIVERS FOR LAN/WAN; WIRELINE TRANSCEIVERS FOR MEGA DATA CENTERS AT/ABOVE 50Gb/s; PERFORMANCE LIMITS IN DATA CONVERTERS

SHORT-COURSE: ULTRA-LOW-POWER ANALOG DESIGN

ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and application to maintain technical currency, and to network with leading experts.

CONFERENCE TECHNICAL HIGHLIGHTS

On Sunday, February 5th, the day before the official opening of the Conference, ISSCC 2017 offers:

- A choice of up to 4 of a total of 10 Tutorials, or
- A choice of 1 of 2 all-day Advanced-Circuit-Design Forums

The 90-minute tutorials offer background information and a review of the basics in specific circuit-design topics. In the all-day Advanced-Circuit-Design Forums, leading experts present state-of-the-art design strategies in a workshop-like format. The Forums are targeted at designers experienced in the technical field.

On Sunday evening, there are two events: A Special-Topic Session entitled, "Intelligent Machines: Will the Technological Singularity Happen" will be offered starting at 8:00pm. In addition, the Student-Research Preview, featuring short presentations followed by a poster session from selected graduate-student researchers from around the world will begin at 7:30 pm. Introductory remarks at the Preview will be provided by a distinguished member of the solid-state circuit community, Professor Hoi-Jun Yoo of KAIST, Daejeon, Korea.

On Monday, February 6th, ISSCC 2017 offers four plenary papers on the theme: "Intelligent Chips for a Smart World". On Monday at 12:15 pm, there will be a Women's-Networking Event, a luncheon. On Monday afternoon, there will be five parallel technical sessions, followed by a Social Hour open to all ISSCC attendees. The Social Hour, held in conjunction with Book Displays and Author Interviews, will also include a Demonstration Session, featuring posters and live demonstrations of selected papers from industry and academia. Monday evening will include 2 events entitled "Quantum Engineering: Hype, Spin, or Reality" and "Semiconductor Economics: How Business Decisions Are Engineered".

On Tuesday, February 7th, there are five parallel technical sessions, both morning and afternoon. A Social Hour open to all ISSCC attendees will follow. The Social Hour, held in conjunction with Book Displays and Author Interviews, will also include a second Demonstration Session. Tuesday evening includes two events, entitled "Return of Survey Says!" and "When Will We Stop Driving Our Cars".

On Wednesday, February 8th, there will be five parallel technical sessions, both morning and afternoon, followed by Author Interviews.

On Thursday, February 9th, ISSCC offers a choice of five all-day events:

- A Short Course entitled "Ultra-Low-Power Analog Design"
- Four Advanced-Circuit-Design Forums entitled
  - "Beyond the Horizon of Traditional Computing: From Deep Learning to Neuromorphic Systems";
  - "Wireless Low-Power Transceivers for Local and Wide-Area Networks";
  - "Wireline Transceivers for Mega Data Centers: 50Gb/s and Beyond";
  - "Pushing the Performance Limits in Data Converters".

Registration for educational events on Sunday and Thursday will be filled on a first-come first-served basis. Use of the ISSCC Web-Registration Site (http://www.isscc.org) is strongly encouraged. Registrants will be provided with immediate confirmation on registration for the Conference, Tutorials, Forums, and the Short Course.

Need Additional Information? Go to: www.isscc.org

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There are a total of 10 tutorials this year on 10 different topics. Each tutorial, selected through a competitive process within each subcommittee of the ISSCC, presents the basic concepts and working principles of a single topic. These tutorials are intended for non-experts, graduate students and practicing engineers who wish to explore and understand a new topic.

Ali Sheikholeslami
ISSCC Education Chair

8:30 AM

T1 mm-Wave Frequency Generation and Synthesis in Silicon

Payam Heydari, *University of California, Irvine, Irvine, CA*

It is anticipated that mm-wave multi-antenna transceivers will be architectures of choice for multi-Gbps wireless communication systems. Millimeter-wave oscillators/synthesizers are crucial building blocks in these transceivers. This tutorial presents an overview of the fundamentals of mm-wave frequency synthesis and signal generation in silicon. Starting from a basic theory of oscillation, this tutorial adopts a step-by-step approach towards an understanding of fundamental challenges in designing mm-wave oscillators/synthesizers. It goes through the analysis and design of both mm-wave varactor-based and varactor-less VCOs and discusses existing trade-offs between different topologies. Next, closed-loop frequency-generation techniques for both mm-wave single-path as well as multi-antenna transceiver architectures are discussed. This includes the design of fundamental phased-locked-based synthesizers as well as circuit techniques to design the LO circuits for multi-antenna transceivers.

Payam Heydari is currently a full professor of electrical engineering at University of California, Irvine, CA. He is best known for pioneering work in silicon-based mm-wave ICs for radar, sensing, and wireless communications.

8:30 AM

T2 NAND Flash Memory Design and Architecture Trends

Sungdae Choi, *SK hynix, Icheon-si, Korea*

NAND flash technology has come to dominate the nonvolatile memory market due to its low cost and high capacity. In the early days, it was used in media storage devices, an application in which its low read/write performance was acceptable. As we head into the future, new systems will demand faster storage, which will require new approaches to improve NAND flash performance.

This tutorial will cover the basics of NAND flash memory and provide an understanding of how its performance compares with conventional memory. Techniques to accelerate both read and write performance will be presented. Limitations of the traditional 2D structure and the recent transition to 3D structures will be discussed as a key breakthrough for future NAND flash memory devices.

Sungdae Choi received the B.S., M.S. and Ph.D. degrees from KAIST, Korea, in 2001, 2003 and 2006, respectively. After post-doctoral research activities from 2006 to 2009, he joined SK hynix where he is currently working as a senior engineer in the Flash Development Division.

8:30 AM

T3 Readout Circuits for Physiological Signal Measurements

Long Yan, *Samsung Electronics, Hwaseong-si, Korea*

Wearable electronics has become mainstream, enabling personal healthcare technologies in the form of patches, wristbands, and smart watches. Measurements of physiological parameters outside of traditional clinical settings make reliable and sustainable measurement a real challenge.

This tutorial provides an overview of how to design low-power readout circuits for measuring different physiological signal modalities in a wearable environment. The talk starts with discussing signal integrity problems. We then focus on different topologies of instrumentation amplifiers and readout circuits (including commercially available ICs in the filed) for measuring ECG, Bio-Impedance, and Photoplethysmography (PPG).

Long Yan received the B.S. and M.S. degree in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2007 and 2009, respectively, and the Ph.D. degree from the same university in 2011.

In 2010, he was with the Microsystems Technology Laboratories at the Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, as a visiting student, where he developed a low-power EEG readout front-end circuit for patient-specific seizure classification. From 2011 to 2014, he has been with IMEC, Leuven, Belgium, as a Senior Scientist. His research at IMEC has focused on the development of low-power mixed-mode circuits for wearable and implantable applications. Since December 2014, he joined Samsung Electronics, Hwaseong, South Korea where he is now leading analog interface circuit developments for bio-sensors. From 2015, Dr. Yan serves on the technical program committee of the International Solid State Circuit Conference (ISSCC).

10:30 AM

T4 Energy-Efficient Processors for Deep Learning

Marian Verhelst, *KU Leuven, Heverlee, Belgium*

Deep learning has become popular for image recognition, and more recently, for other pattern matching tasks (e.g., speech processing, text analysis, etc.). Deep learning, however, is associated with significant computational complexity, which until recently, made it feasible only on power-hungry server platforms. However, we now see a trend towards embedded processing of deep-learning networks.

After an introduction into deep learning and its implementation challenges, this tutorial will give an overview of processing architectures to enable efficient network evaluations on embedded platforms. This discussion is tightly interwoven with coverage of emerging implementation-driven algorithmic innovations, to understand the impact of new deep learning algorithms on embedded hardware design. The tutorial will give the audience an understanding of the opportunities and implementation challenges in embedded deep learning, and enable one to comprehend research on deep learning processors.

Marian Verhelst is assistant professor at MICAS – KU Leuven, Belgium. Her research focuses on embedded machine learning, low-power sensing and processing for the internet-of-things. Marian is member of the Young Academy of Belgium, the ISSCC and DATE executive committees and is an associate editor of JSSC.

10:30 AM

T5 Fundamentals of Time-Based Circuits

Matt Straayer, *Maxim Integrated Products, North Chelmsford, MA*

Time-based circuits have recently been developed as an alternative and enhancement to voltage-based signal processing due to the availability of advanced process nodes with fast transistors and low supply voltages. These time-based circuits offer unique attributes, ranging from simple, area-efficient quantizers to more complex techniques for time-based processing such as interpolation and noise shaping. This tutorial will cover the fundamentals and metrics of time-based circuits, highlight a number of architectures that directly utilize time, and discuss tradeoffs for these circuits in the context of various application requirements, including a comparison to more traditional voltage-based circuits.

Matt Straayer received the Ph.D. degree from MIT in 2008. He worked at Integrated Sensing Systems, Inc. and MIT Lincoln Laboratory, before he helped to co-found Cambridge Analog Technologies, Inc. (CAT), Billerica, MA, where he led the technical development of zero-crossing circuits. In 2011 CAT was acquired by Maxim Integrated, where he has continued to advance mixed-signal circuit architectures and develop enabling IP for a wide range of product areas and applications.

10:30 AM

T6 Signal Integrity Analysis for Gb/s Links

Tony Chan Carusone, *University of Toronto, Toronto, Canada*

Signal integrity analysis permits circuit designers to model and evaluate high-speed I/O with fast simulations, both for quick evaluation of design alternatives and accurate high-level verification. This tutorial covers theoretical underpinnings and practical tools for behavioral modeling and simulation of wireline chip-to-chip links. Attendees will learn to accurately model lossy interconnects, packaging parasitics, and transceiver front-ends. The tutorial will also introduce nondeterministic impairments such as noise and jitter, and the modeling of linear and decision-feedback equalization. Analysis techniques amenable to both circuit-level (netlist) simulators and high-level modeling (e.g. Matlab) tools will be covered.

Tony Chan Carusone is a professor at the University of Toronto and occasional consultant to industry. He co-authored the 2nd edition of the book "Analog Integrated Circuit Design" and 6 best papers at Solid-State Circuits Society conferences. He is currently a Distinguished Lecturer for the SSCS.

1:30 PM

T7 Design Trade-Offs in Digital Intensive PLLs

Ping-Ying Wang, *CMOS-Crystal, Hsinchu, Taiwan*

The tutorial will give a comprehensive overview and provide an intuitive understanding of digital PLLs in spatial domain. Operating principles and limitations of digital PLLs are demonstrated by introducing an architecture-independent model with numerical calculations in the time domain. Various digital PLL architectures, including all-digital and hybrid PLLs are presented, followed by design strategies for building blocks, such as digital loop filters with latency cancellation, numerically-controlled oscillators with suppression of quantization error, digitally-controlled oscillators with all-digital supply regulation and time-to-digital converters with time amplifiers. Finally, all-digital self-calibration techniques and digitally-assisted PLLs are discussed.

Ping-Ying Wang received the M.S. degree in physics science from National Taiwan University, Taipei, Taiwan, in 1994. From 1999 to 2003 he worked at Etron and Realtek, Taiwan, developing all-digital PLLs and spread-spectrum clocking. In 2003, He joined Mediatek, Taiwan, where he developed all-digital CDR for high-speed serial links, hybrid PLLs and all-digital self-calibration techniques for PLL-based modulators. From 2010 to 2014, he was technical director for the Mixed-Signal Design Division working on all-digital regulation techniques and all-digital charge pumps for PLLs. Currently, he is co-founder of a company, CMOS-Crystal, focused on PLLs integrated with crystal amplifiers. He holds over 36 granted patents, and has published over 23 peer-reviewed journal and conference papers. He serves on the IEEE International Solid-State Circuits Conference DCT subcommittee.

1:30 PM

T8 Fundamentals of Class-D Amplifier Design

Xicheng Jiang, *Broadcom, Irvine, CA*

Class-D amplifiers, or switching amplifiers, are popular components in mixed-signal IC design and widely adopted for smart phones and tablets with rich multimedia thanks to their high-efficiency and high-output power capability. Their applications range from audio and video drivers to envelope tracking for power amplifiers. In this tutorial, Class-D amplifier fundamentals and the design of a CMOS high-performance Class-D amplifier will be covered. Topics include 1) an overview of amplifier topologies, such as Class-A, Class-AB, Class-D, Class-G, and Class-H; 2) architecture trade-offs; 3) comparisons of linear amplifiers and switching amplifiers and different modulation schemes; 4) analog implementations vs. digital implementations; and 5) detailed implementations of building blocks and the state-of-the-art of designs. Practical design examples are used throughout the presentation. Advanced topics include Pop-click suppression, EMI reduction, and speaker protection.

Xicheng Jiang received a B.S. degree from University of Science and Technology of China, Hefei, China, and a M.S. and Ph.D. degrees in electrical engineering from University of California, Los Angeles, CA. Since 1997, he has been with Broadcom, where he is a Director of Engineering and a Broadcom Distinguished Engineer. His research interest includes data converters, high-speed serial transceivers, cellular baseband, Hi-Fi audio drivers, microphone interfaces, and precision sensor interfaces.

Dr. Jiang is a Fellow of IEEE. He is a named inventor on more than 40 issued and pending U.S. patents and has authored or coauthored over 40 conference and journal papers and 1 book from Cambridge University Press titled "Digitally-Assisted Analog and Analog-Assisted Digital IC Design." He is the co-recipient of the CICC 2009 Best Paper Award and the CICC 2013 Best Poster Paper Award.

3:30 PM

T9 Integrated mm-Wave Transmitters and Receivers for Spatial-Filtering Arrays

Arun Natarajan, *Oregon State University, Corvallis, OR*

This tutorial will focus on beamforming/spatial-filtering architectures and circuits for integrated mm-Wave transmitter and receiver arrays targeting multi-Gb/s communication and high-resolution radar. Design strategies for analog/digital-intensive building blocks specific to integrated arrays, such as phase shifters and signal combiners, will be discussed in the context of array system performance and link budget. The emergence of 5G has led to increasing interest in large-scale mm-Wave phased arrays/MIMO arrays for communication networks. An overview of transmit/receive circuit/system challenges in large-scale arrays will be presented followed by recent efforts towards realizing scalable, digital-intensive arrays.

Arun Natarajan teaches at Oregon State University where his current research is focused on RF, mm-Wave and sub-mm-Wave integrated circuits and systems for high-speed wireless communication and imaging.

3:30 PM

T10 Circuits and Technologies for Cell and Brain Interfacing

Nick Van Helleputte, *imec, Heverlee, Belgium*

Cell and brain interfacing has gained a lot of interest in recent years. Thanks to advancements in technology scaling, current state-of-the-art systems are able to record the electrical activity down to single neuron resolution from several hundreds of recording sites at the same time. This is a critical tool for the neuroscientist to help understand how our brain operates. In recent years, stimulation has also gained a lot of interest. Neural stimulation serves many potential applications like restoring bodily functions for disabled people, suppressing pain, brain-computer-interfaces and Parkinson's disease. This tutorial will focus on the circuit techniques and technologies to enable such high-density neural recording and stimulation. It will go from high-level system design aspects, to processing/technology aspects (electrodes) and will end with specific circuit design techniques.

Nick Van Helleputte received the M.S. degree in electrical engineering in 2004 from the Katholieke Universiteit Leuven, Belgium. He received his Ph.D. degree from the same institute in 2009 (MICAS research group). His Ph.D. research focused on low-power ultra-wide-band analog front-end receivers for ranging applications. He joined imec in 2009 as an Analog R&D Design Engineer. He is currently team leader of the biomedical circuits and systems team. His research focus is on ultra-low-power circuits for biomedical applications. He has been involved in analog and mixed-signal ASIC design for wearable and implantable healthcare applications. Nick is an IEEE member and served on the technical program committee of VLSI Circuits Symposium and ISSCC.

F1: Integrated Voltage Regulators for SoC and Emerging IoT Systems

Organizers: **Makoto Takamiya**, *University of Tokyo, Tokyo, Japan*
Yogesh K. Ramadass, *Texas Instruments, San Jose, CA*
Keith Bowman, *Qualcomm, Raleigh, NC*

Committee: **Gerard Villar Pique**, *NXP Semiconductors, Eindhoven, The Netherlands*
Shuichi Nagai, *Panasonic, Osaka, Japan*
Dennis Sylvester, *University of Michigan, Ann Arbor, MI*

Integrated voltage regulation is critical to the energy efficiency in systems ranging from high-end processors to emerging IoT devices. For large-scale systems, challenges include the large number of voltage domains, DVFS per domain, large current transients, and wide dynamic range of current loads. In the ultra-low-power space, major obstacles include coping with uncertainty in energy harvesting sources, low input power levels, and small decoupling capacitance in low-cost packages. This forum reviews modern designs and presents recent advances to address future IoT requirements.

Forum Agenda

Time:	Topic:
8:00 AM	Breakfast
8:00 AM	Introduction by Chair
8:30 AM	**Overview and Benchmarking of State-of-the-Art Integrated Voltage Regulators** ***Henk Jan Bergveld,*** *NXP Semiconductors, Eindhoven, The Netherlands*
9:20 AM	**Multi-Phase Buck Converters for Integrated Voltage Regulation in High-Performance SoCs** ***Edward (Ted) Burton****, Intel, Hillsboro, OR*
10:10 AM	Break
10:35 AM	**On-Chip Switched Capacitor Voltage Regulators for High-Performance Processors** ***Toke Meyer Andersen,*** *Nordic Power Converters, Copenhagen, Denmark*
11:25 AM	**Powering Systems-on-Chip for Automotive and Information/Communications Technology** ***Juergen Wittmann,*** *Reutlingen University, Reutlingen, Germany*
12:15 PM	Lunch
1:20 PM	**Power Management System with Ambient Energy Sources for Internet of Things (IoT)** ***Chulwoo Kim,*** *Korea University, Seoul, Korea*
2:10 PM	**Wireless Powering for Wearable and Implantable Devices** ***Wing-Hung Ki,*** *The Hong Kong University of Science and Technology, Hong Kong*
3:00 PM	Break
3:20 PM	**Advances in Integrated Low-Dropout Regulators (LDOs) for Fine-Grained Spatiotemporal Power Management of Digital Load Circuits** ***Arijit Raychowdhury,*** *Georgia Institute of Technology, Atlanta, GA*
4:10 PM	**Advances in Hybrid and Resonant Switched-Capacitor Voltage Regulators** ***Seth R. Sanders,*** *University of California, Berkeley, CA*
5:00 PM	Closing remarks by Chair

F2: High-Performance Frequency Generation for Wireless and Wireline Systems

Organizer: **Jiayoon Ru,** *Broadcom, Irvine, CA*

Committee: **Kohei Onizuka,** *Toshiba, Kawasaki, Japan*
Pavan Hanumolu, *University of Illinois, Urbana-Champaign, Urbana, IL*
Roberto Nonis, *Infineon, Villach, Austria*
Howard Luong, *Hong Kong University of Science and Technology, Hong Kong, China*
Jan Craninckx, *imec, Leuven, Belgium*

Frequency generation equips nearly all electronic systems and is a critical performance factor for many of them. This forum focuses on wireless and wireline systems, which demand high performance clocks, and looks for synergies between them. The topics cover both fundamental techniques and specific applications. State-of-the-art techniques will be explored in depth, such as high-FOM VCOs, digital-to-time converters, sampling phase-detectors, synthesizable and digital PLLs. Attention will also be on booming applications, such as high-speed wireline, FMCW radar, mm-wave and THz. The forum aims at bringing together the contemporary top interests with added value and sowing seeds to inspire the future.

Forum Agenda

Time:	Topic:
8:00 AM	Breakfast
8:25 AM	Introduction ***Jiayoon Zhiyu Ru,*** *Broadcom, Irvine, CA*
8:30 AM	**Integrated Harmonic Oscillators** ***Pietro Andreani,*** *Lund University, Lund, Sweden*
9:20 AM	**Application of Digital-to-Time Converters in PLL and MDLL Frequency Synthesizers** ***Carlo Samori,*** *Politecnico di Milano, Milano, Italy*
10:10 AM	Break
10:30 AM	**Sub-Sampling-Based Phase Locked Loops** ***Eric Klumperink,*** *University of Twente, Enschede, The Netherlands*
11:15 AM	**Synthesizable PLL Using Digital Standard Cell Library** ***Kenichi Okada,*** *Tokyo Institute of Technology, Tokyo, Japan*
12:00 PM	Lunch
1:00 PM	**High-Resolution Low-Power TDCs and ADPLLs for Novel Receiver Architecture** ***Akihide Sai,*** *Toshiba, Kawasaki, Kanagawa, Japan*
1:45 PM	**High-Performance Clock Generation and Distribution in Very-High-Speed Wireline Transceivers** ***Nicola Da Dalt,*** *Intel, San Jose, CA*
2:30 PM	Break
2:50 PM	**Fully-Integrated Millimeter-Wave Clock Generation — from DC to 300GHz** ***Jri Lee,*** *National Taiwan University, Taipei, Taiwan*
3:35 PM	**CMOS Frequency Synthesis and Signal Generation Beyond 0.5THz** ***Frank Chang,*** *University of California, Los Angeles, CA*
4:20 PM	**Frequency Generation for FMCW RADAR** ***Sreekiran Samala,*** *Texas Instruments, Dallas, TX*
5:05 PM	Conclusion

EE1: STUDENT RESEARCH PREVIEW (SRP)

The Student Research Preview (SRP) will highlight selected student research projects in progress. The SRP consists of 24 one-minute presentations followed by a Poster Session, by graduate students from around the world, which have been selected on the basis of a short submission concerning their on-going research. Selection is based on the technical quality and innovation of the work. This year, the SRP will be presented in three theme sections: Analog and Mixed Signal; Imagers, Biomedical Circuits and Advanced Digital Systems; Communications and Power.

The Student Research Preview will begin with a brief talk by a distinguished member of the solid-state circuit community, Professor Hoi-Jun Yoo of KAIST, Korea.

His remarks are scheduled for Sunday, February 5th, starting at 7:30 pm. The SRP is open to all ISSCC registrants.

Chair	SeongHwan Cho	KAIST
Secretary	Denis Daly	Omni Design Technologies
Advisor	Anantha Chandrakasan	MIT
Advisor	Jan Van der Spiegel	University of Pennsylvania
Media/Publications	Laura Fujino	University of Toronto
A/V	Trudy Stetzler	

Committee Members

Bryan Ackland	Stevens Institute of Technology
Jason Anderson	University of Toronto
Andrea Baschirotto	University of Milan-Bicocca
William Bowhill	Intel
Ben Calhoun	University of Virginia
SeongHwan Cho	KAIST
Hayun Chung	Korea University
Denis Daly	Omni Design Technologies
Andreas Demosthenous	University College London
Chun-Huat Heng	National University of Singapore
Makoto Ikeda	University of Tokyo
Jaeha Kim	Seoul National University
Qiang Li	Univ. of Electronic Sci. & Tech. of China
Tsung-Hsien Lin	National Taiwan University
Shahriar Mirabbasi	University of British Columbia
Tinoosh Mohsenin	University of Maryland
Cormac O'Connell	TSMC, Canada
Mondira Pant	Intel
Shanthi Pavan	India Institute of Technology
Patrick Reynaert	K.U. Leuven
Soojung Ryu	Samsung
Farhana Sheikh	Intel
Bing Sheu	Chang Gung University
GuoXing Wang	Shanghai Jiao Tong University
Jeffrey Weldon	Carnegie Mellon University
Peter Wu	National Chiao Tung University
Jerald Yoo	Masdar Institute of Science & Tech.
Samira Zaliasl	IMEC

EE2: Intelligent Machines: Will the Technological Singularity Happen?

Organizer: **Stefano Pellerano,** *Intel, Hillsboro, OR*
Sungdae Choi, *SK Hynix Semiconductor, Gyeonggi-do, Korea*

Chair: **Jan Rabaey,** *University of California, Berkeley, CA*

Artificial intelligence (AI) will no doubt have a significant impact on society in the coming years. But how intelligent can a machine be? When artificially-general intelligence is capable of recursive self-improvement, a hypothetical 'runaway effect' — an intelligence explosion — might happen, yielding an intelligence surpassing all current human control or understanding. This event is known as the *technological singularity*; this is the point beyond which events may become unpredictable or even unfathomable to human intelligence. This panel will picture the current state of the art for AI, deep learning and robotics, and try to predict where this technology is heading.

Panelists

Vijaykrishnan Narayanan, *Pennsylvania State University, State College, PA*
Hiroaki Kitano, *Sony Computer Science Laboratories, Tokyo, Japan*
Hoi-Jun Yoo, *KAIST, Daejeon, Korea*
Vikas Sindhwani, *Google Brain, New York, NY*
Ruchir Puri, *IBM Watson, New York, NY*

Plenary Session — Invited Papers

Chair: ***Anantha Chandrakasan,*** *Massachusetts Institute of Technology, Cambridge, MA*
ISSCC Conference Chair

Associate Chair: ***Boris Murmann,*** *Stanford University, Stanford, CA*
ISSCC International Technical-Program Chair

FORMAL OPENING OF THE CONFERENCE **8:30 AM**

1.1 A Smart Design Paradigm for Smart Chips — 8:45 AM

Cliff Hou, *Vice President, Research & Development, TSMC, Hsinchu, Taiwan*

The world requires more specialized smart chips for connecting people intelligently at all times. Requirements for such chips in computing capability, power consumption, and form factor are becoming ever more demanding, while the market window is significantly shrinking. This talk explores the trends in chip innovation from costly multi-chip and SoC solutions to separated chips combined with wafer-stacking or 3-D packaging. These trends are further driving system-level integration for improved chip and systems performance, cycle time, and costs.

To capitalize on such mega-trends, innovations extending Moore's Law and efforts on specialty technologies for advancing connectivity are discussed. The ultimate goal is to optimize system performance through system-level integration of functionalities in advanced 3-D packaging. These will introduce new design challenges, where possible solutions are further gated by learning curves and cycle times.

Smart-chip designers are increasingly looking for opportunities where others can supply expertise and assets, whether as single-chip designs or system-level integrations. We highlight the emergence of a new collaborative paradigm, which is moving from technology-centric options to total platform-centric solutions sufficiently broad to address the unique challenges of the next big things, particularly in mobile, IoT, automotive, high-performance computing.

1.2 Dynamics of Exponentials in Circuits and Systems — 9:20 AM

Ahmad Bahai, *Chief Technology Officer, Texas Instruments, Santa Clara, CA*

Astonishing progress in semiconductor devices, circuits, and manufacturing has prompted an unprecedented revolution in electronics. "Things" are getting smarter and more connected, with higher semiconductor content. Smart personal electronics, autonomous systems, and smart factories are prime examples.

These impressive developments are fueled by the power of exponentials: CMOS scaling, efficiency of semiconductor manufacturing, the bandwidth efficiency of communication systems, and total network capacity have all been doubling almost every two years! The sheer scaling of CMOS has dominated the challenges and promises of advanced IC design. Advanced digital-intensive designs count on denser, faster, and cheaper switches. Along the way, analog and RF designs have creatively embraced the challenge of implementing analog topologies on digitally-optimized processes.

The present slowdown of the CMOS scaling trend brings exciting opportunities for "multi-dimensional innovations" in circuits and systems: The continuing demand for higher performance, in many applications, will further tilt solutions toward creative system and circuit topologies. Many emerging complementary technologies such as MEMS-based sensors and timing references, III-V devices, high-performance SiGe devices, and silicon photonics, will not necessarily integrate with CMOS monolithically. However, they enable opportunities for system repartitioning and new circuit topologies in applications such as sensing, power, high voltage, high-performance RF, and precision timing.

CMOS is here to stay for the foreseeable future! It will simply coexist synergistically with emerging technologies. This talk will discuss opportunities in "multi-dimensional innovation" that will make the future of the field less predictable.....but even more interesting and exciting!

ISSCC, SSCS, IEEE AWARD PRESENTATIONS **9:55 AM**

BREAK **10:20 AM**

1.3 The Development of High-Speed DNA Sequencing: Jurassic Park, Neanderthal, Moore, and You — 10:45 AM

Jonathan Rothberg
Founder, 4Catalyzer and Adjunct Professor of Genetics, Yale School of Medicine, New Haven, CT

Since Watson and Crick's 1953 landmark discovery that biological information was encoded in DNA as a sequence of chemical building-block "letters", developing technology for reading (or sequencing) this chemical code has been fundamental to advances in biology and medicine.

Techniques that first enabled this were invented by Sanger in 1978, and were taken to massively parallel form by '454 Life Sciences' in 2003. This ushered in the current or "next-gen" era of genome sequencing technologies for research, medicine, and the emerging field of Genomic Personalized Medicine, in which healthcare is more fully informed by the individual's personal genetic makeup. If Sanger was the mainframe of sequencing, '454' was the minicomputer – smaller and faster and establishing the key guiding technical principals.

To further scale, reduce cost, and democratize the technology, I turned back to the developments of Noyce and Moore, and developed the first semiconductor-based sequencing technology to make it truly personal. We demonstrated this by sequencing the genome of Gordon Moore of Moore's Law fame.

This talk will discuss the evolution of semiconductor devices capable of performing DNA sequencing, and how the use of a scalable CMOS chip architecture allows for radical levels of economic scaling, and convenient new formats (from desktop to portable).

1.4 Quantum Computing – The Next Challenge in Circuit and System Design — 11:15 AM

Lieven Vandersypen
Antoni van Leeuwenhoek Professor, QuTech and Kavli Institute of NanoScience, TU Delft, The Netherlands

Quantum computers have the potential to tackle problems in materials science, chemistry, and mathematics that are well beyond the reach of supercomputers. Their power derives from the use of quantum bits, which can exist in arbitrary combinations of 0 and 1. This leads to a computing power that doubles with every additional quantum bit.

The challenge of quantum computing is that quantum bits are extremely fragile and their state is easily perturbed by environmental fluctuations. However, recent theoretical and experimental advances have made it clear that the resulting errors can in-principle be corrected. What it takes is a system containing thousands or millions of quantum bits operating at ultra-low temperatures, that must be interfaced using complex classical mixed-signal and microwave circuits for read-out and control. By comparison, today's practical demonstrations involve no more than a dozen quantum bits controlled by bulky instrumentation that is not scalable.

This talk will introduce the basic concepts behind quantum computing, summarize the state-of-the-art of solid-state implementations, and present the major open challenges in the realization of large-scale quantum circuits, including the design of dedicated classical control circuits and systems.

PRESENTATION TO PLENARY SPEAKERS **11:50 AM**

CONCLUSION **11:55 AM**

Power Amplifiers

Session Chair: ***Kohei Onizuka,*** *Toshiba, Kawasaki, Japan*
Associate Chair: ***Abbas Komijani,*** *Qualcomm, San Jose, CA*

1:30 PM

2.1 A 28GHz/37GHz/39GHz Multiband Linear Doherty Power Amplifier for 5G Massive MIMO Applications
S. Hu, F. Wang, H. Wang, Georgia Institute of Technology, Atlanta, GA

2:00 PM

2.2 A Fully Integrated Reconfigurable Wideband Envelope-Tracking SoC for High-Bandwidth WLAN Applications in a 28nm CMOS Technology
D. Chowdhury, S. R. Mundlapudi, A. Afsahi, Broadcom, San Diego, CA

2:30 PM

2.3 A Single-Inductor Dual-Output Converter with Linear-Amplifier-Driven Cross Regulation for Prioritized Energy-Distribution Control of Envelope-Tracking Supply Modulator
S-H. Yang [1], Y-T. Lin[1], Y-S. Ma[1], H-W. Chen[1], K-H. Chen[1], C-L. Wey[1], Y-H. Lin[2], S-R. Lin[2], T-Y. Tsai[2]
[1]National Chiao Tung University, Hsinchu, Taiwan
[2]Realtek Semiconductor, Hsinchu, Taiwan

Break 3:00 PM

3:15 PM

2.4 A 2.4V 23.9dBm 35.7%-PAE -32.1dBc-ACLR LTE-20MHz Envelope-Shaping-and-Tracking System with a Multiloop-Controlled AC-Coupling Supply Modulator and a Mode-Switching PA
X. Liu, H. Zhang, M. Zhao, X. Chen, P. K. T. Mok, H. C. Luong
Hong Kong University of Science and Technology, Hong Kong, China

3:45 PM

2.5 A High-Efficiency Multiband Class-F Power Amplifier in 0.153μm Bulk CMOS for WCDMA/LTE Applications
J. Ko, X. Guo, C. Cao, S. Rajapandian, S. Peng, J. Li, W. Lee, N. Baskaran, C. Wang
MediaTek, Austin, TX

4:00 PM

2.6 A SiGe BiCMOS E-Band Power Amplifier with 22% PAE at 18dBm OP_{1dB} and 8.5% at 6dB Back-Off Leveraging Current Clamping in a Common-Base Stage
J. Zhao[1,2], E. Rahimi[1], F. Svelto[1], A. Mazzanti[1]
[1]University of Pavia, Pavia, Italy; [2]now with HiSilicon-Technologies, Milan, Italy

4:15 PM

2.7 A Wideband 28GHz Power Amplifier Supporting 8×100MHz Carrier Aggregation for 5G in 40nm CMOS
S. Shakib[1], M. Elkholy[1], J. Dunworth[2], V. Aparin[2], K. Entesari[1]
[1]Texas A&M University, College Station, TX; [2]Qualcomm, San Diego, CA

4:30 PM

2.8 A Class-G Voltage-Mode Doherty Power Amplifier
V. Vorapipat, C. Levy, P. Asbeck, University of California, San Diego, CA

Conclusion 4:45 PM

Digital Processors

Session Chair: ***Thomas Burd,*** *AMD, Sunnyvale, CA*
Associate Chair: ***James Myers,*** *ARM, Cambridge, United Kingdom*

1:30 PM

3.1 POWER9™: A Processor Family Optimized for Cognitive Computing with 25Gb/s Accelerator Links and 16Gb/s PCIe Gen4

C. Gonzalez[1], E. Fluhr[2], D. Dreps[2], D. Hogenmiller[2], R. Rao[3], J. Paredes[2], M. Floyd[2], M. Sperling[4], R. Kruse[2], V. Ramadurai[2], R. Nett[2], S. Islam[2], J. Pille[5], D. Plass[4]
[1]IBM, Yorktown Heights, NY; [2]IBM, Austin, TX; [3]IBM, Bangalore, India; [4]IBM, Poughkeepsie, NY; [5]IBM, Boblingen, Germany

2:00 PM

3.2 Zen: A Next-Generation High-Performance x86 Core

DS1

T. Singh[1], S. Rangarajan[1], D. John[1], C. Henrion[2], S. Southard[1], H. McIntyre[3], A. Novak[1], S. Kosonocky[2], R. Jotwani[1], A. Schaefer[1], E. Chang[2], J. Bell[1], M. Co[1]
[1]AMD, Austin, TX; [2]AMD, Fort Collins, CO; [3]AMD, Sunnyvale, CA

2:30 PM

3.3 A 14nm 1GHz FPGA with 2.5D Transceiver Integration

D. Greenhill[1], R. Ho[1], D. Lewis[2], H. Schmit[1], K. H. Chan[1], A. Tong[1], S. Atsatt[1], D. How[1], P. McElheny[1], K. Duwel[1], J. Schulz[1], D. Faulkner[3], G. Iyer[1], G. Chen[1], H. K. Phoon[4], H. W. Lim[4], W-Y. Koay[4], T. Garibay[3]; [1]Intel, San Jose, CA; [2]Intel, Toronto, Canada; [3]Intel, Austin, TX; [4]Intel, Penang, Malaysia

Break 3:00 PM

3:15 PM

3.4 A 10nm FinFET 2.8GHz Tri-Gear Deca-Core CPU Complex with Optimized Power-Delivery Network for Mobile SoC Performance

H. Mair[1], E. Wang[2], A. Wang[2], P. Kao[2], Y. Tsai[2], S. Gururajarao[1], R. Lagerquist[1], J. Son[1], G. Gammie[1], G. Lin[2], A. Thippana[1], K. Li[1], M. Rahman[1], W. Kuo[2], D. Yen[2], Y-C. Zhuang[2], U. Fu[2], H-W. Wang[2], M. Peng[3], C-Y. Wu[2], T. Dosluoglu[4], A. Gelman[4], D. Dia[2], G. Gurumurthy[2], T. Hsieh[2], W. Lin[2], R. Tzeng[2], J. Wu[2], C. Wang[2], U. Ko[2]
[1]MediaTek, Austin, TX; [2]MediaTek, Hsinchu, Taiwan; [3]MediaTek, San Jose, CA
[4]Endura Technologies, San Diego, CA

3:45 PM

3.5 A 40nm Flash Microcontroller with 0.80µs Field-Oriented-Control Intelligent Motor Timer and Functional Safety System for Next-Generation EV/HEV

H. Kimura[1], H. Noda[1], H. Watanabe[1], T. Higuchi[1], R. Kobayashi[2], M. Utsuno[1], F. Takami[1], S. Otani[1], M. Ito[1], Y. Shimazaki[1], N. Yada[1], H. Kondo[1]
[1]Renesas Electronics, Tokyo, Japan; [2]Renesas System Design, Tokyo, Japan

4:15 PM

3.6 A 60pJ/b 300Mb/s 128×8 Massive MIMO Precoder-Detector in 28nm FD-SOI

H. Prabhu, J. N. Rodrigues, L. Liu, O. Edfors, Lund University, Lund, Sweden

4:45 PM

3.7 A 1920×1080 30fps 2.3TOPS/W Stereo-Depth Processor for Robust Autonomous Navigation

DS1

Z. Li, Q. Dong, M. Saligane, B. Kempke, S. Yang, Z. Zhang, R. Dreslinski, D. Sylvester, D. Blaauw, H. S. Kim
University of Michigan, Ann Arbor, MI

Conclusion 5:15 PM

Imagers

Session Chair: ***Hayato Wakabayashi,*** *Sony Electronics, San Jose, CA*
Associate Chair: ***Jun Deguchi,*** *Toshiba, Kawasaki, Japan*

1:30 PM

4.1 DS1 A 640×480 Dynamic Vision Sensor with a 9µm Pixel and 300Meps Address-Event Representation
B. Son[1], Y. Suh[1], S. Kim[1], H. Jung[1], J-S. Kim[1], C. Shin[1], K. Park[1], K. Lee[1], J. Park[1], J. Woo[1], Y. Roh[1], H. Lee[1], Y. Wang[2], I. Ovsiannikov[2], H. Ryu[1]
[1]Samsung Advanced Institute of Technology, Suwon, Korea; [2]Samsung Electronics, Pasadena, CA

2:00 PM

4.2 DS1 A Fully Integrated CMOS Fluorescence Biochip for Multiplex Polymerase Chain-Reaction (PCR) Processes
A. Hassibi, R. Singh, A. Manickam, R. Sinha, B. Kuimelis, S. Bolouki, P. Naraghi-Arani, K. Johnson, M. McDermott, N. Wood, P. Savalia, N. Gamini, InSilixa, Sunnyvale, CA

2:30 PM

4.3 A Programmable Sub-Nanosecond Time-Gated 4-Tap Lock-In Pixel CMOS Image Sensor for Real-Time Fluorescence Lifetime Imaging Microscopy
M-W. Seo, Y. Shirakawa, Y. Masuda, Y. Kawata, K. Kagawa, K. Yasutomi, S. Kawahito, Shizuoka University, Hamamatsu, Japan

2:45 PM

4.4 A Sub-nW 80mlx-to-1.26Mlx Self-Referencing Light-to-Digital Converter with AlGaAs Photodiode
W. Lim, D. Sylvester, D. Blaauw, University of Michigan, Ann Arbor, MI

Break 3:00 PM

3:15 PM

4.5 DS1 A 1.8e^-_{rms} Temporal Noise Over 110dB Dynamic Range 3.4µm Pixel Pitch Global Shutter CMOS Image Sensor with Dual-Gain Amplifiers, SS-ADC and Multiple-Accumulation Shutter
M. Kobayashi, Y. Onuki, K. Kawabata, H. Sekine, T. Tsuboi, Y. Matsuno, H. Takahashi, T. Koizumi, K. Sakurai, H. Yuzurihara, S. Inoue, T. Ichikawa, Canon, Kanagawa, Japan

3:45 PM

4.6 DS1 A 1/2.3inch 20Mpixel 3-Layer Stacked CMOS Image Sensor with DRAM
T. Haruta[1], T. Nakajima[1], J. Hashizume[1], T. Umebayashi[1], H. Takahashi[1], K. Taniguchi[1], M. Kuroda[1], H. Sumihiro[1], K. Enoki[1], T. Yamasaki[2], K. Ikezawa[1], A. Kitahara[1], M. Zen[1], M. Oyama[1], H. Koga[1], H. Tsugawa[1], T. Ogita[1], T. Nagano[1], S. Takano[3], T. Nomoto[1]
[1]Sony Semiconductor Solutions, Atsugi, Japan
[2]Sony Semiconductor Manufacturing, Atsugi, Japan; [3]Sony LSI Design, Atsugi, Japan

4:15 PM

4.7 DS1 A 2.1Mpixel Organic-Film Stacked RGB-IR Image Sensor with Electrically Controllable IR Sensitivity
S. Machida, S. Shishido, T. Tokuhara, M. Yanagida, T. Yamada, M. Izuchi, Y. Sato, Y. Miyake, M. Nakata, M. Murakami, M. Harada, Y. Inoue, Panasonic, Osaka, Japan

4:30 PM

4.8 A 0.44e-rms Read-Noise 32fps 0.5Mpixel High-Sensitivity RG-Less-Pixel CMOS Image Sensor Using Bootstrapping Reset
M-W. Seo[1], T. Wang[1], S-W. Jun[2], T. Akahori[2], S. Kawahito[1,2]
[1]Shizuoka University, Hamamatsu, Japan; [2]Brookman Technology, Hamamatsu, Japan

4:45 PM

4.9 DS1 A 1ms High-Speed Vision Chip with 3D-Stacked 140GOPS Column-Parallel PEs for Spatio-Temporal Image Processing
T. Yamazaki[1], H. Katayama[1], S. Uehara[1], A. Nose[1], M. Kobayashi[1], S. Shida[1], M. Odahara[2], K. Takamiya[2], Y. Hisamatsu[2], S. Matsumoto[2], L. Miyashita[3], Y. Watanabe[3], T. Izawa[1], Y. Muramatsu[1], M. Ishikawa[3]; [1]Sony Semiconductor Solutions, Atsugi, Japan; [2]Sony LSI Design, Atsugi, Japan
[3]University of Tokyo, Bunkyo, Japan

Conclusion 5:15 PM

Analog Techniques

Session Chair: ***Tim Piessens,*** *Icsense, Leuven, Belgium*
Associate Chair: ***Vadim Ivanov,*** *Texas Instruments, Tucson, AZ*

1:30 PM

5.1 DS1 **A 5×80W 0.004% THD+N Automotive Multiphase Class-D Audio Amplifier with Integrated Low-Latency ΔΣ ADCs for Digitized Feedback after the Output Filter**
F. Mostert[1], D. Schinkel[1,2], W. Groothedde[2], L. Breems[3], R. van Heeswijk[1], M-J. Koerts[1], E. van Iersel[1], D. Groeneveld[2], G. van Holland[1], P. Zeelen[1], D-J. Hissink[1], M. Pos[1], P. Wielage[1], F. Jorritsma[1], M. Klein Middelink[1]
[1]NXP Semiconductors, Nijmegen, The Netherlands
[2]Teledyne DALSA Semiconductors, Enschede, The Netherlands
[3]NXP Semiconductors, Eindhoven, The Netherlands

2:00 PM

5.2 **An 8Ω 10W 91%-Power-Efficiency 0.0023%-THD+N Multi-Level Class-D Audio Amplifier with Folded PWM**
J-H. Lee, J-S. Bang, K-D. Kim, H-D. Gwon, S-H. Park, Y. Huh, K-S. Yoon, J-B. Baek, Y-M. Ju, G. Lee, H. Park, H-M. Bae, G-H. Cho, KAIST, Daejeon, Korea

2:30 PM

5.3 DS1 **A 95µW 24MHz Digitally Controlled Crystal Oscillator for IoT Applications with 36nJ Start-Up Energy and >13× Start-Up Time Reduction Using a Fully-Autonomous Dynamically Adjusted Load**
M. Ding, Y-H. Liu, Y. Zhang, C. Lu, P. Zhang, B. Busze, C. Bachmann, K. Philips
Holst Centre / imec, Eindhoven, The Netherlands

2:45 PM

5.4 DS1 **Frequency-Locked-Loop Ring Oscillator with 3ns Peak-to-Peak Accumulated Jitter in 1ms Time Window for High-Resolution Frequency Counting**
K. Pappu, G. P. Reitsma, S. Bapat, Texas Instruments, Santa Clara, CA

Break 3:00 PM

3:15 PM

5.5 DS1 **A Quadrature Relaxation Oscillator with a Process-Induced Frequency-Error Compensation Loop**
J. Koo[1], K-S. Moon[2], B. Kim[1], H-J. Park[1], J-Y. Sim[1]
[1]Pohang University of Science and Technology, Pohang, Korea
[2]Research Institute of Industrial Science & Technology, Pohang, Korea

3:30 PM

5.6 **A 0.68nW/kHz Supply-Independent Relaxation Oscillator with ±0.49%/V and 96ppm/°C Stability**
A. Savanth[1,2], J. Myers[1], A. Weddell[2], D. Flynn[1,2], B. Al-Hashimi[2]
[1]ARM, Cambridge, United Kingdom; [2]University of Southampton, Southampton, United Kingdom

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5.7 DS1 **A 19nV/√Hz-Noise 2µV-Offset 75µA Low-Drift Capacitive-Gain Amplifier with Switched-Capacitor ADC Driving Capability**
H. Wang[1], G. Mora-Puchalt[2], C. Lyden[3], R. Maurino[4], C. Birk[3], [1]Analog Devices, Beijing, China
[2]Analog Devices, Valencia, Spain; [3]Analog Devices, Cork, Ireland; [4]Analog Devices, Turin, Italy

4:15 PM

5.8 **A 9.3nW All-in-One Bandgap Voltage and Current Reference Circuit**
Y. Ji, C. Jeon, H. Son, B. Kim, H-J. Park, J-Y. Sim
Pohang University of Science and Technology, Pohang, Korea

4:30 PM

5.9 **An 18.75µW Dynamic-Distributing-Bias Temperature Sensor with 0.87°C (3σ) Untrimmed Inaccuracy and 0.00946mm² Area**
Y-C. Hsu[1], C-L. Tai[1], M-C. Chuang[1], A. Roth[2], E. Soenen[2]; [1]TSMC, Hsinchu, Taiwan
[2]TSMC, Austin, TX

4:45 PM

5.10 **A 1A LDO Regulator Driven by a 0.0013mm² Class-D Controller**
W. Xu, P. Upadhyaya, X. Wang, R. Tsang, L. Lin, Marvell, Santa Clara, CA

5:00 PM

5.11 **A 65nm Inverter-Based Low-Dropout Regulator with Rail-to-Rail Regulation and over -20dB PSR at 0.2V Lowest Supply Voltage**
F. Yang, P. K. T. Mok, Hong Kong University of Science and Technology, Hong Kong, China

Conclusion 5:15 PM

Ultra-High-Speed Wireline

Session Chair: ***Simone Erba,*** *STMicroelectronics, Pavia, Italy*
Associate Chair: ***Takayuki Shibasaki,*** *Fujitsu Laboratories, Kawasaki, Japan*

1:30 PM

6.1 A 56Gb/s PAM-4/NRZ Transceiver in 40nm CMOS
P-J. Peng, J-F. Li, L-Y. Chen, J. Lee
National Taiwan University, Taipei, Taiwan

2:00 PM

6.2 A 60Gb/s 288mW NRZ Transceiver with Adaptive Equalization and Baud-Rate Clock and Data Recovery in 65nm CMOS Technology
J. Han[1], Y. Lu[2], N. Sutardja[1], E. Alon[1]
[1]University of California, Berkeley, CA
[2]Qualcomm Atheros, San Jose, CA

2:30 PM

6.3 DS1 A 40-to-56Gb/s PAM-4 Receiver with 10-Tap Direct Decision-Feedback Equalization in 16nm FinFET
J. Im[1], D. Freitas[1], A. Roldan[2], R. Casey[3], S. Chen[1], A. Chou[1], T. Cronin[1], K. Geary[3], S. McLeod[1], L. Zhou[1], I. Zhuang[1], J. Han[4], S. Lin[4], P. Upadhyaya[1], G. Zhang[1], Y. Frans[1], K. Chang[1],
[1]Xilinx, San Jose, CA
[2]Xilinx, Singapore, Singapore
[3]Xilinx, Cork, Ireland
[4]University of California, Berkeley, CA

Break 3:00 PM

3:15 PM

6.4 A 64Gb/s PAM-4 Transmitter with 4-Tap FFE and 2.26pJ/b Energy Efficiency in 28nm CMOS FDSOI
G. Steffan[1], E. Depaoli[1], E. Monaco[1], N. Sabatino[1], W. Audoglio[1], A. A. Rossi[1], S. Erba[1], M. Bassi[2], A. Mazzanti[2]
[1]STMicroelectronics, Pavia, Italy
[2]University of Pavia, Pavia, Italy

3:45 PM

6.5 A 1.8pJ/b 56Gb/s PAM-4 Transmitter with Fractionally Spaced FFE in 14nm CMOS
T. O. Dickson, H. A. Ainspan, M. Meghelli
IBM T. J. Watson Research Center, Yorktown Heights, NY

4:15 PM

6.6 A 22.5-to-32Gb/s 3.2pJ/b Referenceless Baud-Rate Digital CDR with DFE and CTLE in 28nm CMOS
W. Rahman[1], D. Yoo[1], J. Liang[1], A. Sheikholeslami[1], H. Tamura[2], T. Shibasaki[2], H. Yamaguchi[2]
[1]University of Toronto, Toronto, Canada
[2]Fujitsu Laboratories, Kawasaki, Japan

4:45 PM

6.7 A 28Gb/s Digital CDR with Adaptive Loop Gain for Optimum Jitter Tolerance
J. Liang[1], A. Sheikholeslami[1], H. Tamura[2], Y. Ogata[2], H. Yamaguchi[2]
[1]University of Toronto, Toronto, Canada
[2]Fujitsu Laboratories, Kawasaki, Japan

Conclusion 5:15 PM

Demonstration Session 1, Monday February 6th, 5:00-7:00 PM

This year, the Demonstration Session extending in selected regular papers, both Academic and Industrial, will take place on Monday February 6th, and Tuesday February 7th, from 5 pm until 7 pm in the Golden Gate Hall. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2017, as noted by the symbol **DS1**

3.2 Zen: A Next-Generation High-Performance x86 Core

3.7 A 1920×1080 30fps 2.3TOPS/W Stereo-Depth Processor for Robust Autonomous Navigation

4.1 A 640×480 Dynamic Vision Sensor with a 9μm Pixel and 300Meps Address-Event Representation

4.2 A Fully Integrated CMOS Fluorescence Biochip for Multiplex Polymerase Chain-Reaction (PCR) Processes

4.5 A $1.8e^-_{rms}$ Temporal Noise Over 110dB Dynamic Range 3.4μm Pixel Pitch Global Shutter CMOS Image Sensor with Dual-Gain Amplifiers, SS-ADC and Multiple-Accumulation Shutter

4.6 A 1/2.3in 20Mpixel 3-Layer Stacked CMOS Image Sensor with DRAM

4.7 A 2.1Mpixel Organic-Film Stacked RGB-IR Image Sensor with Electrically Controllable IR Sensitivity

4.9 A 1ms High-Speed Vision Chip with 3D-Stacked 140GOPS Column-Parallel PEs for Spatio-Temporal Image Processing

5.1 A 5×80W 0.004% THD+N Automotive Multiphase Class-D Audio Amplifier with Integrated Low-Latency ΔΣ ADCs for Digitized Feedback after the Output Filter

5.3 A 95μW 24MHz Digitally Controlled Crystal Oscillator for IoT Applications with 36nJ Start-Up Energy and >13× Start-Up Time Reduction Using a Fully-Autonomous Dynamically Adjusted Load

5.4 Frequency-Locked-Loop Ring Oscillator with 3ns Peak-to-Peak Accumulated Jitter in 1ms Time Window for High-Resolution Frequency Counting

5.5 A Quadrature Relaxation Oscillator with a Process-Induced Frequency-Error Compensation Loop

5.7 A 19nV/√Hz-Noise 2μV-Offset 75μA Low-Drift Capacitive-Gain Amplifier with Switched-Capacitor ADC Driving Capability

6.3 A 40-to-56Gb/s PAM-4 Receiver with 10-Tap Direct Decision-Feedback Equalization in 16nm FinFET

7.4 A 915MHz Asymmetric Radio Using Q-Enhanced Amplifier for a Fully Integrated 3×3×3mm^3 Wireless Sensor Node with 20m Non-Line-of-Sight Communication

7.5 A TCXO-Less 100Hz-Minimum-Bandwidth Transceiver for Ultra-Narrow-Band Sub-GHz IoT Cellular Networks

7.7 A 118mW 23.3GS/s Dual-Band 7.3GHz and 8.7GHz Impulse-Based Direct RF Sampling Radar SoC in 55nm CMOS

8.1 Improved Power-Side-Channel-Attack Resistance of an AES-128 Core via a Security-Aware Integrated Buck Voltage Regulator

9.2 A 0.6nJ -0.22/+0.19°C Inaccuracy Temperature Sensor Using Exponential Subthreshold Oscillation Dependence

9.5 A 1.8V True-Differential 140dB SPL Full-Scale Standard CMOS MEMS Digital Microphone Exhibiting 67dB SNR

9.6 A 3.9kHz-Frame-Rate Capacitive Touch System with Pressure/Tilt Angle Expressions of Active Stylus Using Multiple-Frequency Driving Method for 65" 104×64 Touch Screen Panel

9.7 A 6.9mW 120fps 28×50 Capacitive Touch Sensor with 41.7dB SNR for 1mm Stylus Using Current-Driven ΔΣ ADCs

10.2 A Digitally Controlled 94.8%-Peak-Efficiency Hybrid Switched-Capacitor Converter for Bidirectional Balancing and Impedance-Based Diagnostics of Lithium-Ion Battery Arrays

10.3 A 94.2%-Peak-Efficiency 1.53A Direct-Battery-Hook-Up Hybrid Dickson Switched-Capacitor DC-DC Converter with Wide Continuous Conversion Ratio in 65nm CMOS

EE3: Quantum Engineering: Hype, Spin or Reality?

Organizer/ Moderator: Edoardo Charbon, *Delft University of Technology Delft, The Netherlands and EPFL, Lausanne, Switzerland*

Quantum engineering is an emerging discipline, which involves studies of materials, devices, circuits, and architectures that are necessary to develop quantum-based systems. Recently, quantum computing has received significant attention, and large investments have been made in this field. Is this interest pure hype, or should we revise our views on computing? This Panel will address this question as well as various others: is our current understanding of classical electronics sufficient for the challenges ahead or should we all rethink the way we design circuits and systems? Will quantum engineering ultimately emerge as the next wave in research and products or will the economy of scale continue to rule? Will Moore's Law compete with, or enable, new quantum technologies?

Panelists

James S. Clarke, *Intel, Hillsboro, OR*
Kenneth Shepard, *Columbia University, NewYork, NY*
Lieven Vandersypen, *Delft University of Technology, Delft, The Netherlands*
Francesco Regazzoni, *University of Lugano, Lugano, Switzerland*
Andrea Morello, *University of New South Wales, Sydney, Australia*
Yoshihisa Yamamoto, *Japan Science and Technology Agency, Tokyo, Japan*

EE4: Semiconductor Economics: How Business Decisions are Engineered

Organizers: **Ichiro Fujimori,** *Broadcom, Irvine, CA*
Pavan Hanumolu, *University of Illinois, Champaign, IL*

Chair: **Ichiro Fujimori,** *Broadcom, Irvine, CA*

This Evening Session is not about circuits or chip architectures; rather it is a technical session on economics driving the semiconductor industry. Business leaders (CEOs, CFOs, VCs, Investors) use very sophisticated financial engineering and analysis tools to make decisions that sometimes do not appear to make sense to designers working in the technology trenches. In this evening session, several eminent speakers from the business community will present various behind-the-scenes technological and business aspects that lead to decisions which can have a profound impact on both the technology and the lives of circuit designers.

Time	Topic
8:00 PM	**Introduction**
8:05 PM	**"Can't We All Just Get Along?" The Challenge in Managing Expectations of Disparate Stakeholders** **Adam Spice,** *Maxlinear Corporation, Carlsbad, CA*
8:30 PM	**Boom vs. Bust: Valuation Methods for Technology Companies from Seed Round to Exit** **Armond Hairapetian,** *Miramar Ventures, Newport Beach, CA*
8:55 PM	**Semiconductor Startups & the IP Challenge: Build, Buy, Borrow, or Burn** **Ravi Subramanian,** *Mentor Graphics Corporation, San Jose, CA*
9:20 PM	**While Searching for the "Indies" You Discover the "New World": How to Manage and Finance Long Term Breakthroughs in the Semiconductor Industry** **Domenico Rossi,** *ST Microelectronics, Milan, Italy*

Wireless Transceivers

Session Chair: ***Yuu Watanabe,*** *Waseda University, Kitakyushu, Japan*
Associate Chair: ***Danielle Griffith,*** *Texas Instruments, Dallas, TX*

8:30 AM

7.1 An 802.11ac Dual-Band Reconfigurable Transceiver Supporting up to Four VHT80 Spatial Streams with 116fs$_{rms}$-Jitter Frequency Synthesizer and Integrated LNA/PA Delivering 256QAM 19dBm per Stream Achieving 1.733Gb/s PHY Rate

T-M. Chen[1], Y. Lu[1], P-N. Chen[1], Y-H. Chang[1], M-C. Liu[1], P-Y. Chang[1], C-J. Liang[1], Y-C. Chen[1], H-L. Lu[1], J-Y. Ding[1], C-C. Wang[1], Y-L. Hsueh[1], J-C. Tsai[1], M-S. Hsu[1], Y-H. Chung[1], G. Chien[2], [1]MediaTek, Hsinchu, Taiwan; [2]MediaTek, San Jose, CA

9:00 AM

7.2 A 28GHz 32-Element Phased-Array Transceiver IC with Concurrent Dual Polarized Beams and 1.4 Degree Beam-Steering Resolution for 5G Communication

B. Sadhu[1], Y. Tousi[1], J. Hallin[2], S. Sahl[3], S. Reynolds[1], Ö. Renström[3], K. Sjögren[2], O. Haapalahti[3], N. Mazor[4], B. Bokinge[3], G. Weibull[2], H. Bengtsson[3], A. Carlinger[3], E. Westesson[5], J-E. Thillberg[3], L. Rexberg[3], M. Yeck[1], X. Gu[1], D. Friedman[1], A. Valdes-Garcia[1], [1]IBM T. J. Watson Research Center, Yorktown Heights, NY
[2]Ericsson, Lindholmen, Sweden; [3]Ericsson, Kista, Sweden
[4]IBM Research, Haifa, Israel; [5]Ericsson, Lund, Sweden

9:30 AM

7.3 A 40nm Low-Power Transceiver for LTE-A Carrier Aggregation

C-S. Chiu[1], S-C. Yen[1], C-Y. Yu[1], T-H. Wu[1], C-Y. Chou[1], S-C. Tseng[1], C-H. Shen[1], Y-T. Lu[1], H. Chen[1], S-Y. Yang[1], Y-T. Chen[1], G-K. Dehng[1], Y. Chen[2], C. Beghein[2], D. Nalbantis[2], M. Collados[2], B. Tenbroek[2], J. Strange[2], C. Wang[3]
[1]MediaTek, Hsinchu, Taiwan; [2]MediaTek, Kent, United Kingdom; [3]MediaTek, Austin, TX

Break 10:00 AM

10:15 AM

7.4 DS1 A 915MHz Asymmetric Radio Using Q-Enhanced Amplifier for a Fully Integrated 3×3×3mm^3 Wireless Sensor Node with 20m Non-Line-of-Sight Communication

L-X. Chuo[1], Y. Shi[1], Z. Luo[1], N. Chiotellis[1], Z. Foo[1,2], G. Kim[1,2], Y. Kim[1,2], A. Grbic[1], D. Wentzloff[1], H-S. Kim[1], D. Blaauw[1]
[1]University of Michigan, Ann Arbor, MI; [2]CubeWorks, Ann Arbor, MI

10:45 AM

7.5 DS1 A TCXO-Less 100Hz-Minimum-Bandwidth Transceiver for Ultra-Narrow-Band Sub-GHz IoT Cellular Networks

D. Lachartre[1], F. Dehmas[1], C. Bernier[1], C. Fourtet[2], L. Ouvry[1], F. Lepin[1], E. Mercier[1], S. Hamard[2], L. Zirphile[2], S. Thuries[1], F. Chaix[1]
[1]CEA-LETI-MINATEC, Grenoble, France; [2]Sigfox, Labège, France

11:15 AM

7.6 A +8dBm BLE/BT Transceiver with Automatically Calibrated Integrated RF Bandpass Filter and -58dBc TX HD2

W. Yang, D. Y. Hu, C. K. Lam, J. Q. Cui, L. K. Soh, D. C. Song, X. W. Zhong, H. C. Hor, C. L. Heng, MediaTek, Singapore, Singapore

11:45 AM

7.7 DS1 A 118mW 23.3GS/s Dual-Band 7.3GHz and 8.7GHz Impulse-Based Direct RF Sampling Radar SoC in 55nm CMOS

N. Andersen[1], K. Granhaug[1], J. A. Michaelsen[1], S. Bagga[1], H. A. Hjortland[1], M. R. Knutsen[1], T. S. Lande[2], D. T. Wisland[1,2], [1]Novelda AS, Oslo, Norway
[2]University of Oslo, Oslo, Norway

Conclusion 12:15 PM

Digital PLLs and Security Circuits

Session Chair: ***Yasuhisa Shimazaki,*** *Renesas Electronics, Tokyo, Japan*
Associate Chair: ***John Maneatis,*** *True Circuits, Los Altos, CA*

8:30 AM

8.1 Improved Power-Side-Channel-Attack Resistance of an AES-128 Core via a Security-Aware Integrated Buck Voltage Regulator DS1
M. Kar[1], A. Singh[1], S. Mathew[2], A. Rajan[2], V. De[2], S. Mukhopadhyay[1]
[1]Georgia Institute of Technology, Atlanta, GA
[2]Intel, Hillsboro, OR

9:00 AM

8.2 8Mb/s 28Mb/mJ Robust True-Random-Number Generator in 65nm CMOS Based on Differential Ring Oscillator with Feedback Resistors
E. Kim, M. Lee, J-J. Kim
Pohang University of Science and Technology, Pohang, Korea

9:30 AM

8.3 A 553F² 2-Transistor Amplifier-Based Physically Unclonable Function (PUF) with 1.67% Native Instability
K. Yang, Q. Dong, D. Blaauw, D. Sylvester
University of Michigan, Ann Arbor, MI

Break 10:00 AM

10:15 AM

8.4 A 2.5ps 0.8-to-3.2GHz Bang-Bang Phase- and Frequency-Detector-Based All-Digital PLL with Noise Self-Adjustment
T. Jang[1], S. Jeong[1], D. Jeon[2], K. D. Choo[1], D. Sylvester[1], D. Blaauw[1]
[1]University of Michigan, Ann Arbor, MI
[2]Seoul National University, Seoul, Korea

10:45 AM

8.5 A 0.42ps-Jitter -241.7dB-FOM Synthesizable Injection-Locked PLL with Noise-Isolation LDO
H. C. Ngo, K. Nakata, T. Yoshioka, Y. Terashima, K. Okada, A. Matsuzawa
Tokyo Institute of Technology, Tokyo, Japan

11:15 AM

8.6 A 2.5-to-5.75GHz 5mW 0.3ps$_{rms}$-Jitter Cascaded Ring-Based Digital Injection-Locked Clock Multiplier in 65nm CMOS
D. Coombs, A. Elkholy, R. K. Nandwana, A. Elmallah, P. K. Hanumolu
University of Illinois, Urbana, IL

11:45 AM

8.7 A 0.0047mm² Highly Synthesizable TDC- and DCO-Less Fractional-N PLL with a Seamless Lock Range of f_{REF} to 1GHz
H. Cho[1], K. Seong[1], K-H. Choi[2], J-H. Choi[2], B. Kim[1], H-J. Park[1], J-Y. Sim[1]
[1]Pohang University of Science and Technology, Pohang, Korea
[2]Samsung Electronics, Hwaseong, Korea

Conclusion 12:15 PM

Sensors

Session Chair: ***Pedram Lajevardi,*** *Bosch Research and Technology Center, Palo Alto, CA*
Associate Chair: ***Masayuki Miyamoto,*** *Sharp, Nara, Japan*

8:30 AM

9.1 A Resistor-Based Temperature Sensor with a 0.13pJ·K² Resolution FOM
S. Pan[1], Y. Luo[1,2], S. H. Shalmany[1,3], K. A. Makinwa[1]
[1]Delft University of Technology, Delft, The Netherlands
[2]Ulm University, Ulm, Germany; [3]Broadcom, Bunnik, The Netherlands

9:00 AM

9.2 DS1 A 0.6nJ -0.22/+0.19°C Inaccuracy Temperature Sensor Using Exponential Subthreshold Oscillation Dependence
K. Yang, Q. Dong, W. Jung, Y. Zhang, M. Choi, D. Blaauw, D. Sylvester
University of Michigan, Ann Arbor, MI

9:15 AM

9.3 A BJT-Based Temperature Sensor with a Packaging-Robust Inaccuracy of ±0.3°C (3σ) from -55°C to +125°C After Heater-Assisted Voltage Calibration
B. Yousefzadeh, K. A. A. Makinwa, Delft University of Technology, Delft, The Netherlands

9:30 AM

9.4 A 27µW 0.06mm² Background Resonance Frequency Tuning Circuit Based on Noise Observation for a 1.71mW CT-ΔΣ MEMS Gyroscope Readout System with 0.9°/h Bias Instability
M. Marx[1], D. De Dorigo[1], S. Nessler[1], S. Rombach[2], M. Maurer[2], Y. Manoli[1,2]
[1]University of Freiburg - IMTEK, Freiburg, Germany
[2]Hahn-Schickard, Villingen-Schwenningen, Germany

Break 10:00 AM

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9.5 DS1 A 1.8V True-Differential 140dB SPL Full-Scale Standard CMOS MEMS Digital Microphone Exhibiting 67dB SNR
E. Bach, R. Gaggl, L. Sant, C. Buffa, S. Stojanovic, D. Straeussnigg, A. Wiesbauer
Infineon Technologies, Villach, Austria

10:30 AM

9.6 DS1 A 3.9kHz-Frame-Rate Capacitive Touch System with Pressure/Tilt Angle Expressions of Active Stylus Using Multiple-Frequency Driving Method for 65" 104×64 Touch Screen Panel
J-S. An[1], S-H. Han[2], J. E. Kim[3], D-H. Yoon[3], Y-H. Kim[2], H-H. Hong[2], J-H. Ye[4], S-J. Jung[1], S-H. Lee[1], J-Y. Jeong[1], K-H. Baek[3], S-K. Hong[1], O-K. Kwon[1]
[1]Hanyang University, Seoul, Korea; [2]Leading UI, Anyang, Korea
[3]Chung-Ang University, Seoul, Korea; [4]MiraeTNS, Cheongju, Korea

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9.7 DS1 A 6.9mW 120fps 28×50 Capacitive Touch Sensor with 41.7dB SNR for 1mm Stylus Using Current-Driven ΔΣ ADCs
H. Hwang[1], H. Lee[1], H. Kim[2], Y. Chae[1], [1]Yonsei University, Seoul, Korea; [2]TRAIS, Ansan, Korea

11:15 AM

9.8 An Energy-Efficient 3.7nV/√Hz Bridge-Readout IC with a Stable Bridge Offset Compensation Scheme
H. Jiang, K. A. Makinwa, S. Nihtianov, Delft University of Technology, Delft, The Netherlands

11:45 AM

9.9 A 0.6nm Resolution 19.8mW Eddy-Current Displacement Sensor Interface with 126MHz Excitation
V. Chaturvedi[1], M. R. Nabavi[2], J. Vogel[1], K. A. Makinwa[1], S. Nihtianov[1]
[1]Delft University of Technology, Delft, The Netherlands
[2]Catena Microelectronics, Delft, The Netherlands

Conclusion 12:15 PM

DC-DC Converters

Session Chair: ***Hoi Lee,*** *University of Texas at Dallas, Richardson, TX*
Associate Chair: ***Gerard Villar Pique,*** *NXP Semiconductors, Eindhoven, The Netherlands*

8:30 AM

10.1 A 1.1W/mm²-Power-Density 82%-Efficiency Fully Integrated 3:1 Switched-Capacitor DC-DC Converter in Baseline 28nm CMOS Using Stage Outphasing and Multiphase Soft-Charging
N. Butzen, M. Steyaert, KU Leuven, Leuven, Belgium

9:00 AM

10.2 DS1 A Digitally Controlled 94.8%-Peak-Efficiency Hybrid Switched-Capacitor Converter for Bidirectional Balancing and Impedance-Based Diagnostics of Lithium-Ion Battery Arrays
C. Schaef[1,2], E. Din[1,3], J. T. Stauth[1]
[1]Dartmouth College, Hanover, NH; [2]Intel, Hillsboro, OR
[3]Hive Battery Management, Seattle, WA

9:30 AM

10.3 DS1 A 94.2%-Peak-Efficiency 1.53A Direct-Battery-Hook-Up Hybrid Dickson Switched-Capacitor DC-DC Converter with Wide Continuous Conversion Ratio in 65nm CMOS
W-C. Liu, P. Assem, Y. Lei, P. Kumar Hanumolu, R. Pilawa-Podgurski
University of Illinois, Urbana, IL

9:45 AM

10.4 A Hybrid Inductor-Based Flying-Capacitor-Assisted Step-Up/Step-Down DC-DC Converter with 96.56% Efficiency
Y-M. Ju, S-U. Shin, Y. Huh, S-H. Park, J-S. Bang, K-D. Kim, S-W. Choi, J-H. Lee, G-H. Cho, KAIST, Daejeon, Korea

Break 10:00 AM

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10.5 A Three-Level Single-Inductor Triple-Output Converter with an Adjustable Flying-Capacitor Technique for Low Output Ripple and Fast Transient Response
L-C. Chu[1], W-H. Yang[1], X-Q. Zhang[1], Y-J. Lai[1], K-H. Chen[1], C-L. Wey[1], Y-H. Lin[2], S-R. Lin[2], T-Y. Tsai[2]
[1]National Chiao Tung University, Hsinchu, Taiwan
[2]Realtek Semiconductor, Hsinchu, Taiwan

10:45 AM

10.6 A 30MHz Hybrid Buck Converter with 36mV Droop and 125ns 1% Settling Time for a 1.25A/2ns Load Transient
L. Cheng, W-H. Ki
Hong Kong University of Science and Technology, Hong Kong, China

11:15 AM

10.7 A 25MHz 4-Phase SAW Hysteretic DC-DC Converter with 1-Cycle APC Achieving 190ns t_{settle} to 4A Load Transient and Above 80% Efficiency in 96.7% of the Power Range
B. Lee, M. K. Song, A. Maity, D. B. Ma, University of Texas at Dallas, Richardson, TX

11:45 AM

10.8 A Buck Converter with 240pW Quiescent Power, 92% Peak Efficiency and a 2×10^6 Dynamic Range
A. Paidimarri[1,2], A. P. Chandrakasan[2]
[1]IBM T. J. Watson Research Center, Yorktown Heights, NY
[2]Massachusetts Institute of Technology, Cambridge, MA

Conclusion 12:15 PM

Nonvolatile Memory Solutions

Session Chair: ***Takashi Kono,*** *Renesas Electronics, Tokyo, Japan*
Associate Chair: ***Ki-Tae Park,*** *Samsung Electronics, Hwasung, Korea*

8:30 AM

11.1 A 512Gb 3b/Cell Flash Memory on 64-Word-Line-Layer BiCS Technology

R. Yamashita[1], S. Magia[1], T. Higuchi[2], K. Yoneya[2], T. Yamamura[2], H. Mizukoshi[1], S. Zaitsu[1], M. Yamashita[1], S. Toyama[1], N. Kamae[1], J. Lee[1], S. Chen[1], J. Tao[1], W. Mak[1], X. Zhang[1], Y. Yu[1], Y. Utsunomiya[2], Y. Kato[1], M. Sakai[1], M. Matsumoto[1], H. Chibvongodze[1], N. Ookuma[1], H. Yabe[1], S. Taigor[1], R. Samineni[1], T. Kodama[2], Y. Kamata[2], Y. Namai[2], J. Huynh[1], S-E. Wang[1], Y. He[1], T. Pham[1], V. Saraf[1], A. Petkar[1], M. Watanabe[1], K. Hayashi[1], P. Swarnkar[1], H. Miwa[1], A. Pradhan[1], S. Dey[1], D. Dwibedy[1], T. Xavier[1], M. Balaga[1], S. Agarwal[1], S. Kulkarni[1], Z. Papasaheb[1], S. Deora[1], P. Hong[1], M. Wei[1], G. Balakrishnan[1], T. Ariki[1], K. Verma[1], C. Siau[1], Y. Dong[1], C-H. Lu[1], T. Miwa[1], F. Moogat[1]

[1]Western Digital, Milpitas, CA
[2]Toshiba, Yokohama, Japan

9:00 AM

11.2 A 1Mb Embedded NOR Flash Memory with 39µW Program Power for mm-Scale High-Temperature Sensor Nodes

Q. Dong[1], Y. Kim[1], I. Lee[1], M. Choi[1], Z. Li[1], J. Wang[1], K. Yang[1], Y-P. Chen[1], J. Dong[1], M. Cho[1], G. Kim[1], W-K. Chang[2], Y-S. Chen[2], Y-D. Chih[2], D. Blaauw[1], D. Sylvester[1]

[1]University of Michigan, Ann Arbor, MI
[2]TSMC, Hsinchu, Taiwan

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11.3 A 10nm 32Kb Low-Voltage Logic-Compatible Anti-Fuse One-Time-Programmable Memory with Anti-Tampering Sensing Scheme

S-Y. Chou, Y-S. Chen, J-H. Chang, Y-D. Chih, T-Y. J. Chang
TSMC Design Technology, Hsinchu, Taiwan

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11.4 A 512Gb 3b/cell 64-Stacked WL 3D V-NAND Flash Memory

C. Kim, J-H. Cho, W. Jeong, I-H. Park, H-W. Park, D-H. Kim, D. Kang, S. Lee, J-S. Lee, W. Kim, J. Park, Y-L. Ahn, J. Lee, J-H. Lee, S. Kim, H-J. Yoon, J. Yu, N. Choi, Y. Kwon, N. Kim, H. Jang, J. Park, S. Song, Y. Park, J. Bang, S. Hong, B. Jeong, H-J. Kim, C. Lee, Y-S. Min, I. Lee, I-M. Kim, S-H. Kim, D. Yoon, K-S. Kim, Y. Choi, M. Kim, H. Kim, P. Kwak, J-D. Ihm, D-S. Byeon, J-Y. Lee, K-T. Park, K-H. Kyung
Samsung Electronics, Hwasung, Korea

Break 10:00 AM

SRAM

Session Chair: ***Fatih Hamzaoglu,*** *Intel, Hillsboro, OR*
Associate Chair: ***Chun Shiah,*** *Etron, Hsinchu, Taiwan*

10:15 AM

12.1 A 7nm 256Mb SRAM in High-K Metal-Gate FinFET Technology with Write-Assist Circuitry for Low-V_{MIN} Applications

J. Chang[1], Y-H. Chen[1], W-M. Chan[1], S. P. Singh[1], H. Cheng[1], H. Fujiwara[1], J-Y. Lin[1], K-C. Lin[1], J. Hung[1], R. Lee[1], H-J. Liao[1], J-J. Liaw[2], Q. Li[2], C-Y. Lin[2], M-C. Chiang[2], S-Y. Wu[2]
[1]TSMC Design Technology, Hsinchu, Taiwan
[2]TSMC, Hsinchu, Taiwan

10:45 AM

12.2 A 7nm FinFET SRAM Macro Using EUV Lithography for Peripheral Repair Analysis

T. Song, H. Kim, W. Rim, Y. Kim, S. Park, C. Park, M. Hong, G. Yang, J. Do, J. Lim, S. Lee, I. Kim, S. Baek, J. Jung, D. Ha, H. Jang, T. Lee, C-H. Park, B. Kwon, H. Jung, S. Cho, Y. Choo, J. Choi
Samsung Electronics, Hwasung, Korea

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12.3 A Low-Power and High-Performance 10nm SRAM Architecture for Mobile Applications

M. Clinton[1], H. Cheng[2], H. Liao[2], R. Lee[2], C-W. Wu[2], J. Yang[2], H-T. Hsieh[2], F. Wu[2], J-P. Yang[2], A. Katoch[3], A. Achyuthan[3], D. Mikan[1], B. Sheffield[1], J. Chang[2]
[1]TSMC Design Technology, Austin, TX
[2]TSMC Design Technology, Hsinchu, Taiwan
[3]TSMC Design Technology, Ottawa, Canada

11:45 AM

12.4 1.4Gsearch/s 2Mb/mm² TCAM Using Two-Phase-Precharge ML Sensing and Power-Grid Pre-Conditioning to Reduce Ldi/dt Power-Supply Noise by 50%

I. Arsovski[1], M. Fragano[1], R. M. Houle[1], A. Patil[1], V. Butler[1,2], R. Kim[3], R. Rodriguez[1], T. Maffitt[4], J. J. Oler[1], J. Goss[1], C. Parkinson[5,6], M. A. Ziegerhofer[1], S. Burns[1]
[1]Globalfoundries, Essex Junction, VT
[2]Green Mountain Semiconductor, Burlington, VT
[3]Globalfoundries, Endicott, NY
[4]IBM Research, Essex Junction, VT
[5]Globalfoundries, Raleigh, NC
[6]ASIC North, Raleigh, NC

Conclusion 12:15 PM

High-Performance Transmitters

Session Chair: ***Guang-Kaai Dehng,*** *MediaTek, Hsinchu, Taiwan*
Associate Chair: ***Kyoohyun Lim,*** *FCI, Seongnam, Korea*

1:30 PM

13.1 A Fully Integrated Multimode Front-End Module for GSM/EDGE/TD-SCDMA/TD-LTE Applications Using a Class-F CMOS Power Amplifier

M-D. Tsai[1], C-C. Lin[1], P-Y. Chen[1], T-Y. Chang[1], C-W. Tseng[1], L-C. Lin[1], C. Beale[2], B. Tseng[1], B. Tenbroek[2], C-S. Chiu[1], G-K. Dehng[1], G. Chien[3]
[1]MediaTek, Hsinchu, Taiwan; [2]MediaTek, Kent, United Kingdom; [3]MediaTek, San Jose, CA

2:00 PM

13.2 A Digital Multimode Polar Transmitter Supporting 40MHz LTE Carrier Aggregation in 28nm CMOS

M. Fulde[1], A. Belitzer[1], Z. Boos[1], M. Bruennert[1], J. Fritzin[1], H. Geltinger[2], M. Groinig[3], D. Gruber[3], S. Gruenberger[3], T. Hartig[3], V. Kampus[3], B. Kapfelsberger[1], F. Kuttner[3], S. Leuschner[1], T. Maletz[1], A. Menkhoff[1], J. Moreira[1], A. Paussa[3], D. Ponton[3], H. Pretl[4], D. Sira[1], U. Steinacker[1], N. Stevanovic[1]
[1]Intel, Neubiberg, Germany; [2]DPMA, Munich, Germany; [3]Intel, Villach, Austria; [4]DMCE, Linz, Austria

2:15 PM

13.3 A SAW-Less Reconfigurable Multimode Transmitter with a Voltage-Mode Harmonic-Reject Mixer in 14nm FinFET CMOS

V. Bhagavatula[1], D. Kwon[2], J. Lee[2], Q-D. Bui[2], J-H. Choi[2], S-I. Lu[1], S. Son[1]
[1]Samsung Semiconductor, San Jose, CA; [2]Samsung Electronics, Gyeongii-do, Korea

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13.4 All-Digital RF Transmitter in 28nm CMOS with Programmable RX-Band Noise Shaping

E. Roverato[1], M. Kosunen[1], K. Cornelissens[2], S. Vatti[2], P. Stynen[2], K. Bertrand[2], T. Korhonen[2], H. Samsom[2], P. Vandenameele[2], J. Ryynänen[1]
[1]Aalto University, Espoo, Finland; [2]Huawei Technologies, Leuven, Belgium

Break 3:00 PM

3:15 PM

13.5 A 0.35-to-2.6GHz Multilevel Outphasing Transmitter with a Digital Interpolating Phase Modulator Enabling up to 400MHz Instantaneous Bandwidth

M. Kosunen[1], J. Lemberg[1], M. Martelius[1], E. Roverato[1], T. Nieminen[1], M. Englund[1], K. Stadius[1], L. Anttila[2], J. Pallonen[3], M. Valkama[2], J. Ryynänen[1], [1]Aalto University, Espoo, Finland
[2]Tampere University of Technology, Tampere, Finland; [3]Nokia, Espoo, Finland

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13.6 A 2.4GHz WLAN Digital Polar Transmitter with Synthesized Digital-to-Time Converter in 14nm Trigate/FinFET Technology for IoT and Wearable Applications

P. Madoglio[1], H. Xu[1,2], K. Chandrashekar[1], L. Cuellar[1], M. Faisal[1,3], W. Y. Li[1], H. S. Kim[1], K. M. Nguyen[1], Y. Tan[1,4], B. Carlton[1], V. Vaidya[1], Y. Wang[1], T. Tetzlaff[1], S. Suzuki[1], A. Fahim[1], P. Seddighrad[1], J. Xie[5], Z. Zhang[6], D. S. Vemparala[1], A. Ravi[1], S. Pellerano[1], Y. Palaskas[1]
[1]Intel, Hillsboro, OR; [2]Fudan University, Shanghai, China; [3]Movellus Circuits, Ann Arbor, MI
[4]Radiawave Technologies, Shenzhen, China; [5]Intel, Chandler, AZ

3:45 PM

13.7 A 0.23mm² Digital Power Amplifier with Hybrid Time/Amplitude Control Achieving 22.5dBm at 28% PAE for 802.11g

D. Cousinard[1], R. Winoto[2], H. Li[2], Y. Fang[2], A. Ghaffari[2], A. Olyaei[2], O. Carnu[2], P. Godoy[2], A. Wong[2], X. Zhao[2], J. Liu[2], A. Mitra[2], R. Tsang[2], L. Lin[2], [1]Marvell, Etoy, Switzerland; [2]Marvell, Santa Clara, CA

4:15 PM

13.8 A 24dBm 2-to-4.3GHz Wideband Digital Power Amplifier with Built-In AM-PM Distortion Self-Compensation

J. Park[1], Y. Wang[2], S. Pellerano[2], C. Hull[2], H. Wang[1]
[1]Georgia Institute of Technology, Atlanta, GA; [2]Intel, Hillsboro, OR

4:30 PM

13.9 A 1.1V 28.6dBm Fully Integrated Digital Power Amplifier for Mobile and Wireless Applications in 28nm CMOS Technology with 35% PAE

A. Passamani[1], D. Ponton[1], E. Thaller[1], G. Knoblinger[1], A. Neviani[2], A. Bevilacqua[2]
[1]Intel, Villach, Austria; [2]University of Padova, Padova, Italy

4:45 PM

13.10 A >1W 2.2GHz Switched-Capacitor Digital Power Amplifier with Wideband Mixed-Domain Multi-Tap FIR Filtering of OOB Noise Floor

R. Bhat, J. Zhou, H. Krishnaswamy, Columbia University, New York, NY

Conclusion 5:15 PM

Deep-Learning Processors

Session Chair: ***Takashi Hashimoto,*** *Panasonic, Osaka, Japan*
Associate Chair: ***Mahesh Mehendale,*** *Texas Instruments, Bangalore, India*

1:30 PM

14.1 A 2.9TOPS/W Deep Convolutional Neural Network SoC in FD-SOI 28nm for Intelligent Embedded Systems DS2

G. Desoli[1], N. Chawla[2], T. Boesch[3], S-P. Singh[2], E. Guidetti[1], F. De Ambroggi[4], T. Majo[1], P. Zambotti[4], M. Ayodhyawasi[2], H. Singh[2], N. Aggarwal[2]
[1]STMicroelectronics, Cornaredo, Italy; [2]STMicroelectronics, Greater Noida, India
[3]STMicroelectronics, Geneva, Switzerland; [4]STMicroelectronics, Agrate Brianza, Italy

2:00 PM

14.2 DNPU: An 8.1TOPS/W Reconfigurable CNN-RNN Processor for General-Purpose Deep Neural Networks

D. Shin, J. Lee, J. Lee, H-J. Yoo, KAIST, Daejeon, Korea

2:30 PM

14.3 A 28nm SoC with a 1.2GHz 568nJ/Prediction Sparse Deep-Neural-Network Engine with >0.1 Timing Error Rate Tolerance for IoT Applications

P. N. Whatmough, S. K. Lee, H. Lee, S. Rama, D. Brooks, G-Y. Wei
Harvard University, Cambridge, MA

Break 3:00 PM

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14.4 A Scalable Speech Recognizer with Deep-Neural-Network Acoustic Models and Voice-Activated Power Gating

M. Price, J. Glass, A. Chandrakasan
Massachusetts Institute of Technology, Cambridge, MA

3:45 PM

14.5 ENVISION: A 0.26-to-10TOPS/W Subword-Parallel Dynamic-Voltage-Accuracy-Frequency-Scalable Convolutional Neural Network Processor in 28nm FDSOI

B. Moons, R. Uytterhoeven, W. Dehaene, M. Verhelst, KU Leuven, Leuven, Belgium

4:15 PM

14.6 A 0.62mW Ultra-Low-Power Convolutional-Neural-Network Face-Recognition Processor and a CIS Integrated with Always-On Haar-Like Face Detector DS2

K. Bong, S. Choi, C. Kim, S. Kang, Y. Kim, H-J. Yoo, KAIST, Daejeon, Korea

4:45 PM

14.7 A 288μW Programmable Deep-Learning Processor with 270KB On-Chip Weight Storage Using Non-Uniform Memory Hierarchy for Mobile Intelligence

S. Bang[1], J. Wang[1], Z. Li[1], C. Gao[1], Y. Kim[1,2], Q. Dong[1], Y-P. Chen[1], L. Fick[1], X. Sun[1], R. Dreslinski[1], T. Mudge[1], H. S. Kim[1], D. Blaauw[1], D. Sylvester[1]
[1]University of Michigan, Ann Arbor, MI; [2]CubeWorks, Ann Arbor, MI

5:00 PM

14.8 A 135mW Fully Integrated Data Processor for Next-Generation Sequencing

Y-C. Wu[1], J-H. Hung[2], C-H. Yang[1,2], [1]National Taiwan University, Taipei, Taiwan
[2]National Chiao Tung University, Hsinchu, Taiwan

Conclusion 5:15 PM

Innovations in Technologies and Circuits

Session Chair: ***Jan Genoe***, *imec, Leuven, Belgium*
Associate Chair: ***Hiroshi Fuketa***, *AIST, Tsukuba, Japan*

1:30 PM

15.1 Large-Scale Acquisition of Large-Area Sensors Using an Array of Frequency-Hopping ZnO Thin-Film-Transistor Oscillators DS2

Y. Afsar, T. Moy, N. Brady, S. Wagner, J. C. Sturm, N. Verma, Princeton University, Princeton, NJ

2:00 PM

15.2 A Flexible ISO14443-A Compliant 7.5mW 128b Metal-Oxide NFC Barcode Tag with Direct Clock Division Circuit from 13.56MHz Carrier DS2

K. Myny[1], Y-C. Lai[2], N. Papadopoulos[1], F. De Roose[1,3], M. Ameys[1], M. Willegems[1], S. Smout[1], S. Steudel[1], W. Dehaene[1,3], J. Genoe[1,3]

[1]imec, Heverlee, Belgium; [2]AU Optronics, Hsinchu, Taiwan; [3]KU Leuven, Leuven, Belgium

2:30 PM

15.3 An a-IGZO Asynchronous Delta-Sigma Modulator on Foil Achieving up to 43dB SNR and 40dB SNDR in 300Hz Bandwidth

C. Garripoli[1], J-L. P. J. van der Steen[2], E. Smits[2], G. H. Gelinck[2], A. H. M. Van Roermund[1], E. Cantatore[1]

[1]Eindhoven University of Technology, Eindhoven, The Netherlands

[2]Holst Centre / TNO, Eindhoven, The Netherlands

Break 3:00 PM

3:15 PM

15.4 A 1024-Element Scalable Optical Phased Array in 0.18μm SOI CMOS DS2

S. Chung, H. Abediasl, H. Hashemi, University of Southern California, Los Angeles, CA

3:45 PM

15.5 Cryo-CMOS Circuits and Systems for Scalable Quantum Computing

E. Charbon[1,2,3], F. Sebastiano[1], M. Babaie[1], A. Vladimirescu[4,5], M. Shahmohammadi[1], R. B. Staszewski[1], H. A. Homulle[1], B. Patra[1], J. P. van Dijk[1], R. M. Incandela[1], L. Song[1,6], B. Valizadehpasha[1]

[1]Delft University of Technology, Delft, The Netherlands; [2]EPFL, Lausanne, Switzerland

[3]Intel, Hillsboro, OR; [4]University of California, Berkeley, CA

[5]Institut Supérieur d'Electronique de Paris, Paris, France; [6]Tsinghua University, Beijing, China

4:15 PM

15.6 A 30-to-80MHz Simultaneous Dual-Mode Heterodyne Oscillator Targeting NEMS Array Gravimetric Sensing Applications with a 300zg Mass Resolution

G. Gourlat, M. Sansa, P. Villard, G. Sicard, G. Jourdan, I. Ouerghi, G. Billiot, S. Hentz
CEA-LETI-MINATEC, Grenoble, France

4:30 PM

15.7 Heterogeneous Integrated CMOS-Graphene Sensor Array for Dopamine Detection

B. Nasri, T. Wu, A. Alharbi, M. Gupta, R. RanjitKumar, S. Sebastian, Y. Wang, R. Kiani, D. Shahrjerdi, New York University, Brooklyn, NY

4:45 PM

15.8 A Permanent Digital Archive System Based on $4F^2$ X-Point Multi-Layer Metal Nano-Dot Structure

N. Miura, S. Liu, T. Watanabe, S. Imai, M. Nagata, Kobe University, Kobe, Japan

5:00 PM

15.9 An Integrated Optical Physically Unclonable Function Using Process-Sensitive Sub-Wavelength Photonic Crystals in 65nm CMOS

X. Lu, L. Hong, K. Sengupta, Princeton University, Princeton, NJ

Conclusion 5:15 PM

Gigahertz Data Converters

Session Chair: ***Jan Mulder,*** *Broadcom, Bunnik, The Netherlands*
Associate Chair: ***Paul Ferguson,*** *Analog Devices, Wilmington, MA*

1:30 PM

16.1 A 13b 4GS/s Digitally Assisted Dynamic 3-Stage Asynchronous Pipelined-SAR ADC

B. Vaz[1], A. Lynam[1], B. Verbruggen[1], A. Laraba[2], C. Mesadri[1], A. Boumaalif[3], J. Mcgrath[3], U. Kamath[1], R. D. L. Torre[1], A. Manlapat[1], D. Breathnach[3], C. Erdmann[1], B. Farley[1]
[1]Xilinx, Dublin, Ireland; [2]Xilinx, San Jose, CA; [3]Xilinx, Cork, Ireland

2:00 PM

16.2 A 9GS/s 1GHz-BW Oversampled Continuous-Time Pipeline ADC Achieving -161dBFS/Hz NSD DS2

H. Shibata[1], V. Kozlov[1], Z. Ji[1], A. Ganesan[2], H. Zhu[2], D. Paterson[2]
[1]Analog Devices, Toronto, Canada; [2]Analog Devices, Wilmington, MA

2:30 PM

16.3 A 330mW 14b 6.8GS/s Dual-Mode RF DAC in 16nm FinFET Achieving -70.8dBc ACPR in a 20MHz Channel at 5.2GHz

C. Erdmann, E. Cullen, D. Brouard, R. Pelliconi, B. Verbruggen, J. Mcgrath, D. Collins, M. De La Torre, P. Gay, P. Lynch, P. Lim, A. Collins, B. Farley
Xilinx, Dublin, Ireland

Break 3:00 PM

3:15 PM

16.4 A 5mW 7b 2.4GS/s 1-then-2b/cycle SAR ADC with Background Offset Calibration

C-H. Chan[1], Y. Zhu[1], I-M. Ho[1], W-H. Zhang[1], S-P. U[1,2], R. P. Martins[1,3]
[1]University of Macau, Macau, China; [2]Synopsys Macau Ltd, Macau, China
[3]Instituto Superior Tecnico/University of Lisboa, Lisboa, Portugal

3:45 PM

16.5 An 8GS/s Time-Interleaved SAR ADC with Unresolved Decision Detection Achieving -58dBFS Noise and 4GHz Bandwidth in 28nm CMOS

J. P. Keane[1], N. J. Guilar[1], D. Stepanovic[1,2], B. Wuppermann[1], C. Wu[1], C. W. Tsang[1,3], R. Neff[1], K. Nishimura[1]
[1]Keysight Technologies, Santa Clara, CA; [2]now with Apple, Cupertino, CA
[3]now with Adecco, Mountain View, CA

4:15 PM

16.6 A 10b DC-to-20GHz Multiple-Return-to-Zero DAC with >48dB SFDR

L. Duncan[1], B. Dupaix[1], J. McCue[1], B. Mathieu[1], M. LaRue[1], M. Teshome[2], M-J. Choe[2], W. Khalil[1]
[1]Ohio State University, Columbus, OH
[2]Teledyne Scientific and Imaging, Thousand Oaks, CA

4:45 PM

16.7 A 12b 10GS/s Interleaved Pipeline ADC in 28nm CMOS Technology DS2

S. Devarajan[1], L. Singer[1], D. Kelly[1], S. Kosic[2], T. Pan[1], J. Silva[1], J. Brunsilius[2], D. Rey-Losada[2], F. Murden[3], C. Speir[3], J. Bray[2], E. Otte[1], N. Rakuljic[2], P. Brown[3], T. Weigandt[2], Q. Yu[1], D. Paterson[1], C. Petersen[2], J. Gealow[1]
[1]Analog Devices, Wilmington, MA; [2]Analog Devices, San Diego, CA
[3]Analog Devices, Greensboro, NC

Conclusion 5:15 PM

TX and RX Building Blocks

Session Chair: ***Brian Ginsburg,*** *Texas Instruments, Dallas, TX*
Associate Chair: ***Payam Heydari,*** *University of California, Irvine, Irvine, CA*

1:30 PM

17.1 A Digitally Assisted CMOS WiFi 802.11ac/11ax Front-End Module Achieving 12% PA Efficiency at 20dBm Output Power with 160MHz 256-QAM OFDM Signal
Y. H. Chee[1], F. Golcuk[1], T. Matsuura[1], C. Beale[2], J. F. Wang[1], O. Shanaa[1]
[1]MediaTek, San Jose, CA; [2]MediaTek, Kent, United Kingdom

2:00 PM

17.2 A 28GHz Magnetic-Free Non-Reciprocal Passive CMOS Circulator Based on Spatio-Temporal Conductance Modulation
T. Dinc, H. Krishnaswamy, Columbia University, New York, NY

2:30 PM

17.3 A 60GHz On-Chip Linear Radiator with Single-Element 27.9dBm P_{sat} and 33.1dBm Peak EIRP Using Multifeed Antenna for Direct On-Antenna Power Combining
T. Chi, F. Wang, S. Li, M-Y. Huang, J. S. Park, H. Wang
Georgia Institute of Technology, Atlanta, GA

2:45 PM

17.4 A Sub-mW Antenna-Impedance Detection Using Electrical Balance for Single-Step On-Chip Tunable Matching in Wearable/Implantable Applications
C. Lu, A. Ba, Y-H. Liu, X. Wang, C. Bachmann, K. Philips
Holst Centre / imec, Eindhoven, The Netherlands

Break 3:00 PM

3:15 PM

17.5 An Intrinsically Linear Wideband Digital Polar PA Featuring AM-AM and AM-PM Corrections Through Nonlinear Sizing, Overdrive-Voltage Control, and Multiphase RF Clocking
M. Hashemi[1], Y. Shen[1], M. Mehrpoo[1], M. Acar[2], R. van Leuken[1], M. S. Alavi[1], L. de Vreede[1],
[1]Delft University of Technology, Delft, The Netherlands; [2]Ampleon, Nijmegen, The Netherlands

3:45 PM

17.6 Rapid and Energy-Efficient Molecular Sensing Using Dual mm-Wave Combs in 65nm CMOS: A 220-to-320GHz Spectrometer with 5.2mW Radiated Power and 14.6-to-19.5dB Noise Figure
C. Wang, R. Han, Massachusetts Institute of Technology, Cambridge, MA

4:15 PM

17.7 A Packaged 90-to-300GHz Transmitter and 115-to-325GHz Coherent Receiver in CMOS for Full-Band Continuous-Wave mm-Wave Hyperspectral Imaging
T. Chi, M-Y. Huang, S. Li, H. Wang, Georgia Institute of Technology, Atlanta, GA

4:30 PM

17.8 DS2 A Compact 130GHz Fully Packaged Point-to-Point Wireless System with 3D-Printed 26dBi Lens Antenna Achieving 12.5Gb/s at 1.55pJ/b/m
N. Dolatsha[1], B. Grave[1,2], M. Sawaby[1], C. Chen[1], A. Babveyh[1], S. Kananian[1], A. Bisognin[3,4], C. Luxey[3], F. Gianesello[4], J. Costa[5], C. Fernandes[5], A. Arbabian[1], [1]Stanford University, Stanford, CA
[2]CEA-LETI-MINATEC, Grenoble, France; [3]University of Nice, Nice, France
[4]STMicroelectronics, Crolles, France; [5]University of Lisbon, Lisbon, Portugal

4:45 PM

17.9 DS2 A 105Gb/s 300GHz CMOS Transmitter
K. Takano[1], S. Amakawa[1], K. Katayama[1], S. Hara[2], R. Dong[2], A. Kasamatsu[2], I. Hosako[2], K. Mizuno[3], K. Takahashi[3], T. Yoshida[1], M. Fujishima[1], [1]Hiroshima University, Higashihiroshima, Japan
[2]National Institute of Information and Communications Technology, Koganei, Japan
[3]Panasonic, Yokohama, Japan

5:00 PM

17.10 A 318-to-370GHz Standing-Wave 2D Phased Array in 0.13µm BiCMOS
H. Jalili, O. Momeni, University of California, Davis, CA

Conclusion 5:15 PM

TIMETABLE OF ISSCC 2017 SESSIONS

ISSCC 2017 • Sunday February 5th

Tutorials

8:30 AM	**T1:** mm-Wave Frequency Generation and Synthesis in Silicon	**T2:** NAND Flash Memory Design and Architecture Trends	**T3:** Readout Circuits for Physiological Signal Measurements
10:30 AM	**T4:** Energy-Efficient Processors for Deep Learning	**T5:** Fundamentals of Time-Based Circuits	**T6:** Signal Integrity Analysis for Gb/s Links
1:30 PM	**T7:** Design Trade-Offs in Digital Intensive PLLs	**T8:** Fundamentals of Class-D Amplifier Design	
3:30 PM	**T9:** Integrated mm-Wave Transmitters and Receivers for Spatial-Filtering Arrays	**T10:** Circuits and Technologies for Cell and Brain Interfacing	

Forums

8:00 AM	**F1:** Integrated Voltage Regulators for SoC and Emerging IoT Systems	**F2:** High-Performance Frequency Generation for Wireless and Wireline Systems

Events Below in Bold Box are Included with your Conference Registration

Evening Events

7:30 PM	**EE1:** Student-Research Preview: Short Presentations with Poster Session	**8:00 PM**	**EE2:** Intelligent Machines: Will the Technological Singularity Happen?

ISSCC 2017 • Monday February 6th

Paper Sessions

8:30 AM	**Session 1:** Plenary Session				
1:30 PM	**Session 2:** Power Amplifiers	**Session 3:** Digital Processors	**Session 4:** Imagers	**Session 5:** Analog Techniques	**Session 6:** Ultra-High-Speed Wireline

12noon to 7:00 PM – Book Displays • 5:00 PM to 7:00 PM – Demonstration Session • 5:15 PM – Author Interviews • Social Hour

Evening Events

8:00 PM	**EE3:** Quantum Engineering: Hype, Spin, or Reality?	**EE4:** Semiconductor Economics: How Business Decisions are Engineered

ISSCC 2017 • Tuesday February 7th

Paper Sessions

8:30 AM	**Session 7:** Wireless Transceivers	**Session 8:** Digital PLLs and Security Circuits	**Session 9:** Sensors	**Session 10:** DC-DC Converters	**Session 11:** Nonvolatile Memory Solutions **Session 12:** SRAM
1:30 PM	**Session 13:** High-Performance Transmitters	**Session 14:** Deep-Learning Processors	**Session 15:** Innovations in Technologies and Circuits	**Session 16:** Gigahertz Data Converters	**Session 17:** TX and RX Building Blocks

10:00 AM to 7:00 PM – Book Displays • 5:00 PM to 7:00 PM – Demonstration Session • 5:15 PM – Author Interviews • Social Hour

Evening Events

8:00 PM	**EE5:** When Will We Stop Driving Our Cars?	**EE6:** Return of Survey Says!

ISSCC 2017 • Wednesday February 8th

Paper Sessions

8:30 AM	**Session 18:** Full Duplex Wireless Front-Ends **Session 19:** Frequency Generation	**Session 20:** Digital Voltage Regulators and Low-Power Techniques	**Session 21:** Smart SoCs for Innovative Applications	**Session 22:** Harvesting and Wireless Power	**Session 23:** DRAM, MRAM & DRAM Interfaces
1:30 PM	**Session 24:** Wireless Receivers and Synthesizers	**Session 25:** GaN Drivers and Galvanic Isolators **Session 26:** Processor-Power Management and Clocking	**Session 27:** Biomedical Circuits	**Session 28:** Hybrid ADCs	**Session 29:** Optical- and Electrical-Link Innovations

10:00 AM to 3:00 PM – Book Displays • 5:15 PM – Author Interviews

ISSCC 2017 • Thursday February 9th

8:00 AM	**Short Course:** Ultra-Low-Power Analog Design	**F3:** Beyond the Horizon of Conventional Computing: From Deep Learning to Neuromorphic Systems	**F4:** Wireless Low-Power Transceivers for Local and Wide-Area Networks	**F5:** Wireline Transceivers for Mega Data Centers: 50Gb/s and Beyond	**F6:** Pushing the Performance Limits in Data Converters

Demonstration Session 2, Tuesday, February 7th, 5:00-7:00 PM

This year, the Demonstration Session extending in selected regular papers, both Academic and Industrial, will take place on Monday February 6th, and Tuesday February 7th, from 5 pm until 7 pm in the Golden Gate Hall. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2017, as noted by the symbol DS2

14.1 A 2.9TOPS/W Deep Convolutional Neural Network SoC in FD-SOI 28nm for Intelligent Embedded Systems

14.6 A 0.62mW Ultra-Low-Power Convolutional-Neural-Network Face-Recognition Processor and a CIS Integrated with Always-On Haar-Like Face Detector

15.1 Large-Scale Acquisition of Large-Area Sensors Using an Array of Frequency-Hopping ZnO Thin-Film-Transistor Oscillators

15.2 A Flexible ISO14443-A Compliant 7.5mW 128b Metal-Oxide NFC Barcode Tag with Direct Clock Division Circuit from 13.56MHz Carrier

15.4 A 1024-Element Scalable Optical Phased Array in 0.18μm SOI CMOS

16.2 A 9GS/s 1GHz-BW Oversampled Continuous-Time Pipeline ADC Achieving -161dBFS/Hz NSD

16.7 A 12b 10GS/s Interleaved Pipeline ADC in 28nm CMOS Technology

17.8 A Compact 130GHz Fully Packaged Point-to-Point Wireless System with 3D-Printed 26dBi Lens Antenna Achieving 12.5Gb/s at 1.55pJ/b/m

17.9 A 105Gb/s 300GHz CMOS Transmitter

18.2 Highly-Linear Integrated Magnetic-Free Circulator-Receiver for Full-Duplex Wireless

18.3 A Single-Port Duplex RF Front-End for X-Band Single-Antenna FMCW Radar in 65nm CMOS

20.1 A Digitally Controlled Fully Integrated Voltage Regulator with On-Die Solenoid Inductor with Planar Magnetic Core in 14nm Tri-Gate CMOS

21.5 A 3-to-5V Input 100V_{pp} Output 57.7mW 0.42% THD+N Highly Integrated Piezoelectric Actuator Driver

21.6 A 12nW Always-On Acoustic Sensing and Object Recognition Microsystem Using Frequency-Domain Feature Extraction and SVM Classification

21.8 An Actively Detuned Wireless Power Receiver with Public Key Cryptographic Authentication and Dynamic Power Allocation

22.1 A Self-Tuning Resonant Inductive Link Transmit Driver Using Quadrature-Symmetric Phase-Switched Fractional Capacitance

22.7 An Inductively-Coupled Wireless Power-Transfer System that is Immune to Distance and Load Variations

23.5 A 4Gb LPDDR2 STT-MRAM with Compact 9F^2 1T1MTJ Cell and Hierarchical Bitline Architecture

24.2 A 0.1-to-3.1GHz 4-Element MIMO Receiver Array Supporting Analog/RF Arbitrary Spatial Filtering

24.5 A 4.5nW Wake-Up Radio with -69dBm Sensitivity

24.7 A 673μW 1.8-to-2.5GHz Dividerless Fractional-N Digital PLL with an Inherent Frequency-Capture Capability and a Phase-Dithering Spur Mitigation for IoT Applications

26.2 Power Supply Noise in a 22nm z13™ Microprocessor

27.4 A Sub-1dB NF Dual-Channel On-Coil CMOS Receiver for Magnetic Resonance Imaging

EE5: When Will We Stop Driving Our Cars?

Organizers: **Martin Brox,** *Micron, Munich, Germany*
Jonathan Chang, *TSMC, Hsinchu, Taiwan*
Howard Luong, *Hong Kong University of Science and Technology, Kowloon, Hong Kong*
Paul Liang, *MediaTek, Hsinchu, Taiwan*

Moderator: **Riccardo Mariani,** *Intel, Hillsboro, OR*

Assisted driving has already arrived. However, widespread adaption of fully autonomous driving is still facing challenges. Will it arrive sooner, later, or ever? Is adoption still limited by technology, or are we simply waiting for the public or the infrastructure to be ready? This panel will discuss the introduction of autonomous driving from various angles. The goal of the discussion will be to arrive at an understanding of what needs to be done to enable mainstream adoption.

Panelists

Roger Berg, *Denso International America, Vista, CA*
Patrick Leteinturier, *Infineon, Neubiberg, Germany*
Markus Tremmel, *Bosch, Leonberg, Germany*
Jürgen Dickmann, *Daimler, Ulm, Germany*
Sahin Kirtavit, *NVIDIA, Santa Clara, CA*

EE6: Return of Survey Says!

Organizers: **Harry Lee,** *MIT, Cambridge, MA*
Matt Straayer, *Maxim Integrated, North Chelmsford, MA*

Moderator: **Chris Mangelsdorf,** *Analog Devices, San Diego, CA*

After the success of this evening event in 2016, Survey Says! returns to entertain the ISSCC audience. Two teams of panelists, all data-converter experts, compete to guess the most popular responses to a series of survey questions. While similar to the US game show "Family Feud", in this event the audience's participation is also solicited to make the evening more amusing and controversial than the TV game show. This year a new set of survey questions, both fun and technical, will be featured. Survey questions probe both professional and personal sides, for example: "What do you like about your job?" or "How do you get more time to tape-out?" or "Why does your project fall behind?". The contestants may ask for the audience's help after two failed guesses. This is an opportunity to learn how others in the field think in various situations and also to see how even the most experienced experts can struggle to guess even obvious answers when under pressure.

Panelists

Robert Adams, *Analog Devices, Wilmington, MA*
Lucien Breems, *NXP Semiconductors, Eindhoven, The Netherlands*
Yun Chiu, *University of Texas, Dallas, TX*
Michael Choi, *Samsung Electronics, Yongin, Korea*
Ian Galton, *University of California San Diego, La Jolla, CA*
Shanthi Pavan, *IIT Madras, Chennai, India*
Kathleen Philips, *imec/Holst Centre, Eindhoven, The Netherlands*
Ken Poulton, *Keysight Labs, Santa Clara, CA*

Full Duplex Wireless Front-Ends

Session Chair: ***Alyosha Molnar,*** *Cornell University, Ithaca, NY*
Associate Chair: ***Jan Craninckx,*** *imec, Leuven, Belgium*

8:30 AM

18.1 A 1.7-to-2.2GHz Full-Duplex Transceiver System with >50dB Self-Interference Cancellation over 42MHz Bandwidth

T. Zhang, A. Najafi, C. Su, J. C. Rudell
University of Washington, Seattle, WA

9:00 AM

18.2 Highly-Linear Integrated Magnetic-Free Circulator-Receiver for Full-Duplex Wireless DS2

N. Reiskarimian, M. Baraani Dastjerdi, J. Zhou, H. Krishnaswamy
Columbia University, New York, NY

9:30 AM

18.3 A Single-Port Duplex RF Front-End for X-Band Single-Antenna FMCW Radar in 65nm CMOS DS2

Y-H. Kao[1], H-C. Chou[1], C-C. Peng[1], Y-J. Wang[2], B. Su[3], T-S. Chu[1]
[1]National Tsing Hua University, Hsinchu, Taiwan
[2]National Chiao Tung University, Hsinchu, Taiwan
[3]National Taiwan University, Taipei, Taiwan

Break 10:00 AM

Frequency Generation

Session Chair: ***Andrea Mazzanti,*** *University of Pavia, Pavia, Italy*
Associate Chair: ***Xiang Gao,*** *Credo Semiconductor, Milpitas, CA*

10:15 AM

19.1 A Fundamental-Frequency 114GHz Circular-Polarized Radiating Element with 14dBm EIRP, -99.3dBc/Hz Phase-Noise at 1MHz Offset and 3.7% Peak Efficiency

P. Nazari, S. Jafarlou, P. Heydari
University of California, Irvine, CA

10:45 AM

19.2 A PVT-Robust -39dBc 1kHz-to-100MHz Integrated-Phase-Noise 29GHz Injection-Locked Frequency Multiplier with a 600μW Frequency-Tracking Loop Using the Averages of Phase Deviations for mm-Band 5G Transceivers

S. Yoo, S. Choi, J. Kim, H. Yoon, Y. Lee, J. Choi
Ulsan National Institute of Science and Technology, Ulsan, Korea

11:00 AM

19.3 A 50-to-66GHz 65nm CMOS All-Digital Fractional-N PLL with 220fs$_{rms}$ Jitter

A. Hussein, S. Vasadi, M. Soliman, J. Paramesh
Carnegie Mellon University, Pittsburgh, PA

11:30 AM

19.4 A 0.0049mm^2 2.3GHz Sub-Sampling Ring-Oscillator PLL with Time-Based Loop Filter Achieving -236.2dB Jitter-FOM

T-H. Chuang, H. Krishnaswamy
Columbia University, New York, NY

11:45 AM

19.5 A 2.4GHz RF Fractional-N Synthesizer with 0.25f$_{REF}$ BW

L. Kong , B. Razavi
University of California, Los Angeles, CA

12:00 PM

19.6 A 0.2V Trifilar-Coil DCO with DC-DC Converter in 16nm FinFET CMOS with 188dB FOM, 1.3kHz Resolution, and Frequency Pushing of 38MHz/V for Energy Harvesting Applications

C-C. Li[1], M-S. Yuan [1], C-H. Chang[1], Y-T. Lin[1], C-C. Liao[1], K. Hsieh[1], M. Chen[1], R. B. Staszewski[2,3]
[1]TSMC, Hsinchu, Taiwan
[2]Delft University of Technology, Delft, The Netherlands
[3]University College Dublin, Dublin, Ireland

Conclusion 12:15 PM

Digital Voltage Regulators and Low-Power Techniques

Session Chair: ***Atsuki Inoue,*** *Fujitsu Laboratories, Kawasaki, Japan*
Associate Chair: ***Dennis Sylvester,*** *University of Michigan, Ann Arbor, MI*

8:30 AM

20.1 A Digitally Controlled Fully Integrated Voltage Regulator with On-Die DS2 Solenoid Inductor with Planar Magnetic Core in 14nm Tri-Gate CMOS

H. K. Krishnamurthy, V. Vaidya, S. Weng, K. Ravichandran, P. Kumar, S. Kim, R. Jain, G. Matthew, J. Tschanz, V. De
Intel, Hillsboro, OR

9:00 AM

20.2 Digital Low-Dropout Regulator with Anti PVT-Variation Technique for Dynamic Voltage Scaling and Adaptive Voltage Scaling Multicore Processor

W-J. Tsou[1], W-H. Yang[1], J-H. Lin[1], H. Chen[1], K-H. Chen[1], C-L. Wey[1], Y-H. Lin[2], S-R. Lin[2], T-Y. Tsai[2]
[1]National Chiao Tung University, Hsinchu, Taiwan
[2]Realtek Semiconductor, Hsinchu, Taiwan

9:30 AM

20.3 A 100nA-to-2mA Successive-Approximation Digital LDO with PD Compensation and Sub-LSB Duty Control Achieving a 15.1ns Response Time at 0.5V

L. G. Salem, J. Warchall, P. P. Mercier, University of California, San Diego, CA

Break 10:00 AM

10:15 AM

20.4 An Output-Capacitor-Free Analog-Assisted Digital Low-Dropout Regulator with Tri-Loop Control

M. Huang[1,2], Y. Lu[1], S-P. U[1,3], R. P. Martins[1,4]
[1]University of Macau, Macau, China
[2]South China University of Technology, Guangzhou, China
[3]Synopsys Macau Ltd, Macau, China
[4]Instituto Superior Tecnico, Universidade de Lisboa, Portugal

10:45 AM

20.5 A Dual-Symmetrical-Output Switched-Capacitor Converter with Dynamic Power Cells and Minimized Cross Regulation for Application Processors in 28nm CMOS

J. Jiang[1,2], Y. Lu[1], W-H. Ki[2], S-P. U[1,3], R. P. Martins[1,4]
[1]University of Macau, Macau, China
[2]Hong Kong University of Science and Technology, Hong Kong, China
[3]Synopsys Macau Ltd, Macau, China
[4]Instituto Superior Tecnico, Universidade de Lisboa, Portugal

11:15 AM

20.6 A 0.5V-V_{IN} 1.44mA-Class Event-Driven Digital LDO with a Fully Integrated 100pF Output Capacitor

D. Kim[1], J. Kim[2], H. Ham[2], M. Seok[1]
[1]Columbia University, New York, NY; [2]SK hynix, Icheon, Korea

11:30 AM

20.7 A 13.8μW Binaural Dual-Microphone Digital ANSI S1.11 Filter Bank for Hearing Aids with Zero-Short-Circuit-Current Logic in 65nm CMOS

H-S. Wu, Z. Zhang, M. C. Papaefthymiou, University of Michigan, Ann Arbor, MI

Conclusion 11:45 AM

Smart SoCs for Innovative Applications

Session Chair: ***Antoine Dupret,*** *CEA Saclay, Gif-sur-Yvette, France*
Associate Chair: ***Pui-In Mak,*** *University of Macau, Macau, China*

8:30 AM

21.1 Nanowatt Circuit Interface to Whole-Cell Bacterial Sensors

P. Nadeau[1], M. Mimee[1], S. Carim[2], T. K. Lu[1], A. P. Chandrakasan[1]
[1]Massachusetts Institute of Technology, Cambridge, MA
[2]University of California, Berkeley, CA

9:00 AM

21.2 A 1.4mΩ-Sensitivity 94dB-Dynamic-Range Electrical Impedance Tomography SoC and 48-Channel Hub SoC for 3D Lung Ventilation Monitoring System

M. Kim, H. Kim, J. Jang, J. Lee, J. Lee, J. Lee, K. Lee, K. Kim, Y. Lee, H-J. Yoo
KAIST, Daejeon, Korea

9:30 AM

21.3 A Sub-mm³ Wireless Implantable Intraocular Pressure Monitor Microsystem

H. Bhamra, J-W. Tsai, Y-W. Huang, Q. Yuan, P. Irazoqui
Purdue University, West Lafayette, IN

9:45 AM

21.4 A Reduced-Order Sliding-Mode Controller with an Auxiliary PLL Frequency Discriminator for Ultrasonic Electric Scalpels

X. Liu[1,2], A. I. Colli-Menchi[1], E. Sanchez-Sinencio[1]
[1]Texas A&M University, College Station, TX; [2]Intel, Hillsboro, OR

Break 10:00 AM

10:15 AM

21.5 A 3-to-5V Input 100V_{pp} Output 57.7mW 0.42% THD+N Highly Integrated Piezoelectric Actuator Driver DS2

S. Chaput, D. Brooks, G-Y. Wei, Harvard University, Cambridge, MA

10:45 AM

21.6 A 12nW Always-On Acoustic Sensing and Object Recognition Microsystem Using Frequency-Domain Feature Extraction and SVM Classification DS2

S. Jeong[1], Y. Chen[1,2], T. Jang[1], J. Tsai[3], D. Blaauw[1], H-S. Kim[1], D. Sylvester[1]
[1]University of Michigan, Ann Arbor, MI; [2]Texas A&M University, College Station, TX
[3]Invensense, San Jose, CA

11:15 AM

21.7 2pJ/MAC 14b 8×8 Linear Transform Mixed-Signal Spatial Filter in 65nm CMOS with 84dB Interference Suppression

S. Joshi[1], C. Kim[1], S. Ha[2], Y. M. Chi[3], G. Cauwenberghs[1]
[1]University of California, San Diego, CA
[2]New York University, Abu Dhabi, United Arab Emirates; [3]Cognionics, San Diego, CA

11:45 AM

21.8 An Actively Detuned Wireless Power Receiver with Public Key Cryptographic Authentication and Dynamic Power Allocation DS2

N. V. Desai[1], C. Juvekar[1], S. Chandak[2], A. P. Chandrakasan[1]
[1]Massachusetts Institute of Technology, Cambridge, MA
[2]Stanford University, Stanford, CA

Conclusion 12:15 PM

Harvesting and Wireless Power

Session Chair: ***Stefano Stanzione,*** *Holst Centre / imec, Eindhoven, The Netherlands*
Associate Chair: ***Edgar Sinencio,*** *Texas A&M University, College Station, TX*

8:30 AM

22.1 A Self-Tuning Resonant Inductive Link Transmit Driver Using Quadrature-Symmetric Phase-Switched Fractional Capacitance DS2
H. Kennedy, R. Bodnar, T. Lee, W. Redman-White
University of Southampton, Southampton, United Kingdom

9:00 AM

22.2 A 1.7mm² Inductorless Fully Integrated Flipping-Capacitor Rectifier (FCR) for Piezoelectric Energy Harvesting with 483% Power-Extraction Enhancement
Z. Chen[1], M-K. Law[1], P-I. Mak[1], W-H. Ki[2], R. P. Martins[1,3]
[1]University of Macau, Macau, China
[2]Hong Kong University of Science and Technology, Hong Kong, China
[3]Instituto Superior Tecnico, Universidade de Lisboa, Portugal

9:30 AM

22.3 Adaptive Reconfigurable Voltage/Current-Mode Power Management with Self-Regulation for Extended-Range Inductive Power Transmission
H. Sadeghi Gougheri, M. Kiani, Pennsylvania State University, University Park, PA

Break 10:00 AM

10:15 AM

22.4 A Reconfigurable Bidirectional Wireless Power Transceiver with Maximum-Current Charging Mode and 58.6% Battery-to-Battery Efficiency
M. Huang[1,2], Y. Lu[1], S-P. U[1,3], R. P. Martins[1,4]
[1]University of Macau, Macau, China
[2]South China University of Technology, Guangzhou, China
[3]Synopsys Macau Ltd, Macau, China
[4]Instituto Superior Tecnico, Universidade de Lisboa, Portugal

10:45 AM

22.5 A 93%-Power-Efficiency Photovoltaic Energy Harvester with Irradiance-Aware Auto-Reconfigurable MPPT Scheme Achieving >95% MPPT Efficiency Across 650μW to 1W and 2.9ms FOCV MPPT Transient Time
S. Uprety, H. Lee, University of Texas at Dallas, Richardson, TX

11:15 AM

22.6 A Fully Integrated Counter-Flow Energy Reservoir for 70%-Efficient Peak-Power Delivery in Ultra-Low-Power Systems
X. Wu, K. Choo, Y. Shi, L-X. Chuo, D. Sylvester, D. Blaauw
University of Michigan, Ann Arbor, MI

11:30 AM

22.7 An Inductively-Coupled Wireless Power-Transfer System that is Immune to Distance and Load Variations DS2
J. Pan, A. A. Abidi, D. Rozgi?, H. Chandrakumar, D. Marković
University of California, Los Angeles, CA

11:45 AM

22.8 An AC-Input Inductorless LED Driver for Visible-Light-Communication Applications with 8Mb/s Data-Rate and 6.4% Low-Frequency Flicker
Y. Gao, L. Li, P. K. Mok
Hong Kong University of Science and Technology, Hong Kong, China

Conclusion 12:15 PM

DRAM, MRAM & DRAM Interfaces

Session Chair: ***Takefumi Yoshikawa,*** *Nagano College, Nagano, Japan*
Associate Chair: ***Seung-Jun Bae,*** *Samsung Electronics, Hwaseong, Korea*

8:30 AM

23.1 An 8Gb 12Gb/s/pin GDDR5X DRAM for Cost-Effective High-Performance Applications
M. Brox[1], M. Balakrishnan[1], M. Broschwitz[1], C. Chetreanu[1], S. Dietrich[1], F. Funfrock[1], M. Alvarez Gonzalez[1], T. Hein[1], E. Huber[1], D. Lauber[1], M. Ivanov[1], M. Kuzmenka[1], C. Mohr[2], F. E. Munoz[1], J. Ocon Garrido[1], S. Padaraju[1], S. Piatkowski[1], J. Pottgiesser[1], P. Pfefferl[1], M. Plan[1], J. Polney[1], S. Rau[1], M. Richter[1], R. Schneider[1], R. O. Seitter[1], W. Spirkl[1], M. Walter[1], J. Weller[1], F. Vitale[1]
[1]Micron, Munich, Germany; [2]Micron, Allen, TX

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23.2 A 5Gb/s/pin 8Gb LPDDR4X SDRAM with Power-Isolated LVSTL and Split-Die Architecture with 2-Die ZQ Calibration Scheme
C-K. Lee, Y-J. Eom, J-H. Park, J. Lee, H-R. Kim, K. Kim, Y. Choi, H-J. Chang, J. Kim, J-M. Bang, S. Shin, H. Park, S. Park, Y-R. Choi, H. Lee, K-H. Jeon, J-Y. Lee, H-J. Ahn, K-H. Kim, J-S. Kim, S. Chang, H-R. Hwang, D. Kim, Y-H. Yoon, S-H. Hyun, J-Y. Park, Y-G. Song, Y-S. Park, H-J. Kwon, S-J. Bae, T-Y. Oh, I-D. Song, Y-C. Bae, J-H. Choi, K-I. Park, S-J. Jang, G-Y. Jin
Samsung Electronics, Hwasung, Korea

9:30 AM

23.3 A 4.8Gb/s/pin 2Gb LPDDR4 SDRAM with Sub-100µA Self-Refresh Current for IoT Applications
N. Kwak, S-H. Kim, K. H. Lee, C-K. Baek, M. S. Jang, Y. Joo, S-H. Lee, W. Y. Lee, E. Lee, D. Han, J. Kang, J. H. Lim, J-B. Park, K-T. Kim, S. Cho, S. W. Han, J. Y. Keh, J. H. Chun, J. Oh, S. H. Lee
SK hynix, Icheon, Korea

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23.4 An Extremely Low-Standby-Power 3.733Gb/s/pin 2Gb LPDDR4 SDRAM for Wearable Devices
H-J. Kwon, E. Seo, C-Y. Lee, Y-H. Seo, G-H. Han, H-R. Kim, J-H. Lee, M-S. Jang, S-G. Do, S-H. cho, J-K. Park, S-Y. Doo, J-B. Shin, S-H. Jung, H-J. Kim, I-H. Im, B-R. cho, J-W. Lee, J-Y. Lee, K-H. Yu, H-K. Kim, C-H. Jeon, H-S. Park, S-S. Kim, S-H. Lee, J-W. Park, S-S. Lee, B-T. Lim, J-Y. Park, Y-S. Park, H-J. Kwon, S-J. Bae, J-H. Choi, K-I. Park, S-J. Jang, G-Y. Jin,
Samsung Electronics, Hwasung, Korea

Break 10:00 AM

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23.5 A 4Gb LPDDR2 STT-MRAM with Compact 9F² 1T1MTJ Cell and Hierarchical Bitline Architecture DS2
K. Rho[1], K. Tsuchida[2], D. Kim[1], Y. Shirai[2], J. Bae[1], T. Inaba[2], H. Noro[2], H. Moon[1], S. Chung[1], K. Sunouchi[2], J. Park[1], K. Park[1], A. Yamamoto[2], S. Chung[1], H. Kim[1], H. Oyamatsu[2], J. Oh[1]
[1]SK hynix Semiconductor, Icheon, Korea; [2]Toshiba Electronics Korea, Seoul, Korea

10:45 AM

23.6 A 0.6V 4.266Gb/s/pin LPDDR4X Interface with Auto-DQS Cleaning and Write-VWM Training for Memory Controller
S-M. Lee, J. Oh, J. Choi, S. Ko, D. Kim, K. Koo, J. Choi, Y. Nam, S. Park, H. Lee, E. Kim, S. Jung, K. Chae, S. Kim, S. Park, S. Lee, S. Park, Samsung Electronics, Hwasung, Korea

11:15 AM

23.7 A Time-Based Receiver with 2-tap DFE for a 12Gb/s/pin Single-Ended Transceiver of Mobile DRAM Interface in 0.8V 65nm CMOS
I-M. Yi[1], M-K. Chae[1], S-H. Hyun[2], S-J. Bae[2], J-H. Choi[2], S-J. Jang[2], B. Kim[1], J-Y. Sim[1], H-J. Park[1]
[1]Pohang University of Science and Technology, Pohang, Korea
[2]Samsung Electronics, Hwasung, Korea

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23.8 A 1V 7.8mW 15.6Gb/s C-PHY Transceiver Using Tri-Level Signaling for Post-LPDDR4
W. Choi[1], T. Kim[1], J. Shim[2], H. Kim[2], G. Han[1], Y. Chae[1]
[1]Yonsei University, Seoul, Korea; [2]SK hynix, Icheon, Korea

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23.9 An 8-Channel 4.5Gb 180GB/s 18ns-Row-Latency RAM for the Last Level Cache
T-K. J. Ting[1], G-B. Wang[1], M-H. Wang[1], C-P. Wu[1], C-K. Wang[1], C-W. Lo[1], L-C. Tien[1], D-M. Yuan[1], Y-C. Hsieh[1], J-S. Lai[2], W-P. Hsu[2], C-C. Huang[2], C-K. Chen[2], Y-F. Chou[2], D-M. Kwai[2], Z. Wang[3], W. Wu[3], S. Tomishima[3], P. Stolt[3], S-L. Lu[4]
[1]Piecemakers Technology, Hsinchu, Taiwan; [2]ITRI, Hsinchu, Taiwan; [3]Intel, Hilsboro, OR
[4]TSMC, Hsinchu, Taiwan

Conclusion 12:15 PM

Wireless Receivers and Synthesizers

Session Chair: ***Chun-Huat Heng,*** *National University of Singapore, Singapore*
Associate Chair: ***Ken Yamamoto,*** *Sony Semiconductor Solutions, Atsugi, Japan*

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24.1 A 770pJ/b 0.85V 0.3mm² DCO-Based Phase-Tracking RX Featuring Direct Demodulation and Data-Aided Carrier Tracking for IoT Applications
Y-H. Liu[1], V. K. Purushothaman[1,2], C. Lu[1], J. Dijkhuis[1], R. B. Staszewski[2,3], C. Bachmann[1], K. Philips[1]
[1]Holst Centre / imec, Eindhoven, The Netherlands
[2]Delft University of Technology, Delft, The Netherlands; [3]University College Dublin, Dublin, Ireland

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24.2 A 0.1-to-3.1GHz 4-Element MIMO Receiver Array Supporting Analog/RF Arbitrary Spatial Filtering DS2
L. Zhang, H. Krishnaswamy, Columbia University, New York, NY

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24.3 A High-Linearity CMOS Receiver Achieving +44dBm IIP3 and +13dBm B_{1dB} for SAW-Less LTE Radio
Y. Lien[1,2], E. Klumperink[1], B. Tenbroek[3], J. Strange[3], B. Nauta[1]
[1]University of Twente, Enschede, The Netherlands; [2]MediaTek, Hsinchu, Taiwan
[3]MediaTek, Kent, United Kingdom

Break 3:00 PM

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24.4 A 0.18V 382µW Bluetooth Low-Energy (BLE) Receiver with 1.33nW Sleep Power for Energy-Harvesting Applications in 28nm CMOS
W-H. Yu[1], H. Yi[1], P-I. Mak[1], J. Yin[1], R. P. Martins[1,2]
[1]University of Macau, Macau, China; [2]Instituto Superior Tecnico, Universidade de Lisboa, Portugal

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24.5 A 4.5nW Wake-Up Radio with -69dBm Sensitivity DS2
H. Jiang, P-H. P. Wang, L. Gao, P. Sen, Y-H. Kim, G. M. Rebeiz, D. A. Hall, P. P. Mercier
University of California, San Diego, CA

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24.6 A Time-Interleaved Filtering-by-Aliasing Receiver Front-End with >70dB Suppression at <4×Bandwidth Frequency Offset
S. Hameed, S. Pamarti, University of California, Los Angeles, CA

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24.7 A 673µW 1.8-to-2.5GHz Dividerless Fractional-N Digital PLL with an Inherent Frequency-Capture Capability and a Phase-Dithering Spur Mitigation for IoT Applications DS2
Y. He[1], Y-H. Liu[1], T. Kuramochi[2], J. van den Heuvel[1], B. Busze[1], N. Markulic[3], C. Bachmann[1], K. Philips[1]
[1]Holst Centre / imec, Eindhoven, The Netherlands
[2]Rohm Semiconductor, Dusseldorf, Germany; [3]imec, Heverlee, Belgium

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24.8 A 14nm Fractional-N Digital PLL with 0.14ps_{rms} Jitter and -78dBc Fractional Spur for Cellular RFICs
C-W. Yao[1], W. F. Loke[1], R. Ni[1], Y. Han[1], H. Li[1], K. Godbole[1], Y. Zuo[1], S. Ko[2], N-S. Kim[2], S. Han[2], I. Jo[2], J. Lee[2], J. Han[2], D. Kwon[2], C. Kim[2], S. Kim[2], S. W. Son[1], T. B. Cho[2]
[1]Samsung Semiconductor, San Jose, CA; [2]Samsung Electronics, Hwasung, Korea

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24.9 A 128-QAM 60GHz CMOS Transceiver for IEEE802.11ay with Calibration of LO Feedthrough and I/Q Imbalance
J. Pang, S. Maki, S. Kawai, N. Nagashima, Y. Seo, M. Dome, H. Kato, M. Katsuragi, K. Kimura, S. Kondo, Y. Terashima, H. Liu, T. Siriburanon, A. T. Narayanan, N. Fajri, T. Kaneko, T. Yoshioka, B. Liu, Y. Wang, R. Wu, N. Li, K. K. Tokgoz, M. Miyahara, K. Okada, A. Matsuzawa
Tokyo Institute of Technology, Tokyo, Japan

Conclusion 5:15 PM

GaN Drivers and Galvanic Isolators

Session Chair: ***Shuichi Nagai,*** *Panasonic, Osaka, Japan*
Associate Chair: ***Yogesh Ramadass*****,** *Texas Instruments, Santa Clara, CA*

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25.1 A 50.7% Peak Efficiency Subharmonic Resonant Isolated Capacitive Power Transfer System with 62mW Output Power for Low-Power Industrial Sensor Interfaces

L. Chen[1], J. Sankman[1,2], R. Mukhopadhyay[2], M. Morgan[2], D. B. Ma[1]
[1]University of Texas at Dallas, Richardson, TX
[2]Texas Instruments, Dallas, TX

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25.2 A 10MHz 3-to-40V V_{IN} Tri-Slope Gate Driving GaN DC-DC Converter with 40.5dBμV Spurious Noise Compression and 79.3% Ringing Suppression for Automotive Applications

X. Ke[1], J. Sankman[1,2], Y. Chen[1], L. He[3], D. B. Ma[1]
[1]University of Texas at Dallas, Richardson, TX
[2]Texas Instruments, Dallas, TX
[3]Zhejiang University, Hangzhou, China

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25.3 A 1.3A Gate Driver for GaN with Fully Integrated Gate Charge Buffer Capacitor Delivering 11nC Enabled by High-Voltage Energy Storing

A. Seidel, B. Wicht
Reutlingen University, Reutlingen, Germany

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25.4 A 500Mb/s 200pJ/b Die-to-Die Bidirectional Link with 24kV Surge Isolation and 50kV/μs CMR using Resonant Inductive Coupling in 0.18μm CMOS

S. Mukherjee[1], A. N. Bhat[1], K. A. Shrivastava[1], M. Bonu[1], B. Sutton[2], V. Gopinathan[1], G. Thiagarajan[1], A. Patki[1], J. Malakar[1], N. Krishnapura[3]
[1]Texas Instruments, Bangalore, India
[2]Texas Instruments, Dallas, TX
[3]IIT Madras, Chennai, India

Break 3:00 PM

Processor-Power Management and Clocking

Session Chair: ***Kathy Wilcox,*** *AMD, Boxborough, MA*
Associate Chair: ***Youngmin Shin*****,** *Samsung, Hwaseong, Korea*

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26.1 Design Optimization of Computing Systems from the Nanoscale Transistor to the Datacentre

A. Nalamalpu
Intel, Hillsboro, OR

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26.2 Power Supply Noise in a 22nm z13™ Microprocessor

DS2 *P. I-J. Chuang[1], C. Vezyrtzis[1], D. Pathak[2], R. Rizzolo[3], T. Webel[4], T. Strach[4], O. Torreiter[4], P. Lobo[5], A. Buyuktosunoglu[1], R. Bertran[1], M. Floyd[6], M. Ware[6], G. Salem[7], S. Carey[8], P. Restle[1]*
[1]IBM Research, Yorktown Heights, NY
[2]Drexel University, Philadelphia, PA
[3]IBM, Poughkeepsie, NY
[4]IBM STG, Boeblingen, Germany
[5]IBM STG, Bangalore, India
[6]IBM STG, Austin, TX
[7]IBM STG, Burlington, NY
[8]IBM STG, Poughkeepsie, NY

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26.3 Reconfigurable Clock Networks for Random Skew Mitigation from Subthreshold to Nominal Voltage

L. Lin, S. Jain, M. Alioto
National University of Singapore, Singapore, Singapore

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26.4 A 0.4-to-1V 1MHz-to-2GHz Switched-Capacitor Adiabatic Clock Driver Achieving 55.6% Clock Power Reduction

L. G. Salem, P. P. Mercier
University of California, San Diego, CA

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26.5 Adaptive Clocking in the POWER9™ Processor for Voltage Droop Protection

M. S. Floyd[1], P. J. Restle[2], M. A. Sperling[3], P. Owczarczyk[3], E. J. Fluhr[1], J. Friedrich[1], P. Muench[3], T. Diemoz[3], P. Chuang[2], C. Vezyrtzis[2]
[1]IBM, Austin, TX
[2]IBM, Yorktown Heights, NY
[3]IBM, Poughkeepsie, NY

Conclusion 5:15 PM

Biomedical Circuits

Session Chair: ***Gert Cauwenberghs,*** *University of California, San Diego, La Jolla, CA*
Associate Chair: ***Michiel Pertijs,*** *Delft University of Technology, Delft, The Netherlands*

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27.1 A 2.8μW 80mV$_{pp}$-Linear-Input-Range 1.6GΩ-Input Impedance Bio-Signal Chopper Amplifier Tolerant to Common-Mode Interference up to 650mV$_{pp}$
H. Chandrakumar, D. Marković, University of California, Los Angeles, CA

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27.2 A 25.2mW EEG-NIRS Multimodal SoC for Accurate Anesthesia Depth Monitoring
U. Ha[1], J. Lee[1], J. Lee[1], K. Kim[1], M. Kim[1], T. Roh[2], S. Choi[3], H-J. Yoo[1]
[1]KAIST, Daejeon, Korea; [2]K-Healthwear, Daejeon, Korea
[3]Korea University Guro Hospital, Seoul, Korea

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27.3 All-Wireless 64-Channel 0.013mm²/ch Closed-Loop Neurostimulator with Rail-to-Rail DC Offset Removal
H. Kassiri[1], M. R. Pazhouhandeh[2], N. Soltani[2], M. T. Salam[3], P. Carlen[2,4], J. L. Perez Velazquez[2], R. Genov[2]
[1]York University, Toronto, Canada; [2]University of Toronto, Toronto, Canada
[3]GSK (GlaxoSmithKline), Stevenage, United Kingdom
[4]Toronto Western Hospital, Toronto, Canada

Break 3:00 PM

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27.4 A Sub-1dB NF Dual-Channel On-Coil CMOS Receiver for Magnetic Resonance Imaging DS2
B. Sporrer[1], L. Wu[1], L. Bettini[1], C. Vogt[1], J. Reber[2], J. Marjanovic[2], T. Burger[1], D. O. Brunner[2], K. P. Prüssmann[2], G. Tröster[1], Q. Huang[1]
[1]ETH Zurich, Zurich, Switzerland; [2]University and ETH Zurich, Zurich, Switzerland

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27.5 A Pixel-Pitch-Matched Ultrasound Receiver for 3D Photoacoustic Imaging with Integrated Delta-Sigma Beamformer in 28nm UTBB FDSOI
M-C. Chen[1], A. Peña Perez[1], S-R. Kothapalli[1], P. Cathelin[2], A. Cathelin[2], S. S. Gambhir[1], B. Murmann[1]
[1]Stanford University, Stanford, CA; [2]STMicroelectronics, Crolles, France

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27.6 Single-Chip 3072ch 2D Array IC with RX Analog and All-Digital TX Beamformer for 3D Ultrasound Imaging
Y. Katsube[1], S. Kajiyama[2], T. Nishimoto[1], T. Nakagawa[2], Y. Okuma[3], Y. Nakamura[2], T. Terada[2], Y. Igarashi[1], T. Yamawaki[2], T. Yazaki[1], Y. Hayashi[2], K. Amino[2], T. Kaneko[2], H. Tanaka[2]
[1]Hitachi, Yokohama, Japan; [2]Hitachi, Kokubunji, Japan; [3]Hitachi, Hatoyama, Japan

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27.7 A 30.5 mm³ Fully Packaged Implantable Device with Duplex Ultrasonic Data and Power Links Achieving 95kb/s with <10^{-4} BER at 8.5cm Depth
T. C. Chang, M. L. Wang, J. Charthad, M. J. Weber, A. Arbabian
Stanford University, Stanford, CA

5:00 PM

27.8 Fully Integrated Optical Spectrometer with 500-to-830nm Range in 65nm CMOS
L. Hong, K. Sengupta, Princeton University, Princeton, NJ

Conclusion 5:15 PM

Hybrid ADCs

Session Chair: ***Tai-Cheng Lee,*** *National Taiwan University, Taipei, Taiwan*
Associate Chair: ***Bob Verbruggen,*** *Xilinx, Dublin, Ireland*

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28.1 A 0.46mW 5MHz-BW 79.7dB-SNDR Noise-Shaping SAR ADC with Dynamic-Amplifier-Based FIR-IIR Filter
C-C. Liu, M-C. Huang, MediaTek, Hsinchu, Taiwan

2:00 PM

28.2 An 11.4mW 80.4dB-SNDR 15MHz-BW CT Delta-Sigma Modulator Using 6b Double-Noise-Shaped Quantizer
T. Kim, C. Han, N. Maghari, University of Florida, Gainesville, FL

2:30 PM

28.3 A 125MHz-BW 71.9dB-SNDR VCO-Based CT ΔΣ ADC with Segmented Phase-Domain ELD Compensation in 16nm CMOS
S-J. Huang, N. Egan, D. Kesharwani, F. Opteynde, M. Ashburn, MediaTek, Woburn, MA

Break 3:00 PM

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28.4 A 12b 330MS/s Pipelined-SAR ADC with PVT-Stabilized Dynamic Amplifier Achieving <1dB SNDR Variation
H. Huang[1], S. Sarkar[1], B. Elies[2], Y. Chiu[1]
[1]University of Texas at Dallas, Richardson, TX; [2]Texas Instruments, Dallas, TX

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28.5 A 10b 1.5GS/s Pipelined-SAR ADC with Background Second-Stage Common-Mode Regulation and Offset Calibration in 14nm CMOS FinFET
L. Kull[1], D. Luu[1,2], C. Menolfi[1], M. Braendli[1], P. A. Francese[1], T. Morf[1], M. Kossel[1], H. Yueksel[1], A. Cevrero[1], I. Ozkaya[1], T. Toifl[1]
[1]IBM Zurich Research Laboratory, Rueschlikon, Switzerland
[2]ETH Zurich, Zurich, Switzerland

4:15 PM

28.6 A 78.5dB-SNDR Radiation- and Metastability-Tolerant Two-Step Split SAR ADC Operating up to 75MS/s with 24.9mW Power Consumption in 65nm CMOS
H. Xu[1], Y. Cai[1], L. Du[2], Y. Zhou[3], B. Xu[1], D. Gong[4], J. Ye[4], Y. Chiu[1]
[1]University of Texas at Dallas, Richardson, TX
[2]University of Electronic Science and Technology of China, Chengdu, China
[3]Broadcom, Irvine, CA; [4]Southern Methodist University, Dallas, TX

4:45 PM

28.7 A 0.7V 12b 160MS/s 12.8fJ/conv-step Pipelined-SAR ADC in 28nm CMOS with Digital Amplifier Technique
K. Yoshioka, T. Sugimoto, N. Waki, S. Kim, D. Kurose, H. Ishii, M. Furuta, A. Sai, T. Itakura
Toshiba, Kawasaki, Japan

Conclusion 5:15 PM

Optical- and Electrical-Link Innovations

Session Chair: ***Sam Palermo,*** *Texas A&M University, College Station, TX*
Associate Chair: ***Hideyuki Nosaka,*** *NTT, Atsugi, Japan*

1:30 PM

29.1 A 64Gb/s 1.4pJ/b NRZ Optical-Receiver Data-Path in 14nm CMOS FinFET

A. Cevrero[1], I. Ozkaya[1,3], P. A. Francese[1], C. Menolfi[1], T. Morf[1], M. Brandli[1], D. Kuchta[2], L. Kull[1], J. Proesel[2], M. Kossel[1], D. Luu[1], B. Lee[2], F. Doany[2], M. Meghelli[2], Y. Leblebici[3], T. Toifl[1]
[1]IBM Research, Rueschlikon, Switzerland; [2]IBM Research, Yorktown Heights, NY
[3]EPFL, Lausanne, Switzerland

2:00 PM

29.2 A Transmitter and Receiver for 100Gb/s Coherent Networks with Integrated 4×64GS/s 8b ADCs and DACs in 20nm CMOS

J. Cao, D. Cui, A. Nazemi, T. He, G. Li, B. Catli, M. Khanpour, K. Hu, T. Ali, H. Zhang, H. Yu, B. Rhew, S. Sheng, Y. Shim, B. Zhang, A. Momtaz
Broadcom, Irvine, CA

2:30 PM

29.3 A 40Gb/s PAM-4 Transmitter Based on a Ring-Resonator Optical DAC in 45nm SOI CMOS

S. Moazeni[1], S. Lin[1], M. T. Wade[2], L. Alloatti[3], R. J. Ram[4], M. A. Popovic[5], V. Stojanovic[1]
[1]University of California, Berkeley, CA; [2]Ayar Labs, San Francisco, CA
[3]ETH Zurich, Zurich, Switzerland
[4]Massachusetts Institute of Technology, Cambridge, MA
[5]Boston University, Boston, MA

Break 3:00 PM

3:15 PM

29.4 A 16Gb/s 3.6pJ/b Wireline Transceiver with Phase Domain Equalization Scheme: Integrated Pulse Width Modulation (iPWM) in 65nm CMOS

A. Ramachandran, A. Natarajan, T. Anand, Oregon State University, Corvallis, OR

3:45 PM

29.5 12Gb/s Over Four Balanced Lines Utilizing NRZ Braid Clock Signaling with 100% Data Payload and Spread Transition Scheme for 8K UHD Intra-Panel Interfaces

Y. Lee, Y. Choi, S-G. Bae, J. Jun, J. Song, S. Hwang, C. Kim
Korea University, Seoul, Korea

4:15 PM

29.6 A 3-to-10Gb/s 5.75pJ/b Transceiver with Flexible Clocking in 65nm CMOS

R. K. Nandwana[1], S. Saxena[2], A. Elkholy[1], M. Talegaonkar[1], J. Zhu[1], W-S. Choi[1], A. Elmallah[1], P. K. Hanumolu[1]
[1]University of Illinois, Urbana, IL; [2]IIT Madras, Chennai, India

4:45 PM

29.7 A 2.5GHz Injection-Locked ADPLL with 197fs$_{rms}$ Integrated Jitter and -65dBc Reference Spur Using Time-Division Dual Calibration

S. Kim[1], H-G. Ko[1], S-Y. Cho[1], J. Lee[1], S. Shin[1], M-S. Choo[1], H. Chi[2], D-K. Jeong[1]
[1]Seoul National University, Seoul, Korea; [2]SK hynix, Icheon, Korea

Conclusion 5:00 PM

Ultra-Low-Power Analog Design

Time:	Topic:
8:00 AM	Breakfast
8:20 AM	Introduction by Chair, ***Daniel Friedman*** *IBM Thomas J. Watson Research Center, Yorktown Heights, NY*
8:30 AM	**MOSFET Modeling for Ultra-Low-Power Analog** ***Christian Enz,*** *EPFL, Neuchatel, Switzerland*
10:00 AM	Break
10:30 AM	**Integrated DC-DC Converters for Low-Power Applications: From Discrete Towards Fully-Integrated-CMOS Power Management** ***Michiel Steyaert,*** *KU Leuven, Leuven, Belgium*
12:15 PM	Lunch
1:20 PM	**Ultra-Low-Power References and Oscillators** ***Dennis Sylvester,*** *University of Michigan, Ann Arbor, MI*
2:50 PM	Break
3:20 PM	**Micropower ADCs** ***Kofi Makinwa,*** *Delft University of Technology, Delft, The Netherlands*
4:50 PM	Conclusion

Introduction

A critical dominant trend in the evolution of the electronics industry is the incredible growth in the sheer number of devices that are being deployed annually across a wide range of applications. Many of these devices are being leveraged to provide interfaces between the analog world and the digital infrastructure that supports the Internet of Everything, providing environmental sensing data to drive more effective pollution management, component data to enhance equipment lifetime and automate repair scheduling, process data to improve manufacturing effectiveness, and much, much more. The proliferation of devices also extends to enabling health care applications, improved logistics capability, and, very broadly, enabling the optimization of compute workloads across complete application stacks. Low power analog circuits are the critical enablers for such applications, and nano-powered analog circuits are and will be the critical enablers for a further wide range of emerging applications.

In this short course, we explore ultra-low power analog circuits from modeling strategies to their implementation in the context of critically significant macro-level elements. The first presentation examines modeling approaches suited to ultra-low power analog design, describing the methodology in the context of several deep submicron processes. Circuit design examples are used extensively in the presentation to clarify the presented concepts. The second presentation takes up a key block in any low power system, namely, the DC-DC converter, with primary focus on the path from bulky to compact regulator solutions that enable the penetration of electronics into an ever-widening set of applications. The third presentation focuses on references and oscillators, both of which are central to almost any low-power electronic implementation. Key elements discussed in detail include ultra-low power bandgap circuits and ultra-low power timer implementations. Finally, the last presentation turns to the challenge of micropower data converters, which must provide an efficient interface between the analog world and the digital back end for a host of applications. The presentation interleaves the discussion of core ultra-low power techniques with design examples that elucidate these techniques. Broadly, the four presentations explore ultra-low power analog design, an integral part of creating efficient, pervasive solutions for the problems of today and tomorrow.

8:30 AM SC1: MOSFET Modeling for Ultra-Low-Power Analog

Christian Enz, *EPFL, Neuchatel, Switzerland*

The emergence of the IoT poses stringent requirements on the energy consumption and has hence become the primary driver for ultra-low-power circuit design. Implementation of complex functions under highly constrained power and area budgets makes analog and RF circuit design ever more challenging. Some guidance would therefore be invaluable for the designer to navigate the design space.

This short course presents simple MOSFET models that can be applied to design of ultra-low-power analog and RF. It starts with the presentation of the concept of inversion coefficient IC as an essential design parameter that spans the entire range of operating points from weak to strong inversion. Several figures-of-merit (FOM) capturing the various trade-offs encountered in analog and RF circuit design are presented and compared to measurements of 40nm and 28nm CMOS processes. Finally, a simple technique to extract the basic model parameters is described before concluding.

Christian Enz is currently Professor at the Swiss Federal Institute of Technology (EPFL), Director of the Microengineering Institute and head of the IC Lab. Until April 2013 he was VP at the Swiss Center for Electronics and Microtechnology (CSEM) heading the Integrated and Wireless Systems Division.

10:30 AM SC2: Integrated DC-DC Converters for Low-Power Applications: From Discrete Towards Fully-Integrated-CMOS Power Management

Michiel Steyaert, *KU Leuven, Leuven, Belgium*

In this session, trends and techniques towards fully integrated CMOS DC-DC converters for low-power applications are studied. Both inductive and capacitive DC-DC converters are analyzed towards the objective of full integration with external components. The required on-chip components, such as inductors, capacitors and switches, are discussed. Different control-loop techniques are presented in order to achieve high integration density and meet low ripple requirements. Many recent design techniques, such as multi-core, gearbox and SPCR (Scalable Parasitic Charge Redistribution) are studied. Different design styles, both boost and buck, are analyzed and compared with classical LDO regulators.

Michiel Steyaert received the Ph.D. degree from KU Leuven in 1987. In 1988, he was Visiting Assistant Professor at UCLA. In 1989, he was appointed as part-time Associate Professor and Research Director at MICAS, KU Leuven, where he is now a Full Professor. He was the Chair of the EE Department from 2005 until 2012, and now serves as Dean of the Faculty of Engineering.

Prof. Steyaert has co-authored over 500 papers and over 24 books. He received ESSCIRC Best Paper Awards in 1990 and 2001, IEEE ISSCC Evening Session Awards in 1995 and 1997, ISSCC Top Contributor Awards in 2003 and 2013 (the only European researcher to receive both). He became an IEEE Fellow in 2003.

1:20 PM SC3: Ultra-Low-Power References and Oscillators

Dennis Sylvester, *University of Michigan, Ann Arbor, MI*

This talk reviews the state of the art in ultra-low-power voltage references as well as RC oscillators and 32kHz crystal oscillators. The focus is on sub-μW designs, including many in the sub-nW range. Threshold-based references and bandgap references are discussed, as well as oscillators with power consumptions that range from pW with relatively poor temperature and line sensitivities, to tens of nW with excellent frequency stability.

Dennis Sylvester received a PhD from the University of California, Berkeley and is a Professor of Electrical Engineering and Computer Science at the University of Michigan, Ann Arbor. He has published over 400 articles along with one book and several book chapters, and holds 31 US patents. His research interests include the design of millimeter-scale computing systems and energy efficient near-threshold computing. He is co-founder of Ambiq Micro, a fabless semiconductor company developing ultra-low-power mixed-signal solutions for compact wireless devices. He is an IEEE Fellow.

3:20 PM SC4: Micropower ADCs

Kofi Makinwa, *Delft University of Technology, Delft, The Netherlands*

Micropower ADCs, i.e. ADCs that dissipate less than 1mW, have become critical components of autonomous systems for the IoT. In this short course, the basic principles of micropower SAR and delta-sigma ADCs will be discussed. It will then be shown how these two well-known techniques can be combined to realize hybrid ADCs that can achieve both micropower and high (> 14-bit) resolution.

Kofi Makinwa is a Professor at Delft University of Technology. His main research interests are in the design of analog circuits and sensor interfaces. This has resulted in over 200 publications. He is an IEEE fellow, an ISSCC top-10 contributor, and a co-recipient of 13 best paper awards, from the JSSC, ISSCC, ESSCIRC, Transducers and ISCAS among others.

F3: Beyond the Horizon of Conventional Computing: From Deep Learning to Neuromorphic Systems

Organizer: **Meng-Fan Chang,** *National Tsing Hua University, Hsinchu, Taiwan*

Committee: **Jun Deguchi,** *Toshiba, Kawasaki, Japan*
Vivek De, *Intel, Hillsboro, OR*
Masato Motomura, *Hokkaido University, Hokkaido, Japan*
Shinichiro Shiratake, *Toshiba, Tokyo, Japan*
Marian Verhelst, *KU Leuven, Leuven, Belgium*

This forum brings together experts in software applications, system architectures, and chip designs to explore cognitive computing approaches over the near-, mid-, and long-term.

Forum Agenda

Time:	Topic:
8:00 AM	Breakfast
8:20 AM	Introduction ***Meng-Fan Chang,*** *National Tsing Hua University, Hsinchu, Taiwan*
8:30 AM	**High Performance Computing Opportunities in Deep Learning** ***Gregory Diamos,*** *Baidu, Sunnyvale, CA*
9:20 AM	**Deep Learning at Cloud Scale** ***Andrew Putnam,*** *Microsoft, Seattle, WA*
10:10 AM	Break
10:35 AM	**High Performance Deep-Learning Architecture and its Implementation** ***Zidong Du,*** *Chinese Academy of Sciences, Beijing, China*
11:25 AM	**Deep Learning-Deep Neural Networks, Architecture and SoC Implementations** ***Hoi-Jun Yoo,*** *KAIST, Daejeon, Korea*
12:15 PM	Lunch
1:20 PM	**Neural Networks on FPGAs** ***Jason Cong,*** *University of California, Los Angeles, Los Angeles, CA*
2:10 PM	**Efficient Hardware for Deep Learning** ***Bill Dally****, NVIDIA, Santa Clara, CA*
3:00 PM	Break
3:20 PM	**Plenty of Room at the Bottom? Toward fJ/OP Deep Convolutional Network Accelerators** ***Luca Benini****, ETH Zurich, Zurich, Switzerland*
4:10 PM	**Building Neuromorphic Circuits with Mixed CMOS/Emerging NVM Technologies: A Step Toward Embedded Cognitive Devices?** ***Christian Gamrat****, CEA Leti, Grenoble, France*
5:00 PM	Conclusion

F4: Wireless Low-Power Transceivers for Local and Wide-Area Networks

Organizer: **Jan van Sinderen,** *NXP Semiconductors, Eindhoven, The Netherlands*

Committee: **Danielle Griffith,** *Texas Instruments, Dallas, TX*
Ken Yamamoto, *Sony Semiconductor Solutions, Okata Atsugi-shi, Japan*
Antonio Liscidini, *University of Toronto, Toronto, Canada*
Young-sub Yuk, *SK Hynix, Gyeongchung-daero, Korea*

An overview and comparison is provided of the different emerging wireless standards and their circuit solutions, which target low data-rate IoT applications, featuring ultra-low-power and/or long-range. Different RF transceiver implementations are presented, including proprietary solutions in license-free spectrum, WLAN-based IEEE802.11ah solutions and mobile operators' alternatives based on emerging long-term evolution (LTE-M) standards. The different approaches coming to the market and their circuit design aspects will be discussed.

Forum Agenda

Time:	Topic:
8:00 AM	Breakfast
8:20 AM	Introduction by Chair
8:30 AM	**Emerging Standards for Low-Power IoT from BLE to Wide Area Networking Solutions** ***Thomas Almholt****, Texas Instruments, Dallas, TX*
9:20 AM	**Ultra-Narrow-Band Transceiver for M2M and IoT – System and Design Challenges** ***Alastair Hopper,*** *NXP Semiconductors, Gratkorn, Austria*
10:10 AM	Break
10:35 AM	**Ultra-Low-Power WiFi-Based 802.11ah Transceiver Design for IoT Applications** ***Yao-Hong Liu,*** *Holst Centre/IMEC, Eindhoven, The Netherlands*
11:25 AM	**Circuit Design Challenges and Solutions for 3GPP NB-IoT** ***Eric Wang,*** *Ericsson, San Jose, CA*
12:15 PM	Lunch
1:20 PM	**RF Design Challenges and Solutions for 3GPP Machine-Type Communications** ***Jon Strange****, Mediatek, Kent, United Kingdom*
2:10 PM	**Ultra-Low-Power IoT Transceivers** ***Sang-Gug Lee****, KAIST, Daejeon, Korea*
3:00 PM	Break
3:20 PM	**Low-Power Techniques in BLE Transceivers** ***Hisayasu Sato****, Renesas, Itami, Japan*
4:10 PM	**Batteryless IoT Wireless Networks: Challenges and Trends** ***Pascal Urard****, STMicroelectronics, Crolles, France*
5:00 PM	Closing remarks by Chair

F5: Wireline Transceivers for Mega Data Centers: 50Gb/s and Beyond

Organizer: **Yohan Frans**, *Xilinx, San Jose, CA*

Committee: **Ichiro Fujimori,** *Broadcom, Irvine, CA*
Seung-Jun Bae, *Samsung, Gyenggi, Korea*
Sam Palermo, *Texas A&M University, College Station, TX*
Hideyuki Nosaka, *NTT, Atsugi, Japan*
Simone Erba, *STMicroelectronics, Pavia, Italy*

With the explosive data growth due to HD video content, IoT, and the rapid shift from enterprise to cloud computing, Mega Data Centers have become an essential part of the global network infrastructure. Despite their massive scale, Data Center architectures require software-defined network capability and scalability, with lower latency. Interconnects will need to support diversified media-types, higher data-rates (>50Gb/s per lane), and longer distance (up to 2km) to achieve this and still make economic sense. Once a niche for mainly VCSEL links in HPC, "Optical Ethernet" is now becoming mainstream as interconnects for both MMF and SMF in various fiber configurations are being defined within the standards. Also, copper links including backplane continue to be the interconnect with highest volume. The Forum will cover various wireline transceivers enabling Mega Data Centers such as ADC-based transceivers and Silicon Photonics, and challenges moving forward.

Forum Agenda

Time:	Topic:
8:00 AM	Breakfast
8:20 AM	Introduction
8:30 AM	**Hyper-Scale Data Center – Pushing Bandwidth Requirements** ***Mike Andrewartha,*** *Microsoft, Redmond, WA*
9:20 AM	**256GB/s High-Bandwidth Memory Interface for Next-Generation Data Center** ***Kyomin Sohn,*** *Samsung Electronics, Hwaseong-si, Korea*
10:10 AM	Break
10:35 AM	**25-to-50Gb/s Mixed-Signal Wireline Transceiver for Copper Backplane and Cable Interconnects** ***Parag Upadhyaya,*** *Xilinx, San Jose, CA*
11:25 AM	**50Gb/s+ ADC/DAC-Based Wireline Transceivers** ***Aaron Buchwald,*** *Inphi, Santa Clara, CA*
12:15 PM	Lunch
1:20 PM	**VCSEL-Based Transceivers for MMF Data-Center Interconnects** ***Thé Linh Nguyen,*** *Finisar, Sunnyvale, CA*
2:10 PM	**Silicon Photonics Platform for 50G Optical Interconnects** ***Michal Rakowski,*** *imec, Leuven, Belgium*
3:00 PM	Break
3:20 PM	**For Ultra-Dense Silicon Photonic Interconnect: Hybrid Integration and Electrical-Optical Co-Design** ***Akinori Hayakawa,*** *Photonics Electronics Technology Research Association, Atsugi, Kanagawa, Japan*
4:10 PM	**Large-Scale Electronic/Photonic Integration to Transform Future Data Centers** ***Clint Schow,*** *University of California, Santa Barbara, Santa Barbara, CA*
5:00 PM	Concluding Remarks

F6: Pushing the Performance Limit in Data Converters

Organizers: **Venkatesh Srinivasan,** *Texas Instruments, Dallas, TX*
Kostas Doris, *NXP Semiconductors, Eindhoven, The Netherlands*

Moderator: **David Robertson,** *Analog Devices, Wilmington, MA*

Committee: **Seung-Tak Ryu,** *KAIST, Daejeon, Korea*
Seng-Pan U. (Ben), *University of Macau, Macau, China*

Data converters continue to push the boundaries of performance by achieving higher sampling speeds and wider bandwidths. In today's data converters, GS/s is starting to become common-place. This forum brings together experts from industry and academia to talk about recent advancements that have enabled these breakthroughs. These experts will present the state-of-the-art and address design challenges pertaining to a wide range of topics (GS/s pipes & multi-GHz sampling in DS Modulators, high-speed SAR ADCs, high-speed DACs, hybrid data converters and time-domain converters). The forum will conclude with a panel discussion with the speakers.

Forum Agenda

Time:	Topic:
8:00 AM	**Breakfast + Forum Opening**
8:30 AM	**Pushing the Boundaries of Performance – A Technology Perspective** ***Marcel J.M. Pelgrom,*** *Pelgrom Consult, Helmond, The Netherlands*
9:20 AM	**Wideband GHz-Sampling ΔΣ Modulators for Wireless Communications** ***Muhammed Bolatkale,*** *NXP Semiconductors, Eindhoven, The Netherlands*
10:10 AM	Break
10:35 AM	**Design Techniques for Multi-GS/s and High-Performance Pipelined ADCs** ***Manar El-Chammas,*** *Texas Instruments, Dallas, TX*
11:25 AM	**Advanced SAR ADCs for High-Throughput Applications** ***Ron Kapusta,*** *Analog Devices, Wilmington, MA*
12:15 PM	Lunch
1:20 PM	**High Speed Linear Digital-to-Analog Converters** ***Arthur H.M. van Roermund,*** *Eindhoven University of Technology, Eindhoven, The Netherlands*
2:10 PM	**Best of Both Worlds – Hybrid Data Converters** ***Michael Flynn,*** *University of Michigan, Ann Arbor, MI*
3:00 PM	Break
3:20 PM	**Quantizing Time: Time-Domain Converters** ***SeongHwan Cho,*** *KAIST, Daejeon, Korea*
4:10 PM	**Panel Discussion – Q&A, Moderator:** ***David Robertson,*** *Analog Devices, Wilmington, MA*
5:00 PM	Closing Remarks

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HOW TO REGISTER FOR ISSCC

Online: This is the fastest, most convenient way to register and will give you immediate email confirmation of your events. To register online (which requires a credit card), go to the ISSCC website at www.isscc.org and select the link to the registration website.

FAX, mail or email: Use the "2017 IEEE ISSCC Registration Form" which can be downloaded from the registration website. All payments must be made in U.S. Dollars, by credit card or check. Checks must be made payable to "ISSCC 2017". It will take several days before you receive email confirmation when you register using the form. **Registration forms received without full payment will not be processed until payment is received at YesEvents.** Please read the descriptions and instructions on the back of the form carefully.

On site: The On-site Registration and Advance Registration Pickup Desks at ISSCC 2017 will be located in the Yerba Buena Ballroom Foyer at the San Francisco Marriott Marquis. All participants, except as noted below, should register or pick up their registration materials at these desks as soon as possible. **Pre-registered Presenting Authors and pre-registered members of the ISSCC Program and Executive Committees must go to the Nob Hill Room, Ballroom level, to collect their conference materials.**

REGISTRATION DESK HOURS:

Saturday	February 4	4:00 pm to 7:00 pm
Sunday	February 5	6:30 am to 8:30 pm
Monday	February 6	6:30 am to 3:00 pm
Tuesday	February 7	8:00 am to 3:00 pm
Wednesday	February 8	8:00 am to 3:00 pm
Thursday	February 9	7:00 am to 2:00 pm

Students must present their Student ID at the Registration Desk to receive the student rates. Those registering at the IEEE Member rate must provide their IEEE Membership number.

Deadlines: The deadline for registering at the Early Registration rates is 11:59 pm Pacific Time **Sunday January 8, 2017.** After January 8th, and on or before 11:59 pm Pacific Time **Sunday January 15, 2017**, registrations will be processed **at the Late Registration rates. After January 15th, you must register at the on-site rates.** You are urged to register early to obtain the lowest rates and ensure your participation in all aspects of ISSCC.

Cancellations/Adjustments/Substitutions: Prior to 11:59 pm Pacific Time **Sunday January 15, 2017,** conference registration can be cancelled. Fees paid will be refunded (less a processing fee of $75). Registration category or credit card used can also be changed (for a processing fee of $35). Send an email to the registration contractor at ISSCCinfo@yesevents.com to cancel or make other adjustments. **No refunds will be made after 11:59 pm Pacific Time January 15, 2017.** Paid registrants who do not attend the conference will be sent all relevant conference materials. Transfer of registration to someone else is allowed with **WRITTEN** permission from the original registrant.

IEEE Membership Saves on ISSCC Registration

Take advantage of reduced ISSCC fees by joining the Solid-State Circuits Society today, or by using your IEEE membership number. If you're an IEEE member and have forgotten your member number, simply phone IEEE at 1(800) 678-4333 and ask. IEEE membership staff will take about two minutes to look up your number for you. If you come to register on site without your membership card, you can phone IEEE then, too. Or you can request a membership number look-up by email by using the online form at: www.ieee.org/about/help/member_support.html. If you're not an IEEE member, consider joining before you register to save on your fees. Join online at www.ieee.org/join any time and you'll receive your member number by email. If you join IEEE at the conference, you can also select a free Society membership. This offer is not available to existing IEEE members.

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-Access exclusive SSCS Conference Digests for ISSCC, CICC, A-SSCC, ESSCIRC, and Symposium on VLSI Circuits.

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SSCS Membership Saves Even More on ISSCC Registration

This year, SSCS members will again receive an exclusive benefit of a $40 discount on the registration fee for ISSCC in addition to the IEEE discount. Also, the SSCS will again reward our members with a $10 Starbucks gift card when they attend the Conference as an SSCS member in good standing.

Join or renew your membership with IEEE's Solid-State Circuit Society today at sscs.ieee.org – you will not want to miss out on the opportunities and benefits your membership will provide now and throughout your career.

ITEMS INCLUDED IN REGISTRATION

Technical Sessions: Registration includes admission to all technical and evening sessions starting Sunday evening and continuing throughout Monday, Tuesday and Wednesday. ISSCC does not offer partial conference registrations.

Technical Book Display: Several technical publishers will have collections of professional books and textbooks for sale during the Conference. The Book Display will be open on Monday from Noon to 7:00 pm; on Tuesday from 10:00 am to 7:00 pm; and on Wednesday from 10:00 am to 3:00 pm.

Demonstration Sessions: Hardware demonstrations will support selected papers.

Author Interviews: Author Interviews will be held Monday, Tuesday and Wednesday evenings. Authors from each day's papers will be available to discuss their work.

Social Hour: Social Hour refreshments will be available starting at 5:15 pm.

University Events: Several universities are planning social events during the Conference. Check the University Events display at the conference for the list of universities, locations and times of these events.

ISSCC Water Bottle: A convenient water bottle for travel or sports will be given to all Conference registrants.

Publications: Conference registration includes:

-The **Digest of Technical Papers** in hard copy and by download. The Digest book will be distributed during registration hours beginning on Sunday at 10:00 am.

-**Papers Visuals:** The visuals from all papers presented will be available by download.

-**Demonstration Session Guidebook:** A descriptive guide to the Demonstration Session will be available by download.

-**Note:** Instructions will be provided for access to all downloads. Downloads will be available both during the Conference and for a limited time afterwards.

OPTIONAL EVENTS

Educational Events: Many educational events are available at ISSCC for an additional fee. There are ten 90-minute Tutorials and two all-day Forums on Sunday. There are four additional all-day Forums on Thursday as well as an all-day Short Course. All events include a course handout in color. The Forums and Short Course include breakfast, lunch and break refreshments. The Tutorials include break refreshments. See the schedule for details of the topics and times.

Women's Networking Event: ISSCC will be offering a networking event for women in solid-state circuits on **Monday at 12:15 pm**. This luncheon is an opportunity to hear from an accomplished speaker, get to know other women in the profession and discuss a range of topics including leadership, work-life balance, and professional development.

Young Professionals, Faculty & Students Mentoring & Career Coaching Session:
Tuesday 6-7 PM, Foothill E. This is a complimentary session for all conference attendees (Atrium Level). Leading experts from industry and academia will answer your questions 1-on-1. Complimentary snacks and beverages will be available for all participants, as well student participants will receive a 1-year complimentary SSCS membership. For further information see: http://sscs.ieee.org/membership/young-professionals.

OPTIONAL PUBLICATIONS

ISSCC 2017 Publications: The following ISSCC 2017 publications can be purchased in advance or on site:

2017 ISSCC Download USB: All of the downloads included in conference registration **(mailed in March).**

2017 Tutorials DVD: All of the 90 minute Tutorials **(mailed in May).**

2017 Short Course DVD: "Ultra-LOW-Power Analog Design" **(mailed in May)**.

Short Course and Tutorial DVDs contain audio and written English transcripts synchronized with the presentation visuals. In addition, the Short Course DVD contains a pdf file of the presentations suitable for printing, and pdf files of key reference material.

Earlier ISSCC Publications: Selected publications from earlier conferences can be purchased. There are several ways to purchase this material:

-Items listed on the registration form can be purchased with registration and picked up at the conference.

-Visit the ISSCC Publications Desk. This desk is located in the registration area and has the same hours as conference registration. With payment by cash, check or credit card, you can purchase materials at this desk. See the posted list at the Conference for titles and prices.

-Visit the ISSCC website at www.isscc.org and click on the link "SHOP ISSCC" where you can order online or download an order form to mail, email or fax. For a small shipping fee, this material will be sent to you immediately and you will not have to wait until you attend the Conference to get it.

HOW TO MAKE HOTEL RESERVATIONS

Online: ISSCC participants are urged to make their hotel reservations at the San Francisco Marriott Marquis online. Go to the conference website and click on the Hotel Reservation link. **Conference room rates are $271 for a single/double, $296 for a triple and $321 for a quad** (per night plus tax). In addition, ISSCC attendees booked in the ISSCC group receive **in-room Internet access for free**. All online reservations require the use of a credit card. Online reservations are confirmed immediately. You should print the page containing your confirmation number and reservation details and bring it with you when you travel to ISSCC.

Telephone: Call 877-622-3056 (US) or 415-896-1600 and ask for "Reservations." When making your reservation, identify the group as ISSCC 2017 to get the group rate.

Hotel Deadline: Reservations must be received at the San Francisco Marriott Marquis no later than 5 pm Pacific Time January 12, 2017 to obtain the special ISSCC rates. A limited number of rooms are available at these rates. **Once this limit is reached or after January 12th, the group rates may no longer be available and reservations will be filled at the best available rate.** Changes: Before the hotel deadline, your reservation can be changed by calling the telephone numbers above. After the hotel deadline, call the Marriott Marquis at 415-896-1600 (ask for "Reservations"). Have your hotel confirmation number ready.

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REFERENCE INFORMATION

TAKING PICTURES, VIDEOS OR AUDIO RECORDINGS DURING ANY OF THE SESSIONS IS NOT PERMITTED

Conference Website:	www.isscc.org
ISSCC Email:	ISSCC@ieee.org
Registration questions:	ISSCCinfo@yesevents.com
Hotel Information:	San Francisco Marriott Marquis 780 Mission Street San Francisco, CA 94103 Phone: 415-896-1600
Press Information:	Kenneth C. Smith University of Toronto Email: lcfujino@aol.com Phone: 416-418-3034
Registration:	YesEvents 1700 Reisterstown Road #236 Baltimore, MD 21208 Email: issccinfo@yesevents.com Phone: 410-559-2200 or 800-937-8728 Fax: 410-559-2217

Hotel Transportation: Visit the ISSCC website "Attendees" page for helpful travel links and to download a document with directions and pictures of how to get from the San Francisco Airport (SFO) to the Marriott Marquis. You can get a map and driving directions from the hotel website at www.marriott.com/hotels/travel/sfodt-san-francisco-marriott-marquis/

Next ISSCC Dates and Location: ISSCC 2018 will be held on February 11-15, 2018 at the San Francisco Marriott Marquis Hotel.

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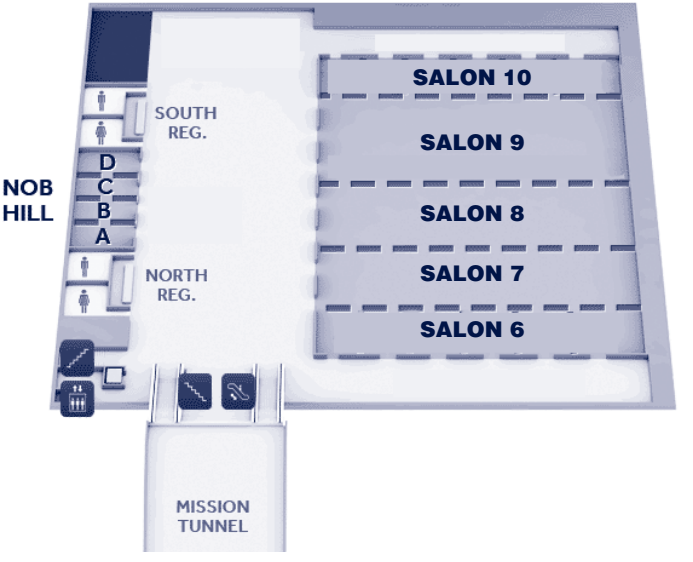
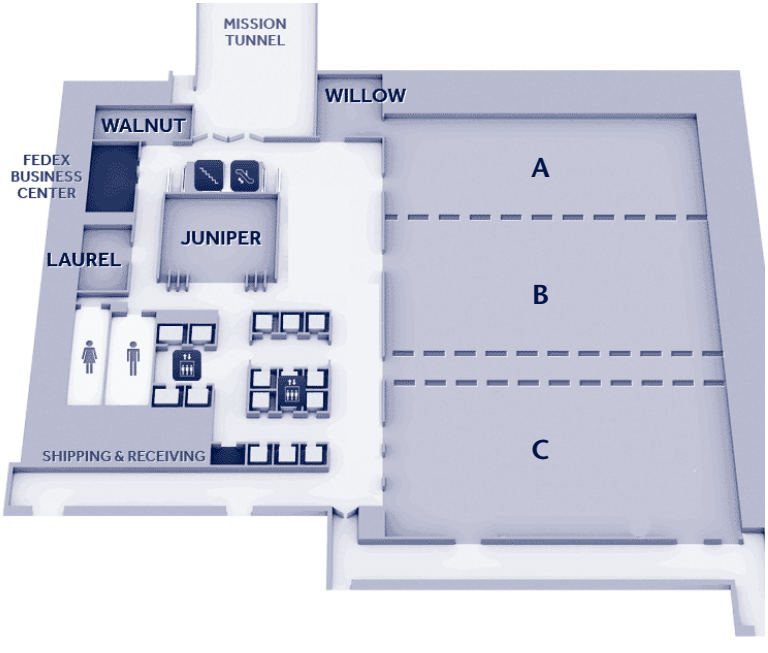
Lower B2 Level - Yerba Buena Ballroom



B2 Level - Golden Gate Hall



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