ADVANCE PROGRAM

2019 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

FEBRUARY 17, 18, 19, 20, 21

CONFERENCE THEME:

ENVISIONING THE FUTURE

SAN FRANCISCO MARRIOTT MARQUIS HOTEL

NEW THIS YEAR!

INDUSTRY SHOWCASE:
Featuring Future Industrial Products

STUDENT EVENT:
Making a Career Choice

IEEE SOLID-STATE CIRCUITS SOCIETY

5-DAY PROGRAM

SUNDAY ALL-DAY

2 FORUMS: 5G SUB-6GHZ RADIO; MEMORY-CENTRIC COMPUTING

10 TUTORIALS: INTEGRATED RADARS; POWER-CONVERSION TOPOLOGIES; ADVANCED IN-MEMORY COMPUTING; EFFICIENT IOT MICROCONTROLLERS; NOISE-SHAPING IN DATA CONVERTERS; CLOCK- & DATA-RECOVERY CIRCUITS; ASICS FOR HARDWARE SECURITY; CURRENT-SENSING TECHNIQUES; CALIBRATION OF WIRELESS TRANSCEIVERS; LOW-NOISE SENSOR INTERFACES

2 EVENING EVENTS: GRADUATE STUDENT RESEARCH IN PROGRESS; WIC: "HOW TO SAVE LIVES WITH CIRCUITS"

THURSDAY ALL-DAY

4 FORUMS: COMPLETE ADAS SENSING NETWORK; POWER EFFICIENCY OF ML; WIRELINE FROM 56 TO 112GB/S; APPLICATION-OPTIMIZED DATA CONVERTERS

SHORT-COURSE: INTEGRATED PHASED ARRAYS

ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and application to maintain technical currency, and to network with leading experts.

CONFERENCE TECHNICAL HIGHLIGHTS

On Sunday, February 17th, the day before the official opening of the Conference, ISSCC 2019 offers:

- A choice of up to 4 of a total of 10 Tutorials, or
- A choice of 1 of 2 all-day Advanced-Circuit-Design Forums

The 90-minute tutorials offer background information and a review of the basics in specific circuit- and system-design topics. In the all-day Advanced-Circuit-Design Forums, leading experts present state-of-the-art design strategies in a workshop-like format. The Forums are targeted at designers experienced in the technical field.

On Sunday evening, there are two events: A WiC Workshop on "How to Save Lives with Circuits" will be offered starting at 6:00 pm. In addition, the Student-Research Preview, featuring 20 ninety-second introductory presentations followed by a poster session from selected graduate-student researchers from around the world will begin at 7:30 pm. Introductory remarks at the Preview will be provided by a distinguished member of the solid-state circuit community, Marian Verhelst, Professor, KU Leuven.

On Monday, February 18th, ISSCC 2019 at 8:30 am offers four plenary papers on the theme: "Envisioning the Future". On Monday at 1:30 pm, there begin five parallel technical sessions, followed by a Social Hour at 5:15 pm open to all ISSCC attendees. The Social Hour, held in conjunction with Book Displays and Author Interviews, will also include a Demonstration Session, featuring posters and live demonstrations of selected papers from industry and academia. On Monday evening there are two separate events: At 7:00 pm Student Event: "Making a Career Choice", in which panelists from diverse areas present brief remarks followed by a Q&A session. At 8:00 pm "Industry Showcase", consisting of an introductory commentary followed by brief presentations by industrial contributors and subsequently an opportunity to participate in their demonstrations.

On Tuesday, February 19th, there are five parallel technical sessions, both morning and afternoon. A Social Hour open to all ISSCC attendees will follow. The Social Hour, held in conjunction with Book Displays and Author Interviews, will also include a second Demonstration Session. Tuesday evening includes two events, entitled "Moving to 'The Dark Side'!" and "How Can Hardware Designers Reclaim the Spotlight?".

On Wednesday, February 20th, there will be five parallel technical sessions, both morning and afternoon, followed by Author Interviews.

On Thursday, February 21st, ISSCC offers a choice of five all-day events:

- A Short Course entitled: "Integrated Phased Arrays:
  Theory, Practice, & Implementation for 5G & Beyond"
- Four Advanced-Circuit-Design Forums entitled:
  "The Complete ADAS Sensing Network"
  "Intelligence at the Edge: How Can we Make Machine Learning More Energy Efficient"
  "56Gs/s to 112Gb/s & Beyond — Design Challenges & Solutions in Wireline Communications"
  "The Right Tool for the Job: Application-Optimized Data Converters"

This year, for the second time, there is an option which allows an attendee to sample parts of all 5 Thursday offerings. Registration for educational events on Sunday and Thursday will be filled on a first-come first-served basis. Use of the ISSCC Web-Registration Site (http://www.isscc.org) is strongly encouraged. Registrants will be provided with immediate confirmation on registration for the Conference, Tutorials, Forums, and the Short Course.

Need Additional Information? Go to: www.isscc.org

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There are a total of 10 tutorials this year on 10 different topics. Each tutorial, selected through a competitive process within each subcommittee of the ISSCC, presents the basic concepts and working principles of a single topic. These tutorials are intended for non-experts, graduate students and practicing engineers who wish to explore and understand a new topic.

Ali Sheikholeslami
ISSCC Education Chair

8:30 AM

T1: Fundamentals of Integrated Radars

Brian Ginsburg, *Texas Instruments, Dallas, TX*

Radar is essential to modern aviation, meteorology, and automobiles, among others. This tutorial will cover the basic radar parameters including resolution, accuracy, and maximum range, and show how those are linked to fundamental system specifications. Modern highly integrated radars primarily use continuous-wave modulations, including FMCW and PMCW. High-level architectures and key circuits for a mm-wave implementation will be presented, along with a look at detection signal processing.

Brian Ginsburg received his S.B., M.Eng., and Ph.D. degrees from the Massachusetts Institute of Technology. He joined Texas Instruments, Dallas, Texas in 2007 working in its wireless terminals business unit and Kilby research labs. He is the systems manager of TI's Radar and Analytics Processors organization, developing mm-wave sensors for automotive and industrial applications. He serves on the ISSCC and VLSI Circuits Symposium Technical Program Committees.

8:30 AM

T2: Fundamentals of Power-Conversion Topologies

Robert Pilawa, *UC Berkeley, Berkeley, CA*

This tutorial will provide an overview of various power-converter topologies, with a focus on techniques to achieve high-efficiency and high-power density. A brief summary of common power converters, such as buck, boost, single-input multiple-output (SIMO) and multi-phase converters will be presented followed by a detailed analysis and comparison to more recent topologies, such as switched-capacitor (SC) power converters, hybrid and resonant SC converters, and multi-level converters.

Robert Pilawa-Podgurski is currently an Associate Professor in the Electrical Engineering and Computer Sciences Department at the University of California, Berkeley. He received his B.S., M.Eng., and Ph.D. degrees from MIT. He performs research in the area of power electronics. Dr. Pilawa-Podgurski received the Google Faculty Research Award in 2013, and the 2014 Richard M. Bass Outstanding Young Power Electronics Engineer Award of the IEEE Power Electronics Society, given annually to one individual for outstanding contributions to the field of power electronics before the age of 35. He is co-author of nine IEEE prize papers.

8:30 AM

T3: Advances and Prospects for In-Memory Computing

Naveen Verma, *Princeton University, Princeton, NJ*

As applications become more data centric, the cost of accessing data from memory dominates energy and throughput. An emerging paradigm to address this is in-memory computing. Early approaches show the potential to reduce energy-delay product (EDP) by 2-to-3 orders of magnitude. However, architectures for enabling computation within the constrained structure of memory raise new challenges and opportunities. This tutorial will map out advances in these areas and examine recent demonstrations.

Naveen Verma received the B.A.Sc. degree in Electrical and Computer Engineering from the UBC, Vancouver, Canada, in 2003, and the M.S. and Ph.D. degrees in Electrical Engineering from MIT in 2005 and 2009, respectively. Since July 2009, he has been with the Department of Electrical Engineering at Princeton, where he is currently an Associate Professor. His research focuses on advanced sensing systems and on exploring how systems for learning, inference, and action planning can be enhanced by algorithms that exploit new sensing and computing technologies. This includes research on large-area, flexible sensors, energy-efficient statistical-computing architectures and circuits, and machine-learning and statistical-signal-processing algorithms.

10:30 AM

T4: Fundamentals of Efficient IoT Microcontrollers

James Myers, *ARM, Cambridge, United Kingdom*

IOT microcontrollers are complex constrained SOCs with analog peripherals, DCDC converters, CPUs, accelerators, volatile/non-volatile memories, and radios – all well represented at ISSCC.

However state-of-the-art circuits do not automatically translate to a state-of-the-art system. This tutorial presents an overview of system components and their system efficiency considerations, using published systems as examples. Future trends, such as battery-free energy harvesting, will also be covered.

James Myers leads the Devices, Circuits and Systems team within Arm Research, which seeks to push compute to the furthest extremes of cost, efficiency, performance, and integration. He joined Arm in 2007 initially responsible for reference implementation flows for the whole processor family. Joining R&D full time from 2009, he has since focused on deployable techniques for reduction of CPU and SoC power, embodied across more than a dozen tapeouts. James holds 20 granted and 16 pending US patents, co-authored one book chapter, and has presented at ISSCC and VLSI Circuits Symposium. His current interests include energy harvesting, printed electronics, sub-threshold circuits, and better-than-worst-case design.

10:30 AM

T5: Noise-Shaping in Data Converters

Venkatesh Srinivasan, *Texas Instruments, Dallas, TX*

Noise shaping is a powerful technique that helps improve the overall accuracy of a data converter. While this technique is widely used in the context of $\Delta\Sigma$ modulators, noise shaping is also gaining popularity in other kinds of converters such as SARs. This tutorial will present the fundamentals of noise shaping along with the architectural view of their application in different data converters such as $\Delta\Sigma$ modulators and SARs. Circuit implementation of key building blocks along with challenges in realization and their mitigation strategies will be discussed as well.

Venkatesh Srinivasan received his B.E (Hons) in Electrical and Electronic Engineering from Birla Institute of Technology and Science, Pilani, India in 1999 and his M.S and Ph.D. degrees in Electrical and Computer Engineering from the University of Tennessee, Knoxville and Georgia Institute of Technology, Atlanta in 2002 and 2006 respectively. Since 2006, he has been with Texas Instruments leading the architecture, design and development of multiple RF, Analog and high-speed $\Delta\Sigma$ modulators for wireless transceivers. He is the author/co-author of 27 publications in IEEE Journals and Conferences and has been issued 14 US patents. He is the recipient of the Best Student Paper Award from IEEE CICC in 2005. He currently serves on the Technical Program Committee of ISSCC.

10:30 AM

T6: Basics of Clock-and-Data-Recovery Circuits

Amir Amirkhany, *Samsung Electronics, San Jose, CA*

The choice of the clock-and-data-recovery (CDR) architecture in serial links dictates many of the block-level circuit specs. In the first half of this tutorial we will discuss the basics of CDR operation, CDR main performance metrics, and the relationship between circuit-level parameters and system-level performance metrics. In the second half, we will review various CDR architectures and their associated design trade-offs. We will conclude with the review of a few practical CDR design considerations.

Amir Amirkhany is a Director of Engineering at Samsung Display America Lab, San Jose, CA. He received his B.S. from Sharif University of Technology, M.S. from University of California, Los Angeles, and Ph.D. from Stanford University, all in Electrical Engineering. At Samsung Electronics, Dr. Amirkhany is in charge of the development of future generations of high-speed interfaces for Samsung displays. Prior to Samsung, he was an engineering manager at Rambus Inc., where he led the development of DDR and proprietary high-speed memory interfaces. Dr. Amirkhany has authored or co-authored over 25 IEEE conference and journal papers, including a best paper award, and has over 50 issued US patents.

1:30 PM

T7: Hardware Security – from Basics to ASICs

Massimo Alioto, *National University of Singapore, Singapore*

Many applications require security to be rooted in hardware, due to constrained resources or demanding security levels (e.g., IoT, automotive, e-wallets). This tutorial introduces state-of-the-art techniques to create security primitives (e.g., PUFs, TRNGs, ciphers), and counteract hardware attacks.

At the end of the tutorial, attendees will understand basic principles of HW security, its state of the art and the challenges ahead, with emphasis on low-cost techniques for pervasive adoption.

Massimo Alioto directs the Integrated Circuits and Embedded Systems area, and leads the Green IC group at the National University of Singapore. He held visiting positions at the University of California Berkeley (BWRC), University of Michigan Ann Arbor, Intel Labs, EPFL, and positions at the University of Siena.

He is author of 250+ publications and three books, focusing on ultra-low power integrated system design, widely energy-scalable circuits, and hardware security, among others.

He is Editor in Chief of IEEE Transactions on VLSI Systems, and was Deputy Editor in Chief of IEEE JETCAS, Guest Editor of various IEEE journal special issues, Program Chair of several IEEE conferences, and an IEEE Distinguished Lecturer. He is an IEEE Fellow.

1:30 PM

T8: Current-Sensing Techniques

Mahdi Kashmiri, *Robert Bosch, Sunnyvale, CA*

Current-sensing is an essential part of a wide range of applications from hand-held products to the electro-mobility drivetrains. The state of charge in a battery and the control of an electromotor or a power converter have specific demands for dynamic-range, precision, speed, isolation, size, and cost. This tutorial provides an overview of the principles of operation and readout techniques for the two current-sensing approaches: Contacted (shunt-based) and contactless (Hall, fluxgate, transformer, AMR/GMR based).

Mahdi Kashmiri received his B.Sc. from Tehran University and his M.Sc. and Ph.D. in Microelectronics from Delft University of Technology, Delft, The Netherlands. From 2010 to 2016 he was with Texas Instruments Inc. in Delft and Santa Clara locations, where he worked on precision products including AFEs for low-power ECG, shunt-based current and voltage monitor, contactless current sensor based on integrated Fluxgate and automotive and industrial ultrasound. Since 2016 he has been with the Mixed-signal ASICs group of Robert Bosch Research and Technology Center in Sunnyvale, CA, where he works on ASICs for automotive Lidar. He received the ESSCIRC 2009 Young Scientist Award and is an ISSCC member of the Analog technical program committee.

3:30 PM

T9: Calibration Techniques for Wireless Transceivers

David McLaurin, *Analog Devices, Raleigh, NC*

Modern wireless transceivers are expected to meet aggressive performance, cost, and power consumption targets with adequate yield in short design cycles. To address these challenges, RFICs are relying extensively on calibration techniques. This tutorial presents the impact of analog/RF non-idealities on key radio metrics and will cover techniques to address topics such as IQ imbalance, LO feed-through, IIP2 nonlinearities, analog filter tuning, full duplex radio and phased array calibrations.

David McLaurin joined Analog Devices in 2000, designing high speed pipeline ADCs. In 2002 he joined an RF IC team in Raleigh, NC, where he architects and designs wideband reconfigurable wireless transceivers. David graduated from the Georgia Institute of Technology (MSEE 2000), and North Carolina State University (BSEE 1998). He has been serving as a member of the technical program committee of ISSCC since 2016.

3:30 PM

T10: Low-Noise Sensor Interfaces

Pedram Lajevardi, *Robert Bosch, Sunnyvale, CA*

Applications, such as autonomous driving, rely on the perception of the environment around us based on extensive sensing. While most signals in the nature are not changing quickly and can be captured with relatively low-bandwidth sensors, most require low-noise sensors. This tutorial goes over the main sources of noise with a focus on capacitive and image sensors. Advanced noise-reduction circuit techniques, such as chopping, correlated-double sampling, and Boxcar sampling, are explained.

Pedram Lajevardi received B.A.Sc. degree in Electrical and Computer Engineering from the University of British Columbia and MS and Ph.D. in Electrical Engineering from Stanford University. He joined Bosch Research and Technology Center, Sunnyvale, CA in 2012 working on CMOS image sensors. Since 2015 he has been serving as a member of the technical program committee of ISSCC. His research interests are low-power and high-precision sensor interfaces.

F1: Sub-6GHz 5G Radio Circuits and Systems: From Concepts to Silicon

Organizer: **Theodoros Georgantas,** *Broadcom, Athens, Greece*

Committee: **Chan-Hong Chern,** *TSMC, Hsinchu, Taiwan*
Xin He, *NXP, Eindhoven, The Netherlands*
Yen-Hsun Hsu, *MediaTek, Hsinchu, Taiwan*
Harish Krishnaswamy, *Columbia University, New York, NY*
Hua Wang, *Georgia Institute of Technology, Atlanta, GA*

The next-generation cellular (5G) will offer Gb/s data rates with high spectral efficiency and minimal latency. To meet these performance targets and provide an optimal balance between coverage and implementation cost, 5G deployments in sub-6GHz bands will coexist with LTE and employ broadband operation along with massive MIMO and beamforming. This forum will describe how 5G requirements affect radio designs below 6GHz, current state-of-the-art of 5G systems, and what the future directions of key circuits and system architectures are. In addition, power efficiency along with various challenges and solutions on silicon integration of 5G radios will be also addressed.

Forum Agenda

Time	Topic
8:00 AM	Breakfast
8:20 AM	**Introduction**
8:30 AM	**Overview of Radio RF Systems Requirements and Challenges for Sub-6GHz 5G NR Commercialization** ***Walid Ali-Ahmad,*** *Facebook, Menlo Park, CA*
9:20 AM	**Multiband Receivers for LTE-A/5G Systems** ***Thomas Byunghak Cho,*** *Samsung Electronics, Suwon, Korea*
10:10 AM	Break
10:30 AM	**Digital Transmitters for Sub-6GHz Wireless Applications** ***Leo de Vreede,*** *Delft University of Technology, Delft, The Netherlands*
11:20 AM	**High-Power, High-Bandwidth, and High-Efficiency Supply Modulator for 5G System** ***Paul Liang,*** *MediaTek, Hsinchu, Taiwan*
12:10 PM	Lunch
1:10 PM	**Massive MIMO for Sub-6GHz Wireless Communications** ***Ove Edfors,*** *Lund University, Lund, Sweden*
2:00 PM	**RF Transceivers for 5G Basestations** ***Tony Montalvo,*** *Analog Devices, Raleigh, NC*
2:50 PM	Break
3:10 PM	**Power Amplifier Linearity and Efficiency Challenges for Sub-6GHz 5G Systems** ***Christian Fager,*** *Chalmers University of Technology, Gothenburg, Sweden*
4:00 PM	**Silicon Technologies for Sub-6GHz Front-End and Radio Integrations** ***Alvin Joseph,*** *GlobalFoundries, Burlington, VT*
4:50 PM	Conclusion

F2: Memory-Centric Computing from IoT to Artificial Intelligence and Machine Learning

Organizer: **Fatih Hamzaoglu,** *Intel, Hillsboro, OR*

Committee: **Meng-Fan Chang,** *National Tsing Hua University, Hsinchu, Taiwan*
Ki-Tae Park, *Samsung, Hwaseong, Korea*
Yasuhiko Taito, *Renesas, Kodaira, Tokyo, Japan*
Alicia Klinefelter, *Nvidia, Durham, NC*
Naveen Verma, *Princeton University, Princeton, NJ*

This forum will present state-of-the-art memory-centric architectures, as well as future innovative solutions to enable energy-efficient, high-performance AI/ML applications. It will also describe the challenges and solutions from edge processors to cloud applications, such as algorithmic accuracy, cost, security and practicality, including technology readiness to areas where further technology development is needed. At the high-performance and machine-learning end, emerging and storage-class memories are going to change the memory hierarchy. Meanwhile, low-power high-bandwidth DRAMs and SRAMs continue to be innovated around, to remain the workhorses of the latest process nodes (HBM, GDDR6, 7nm-FinFET SRAM etc.). Furthermore, with the explosive growth of memory intensive workloads like machine learning, video capture/playback, language translation, etc. there is a tremendous interest in preforming some compute near memory, by placing logic inside the DRAM/NVM main-memory die (AKA near-memory compute), or even doing the compute within the SRAM/STTRAM/RRAM array embedded within the compute die (AKA in-memory compute). In either case, the motivation is to reduce the significant data movement between main/embedded memory and compute units, as well as to reduce latency by preforming many operations in parallel, inside the array. Many challenges to productize these ideas remain to be addressed, including area-cost trade-offs for adding logic in the memory die for near-memory compute or augmenting embedded arrays with mixed-signal circuits to enable in-memory compute. Noticeable degradation of S/N ratio, especially in the in-memory compute case, is lurking and may direct its use to specific applications.

Forum Agenda

Time	Topic
8:00 AM	Breakfast
8:20 AM	**Introduction by Chair, *Fatih Hamzaoglu,*** *Intel, Hillsboro, OR*
8:30 AM	**Hardware-Enabled AI, *Bill Dally,*** *Nvidia, Santa Clara, CA*
9:20 AM	**Embedded Memory Solutions for AI, ML and IoT** ***Masanori Hayashikoshi,*** *Renesas, Kodaira, Tokyo, Japan*
10:10 AM	Break
10:35 AM	**High-Bandwidth Memory (HBM) DRAM for Energy-Efficient Near-Memory Computing, *Kyomin Sohn,*** *Samsung, Hwasung, Korea*
11:25 AM	**Novel Memory/Storage Solutions for Memory-Centric Computing** ***Mohamed Arafa,*** *Intel, Chandler, AZ*
12:15 PM	Lunch
1:20 PM	**The Deep In-memory Architecture for Energy Efficient Machine Learning** ***Naresh Shanbhag,*** *UIUC, Urbana, IL*
2:10 PM	**Low Power SRAM for IoT and ML Applications** ***YK Chong,*** *ARM, Austin, TX*
3:00 PM	Break
3:20 PM	**Advanced Memory, Logic and 3D Technologies for In-Memory Computing and Machine Learning** ***Stefan Cosemans,*** *IMEC, Leuven, Belgium*
4:10 PM	**Deep-Learning Hardware Acceleration: Opportunities in Memory Design** ***Leland Chang,*** *IBM, Yorktown Heights, NY*
5:00 PM	Closing Remarks by Chair

EE1: Student Research Preview (SRP)

The Student Research Preview (SRP) will highlight selected student research projects in progress. The SRP consists of 20 ninety-second presentations followed by a Poster Session, by graduate students from around the world, which have been selected on the basis of a short submission concerning their on-going research. Selection is based on the technical quality and innovation of the work. This year, the SRP will be presented in three theme sections: Digital and Machine Learning Circuits and Systems; Data Converters and Clocking; Analog and Wireless Circuits.

The Student Research Preview will include the talk "Machine Learning: The Next Big Opportunity for Chip Designers" by Professor Marian Verhelst, KU Leuven. The SRP begins at 7:30 pm on Sunday, Febuary 17th. SRP is open to all ISSCC registrants.

Co-Chair:	Denis Daly	Omni Design Technologies, MA
Co-Chair:	Makoto Ikeda	University of Tokyo, Japan
Secretary:	Jerald Yoo	National University of Singapore, Singapore
Advisor:	Jan Van der Spiegel	University of Pennsylvania, PA
Advisor:	Anantha Chandrakasan	Massachusetts Institute of Technology, MA
Media/Publications:	Laura Fujino	University of Toronto, Canada
A/V:	Trudy Stetzler	Houston, TX

Committee Members

Jason Anderson	University of Toronto, Canada
Masoud Babaie	Delft University of Technology, Netherlands
Andrea Baschirotto	University of Milan-Bicocca, Italy
Ben Calhoun	University of Virginia, VA
Hayun Chung	Korea University, Korea
Denis Daly	Omni Design Technologies, MA
Shidhartha Das	ARM, United Kingdom
Andreas Demosthenous	University College London, United Kingdom
Makoto Ikeda	University of Tokyo, Japan
Seulki Lee	IMEC-NL, Netherlands
Yoonmyung Lee	SungKyunKwan University, Korea
Salvatore Levantino	Politecnico di Milano, Italy
Qiang Li	University of Electronic Science & Tech., China
Shih-Chii Liu	University of Zurich / ETH Zurich, Switzerland
Shahriar Mirabbasi	University of British Columbia, Canada
Tinoosh Mohsenin	University of Maryland, MD
Cormac O'Connell	TSMC, Canada
Mondira Pant	Intel, MA
Shanthi Pavan	Indian Institute of Technology, India
Jae-sun Seo	Arizona State University, AZ
Mingoo Seok	Columbia University, NY
Farhana Sheikh	Intel, OR
Bing Sheu	Chang Gung University, Taiwan
Atsushi Shirane	Tokyo Institute of Technology, Japan
GuoXing Wang	Shanghai Jiao Tong University, China
Jeffrey Weldon	University of Hawaii, HI
Chia-Hsiang Yang	National Taiwan University, Taiwan
Rabia Tugce Yazicigil	Boston University, MA
Jerald Yoo	National University of Singapore, Singapore
Samira Zaliasl	Ferric, New York, NY
Milin Zhang	Tsinghua University, China

EE2: How to Save Lives with Circuits

Chair: ***Kathy Wilcox,*** *AMD, Boxborough, MA*
Organizers: ***Edith Beigné,*** *Facebook, Menlo Park, CA*
Dina El-Damak, *University of Southern California, Los Angeles, CA*
Azita Emami, *California Institute of Technology, Pasadena, CA*
Ulkuhan Guler, *Worcester Polytechnic Institute, Worcester, MA*
Rikky Muller, *University of California, Berkeley, Berkeley, CA*
Mandy Pant, *Intel, Hudson, MA*
Negar Reiskarimian, *Columbia University, New York, NY*
Abira Sengupta, *IEEE SSCS, Piscataway, NJ*
Farhana Sheikh, *Intel, Hillsboro, OR*
Trudy Stetzler, *Haliburton, Houston, TX*
Vivienne Sze, *Massachusetts Institute of Technology, Cambridge, MA*
Ingrid Verbauwhede, *KU Leuven, Leuven, Belgium*
Alice Wang, *PsiKick, Santa Clara, CA*
Rabia Tugce Yazicigil, *Boston University, Boston, MA*

The workshop highlights circuits and their impact on healthcare-related industries. The goal of the panel is to provide perspectives from system architects, security experts and circuit designers on where we should be heading with the large amount of data that is being generated from more-advanced tests and increased monitoring of our current health status.

Distinguished Speakers

6:00 - 6:30 PM

Catalyzing Growth and Innovation
Sue Siegel, *GE Chief Innovation Officer and CEO, GE Business Innovations*

6:30 - 7:00 PM

Better Circuits for a Better World
Dr. Jennifer Lloyd, *VP, Healthcare and Consumer, Analog Devices*

Invited Talks

7:00 - 7:20 PM

Unravelling the Brain with High-Density CMOS Neural Probes
Dr. Carolina Mora Lopez, *Team Leader, Circuits for Neural Interfaces at imec*

7:20 - 7:40 PM

Neurotechnology: Where Engineering Meets Neuroscience
Dr. Hyunjoo J. Lee, *Assistant Professor Electrical Engineering, KAIST*

Panel

7:45 - 9:00 PM

What Can Circuit Designers Do to Bolster Security in AI-driven Healthcare

Moderator: ***Ingrid Verbauwhede,*** *KU Leuven, Leuven, Belgium*

Security and privacy problems with medical devices and IOT devices in general are in the news on an almost daily basis. One example from 2017 stated: "FDA issues recall of 465,000 pacemakers to patch security holes." Once medical data is obtained reliably and securely, it is stored on remote servers and in remote databases where there are risks of leaks and data breaches of private medical records. However, it is difficult to put the genie back into the bottle! We have asked our distinguished panel to discuss how circuit designers can contribute to bolster our trust in medical devices and in electronic healthcare systems that manage private medical records. We also encourage the audience to propose attacks and countermeasures.

Distinguished Speaker

7:45 - 8:15 PM

Perspectives on Machine Learning and Cryptography by Turing Award Winner Shafi Goldwasser
Shafi Goldwasser, *Professor Electrical Engineering and Computer Sciences, University of California at Berkeley, Berkeley, CA*

Panelists

Alison Burdett, *Sensium Healthcare, Abingdon, United Kingdom*
Shafi Goldwasser, *University of California at Berkeley, Berkeley, CA*
Rikky Muller, *University of California at Berkeley, Berkeley, CA*
Sugako Otani, *Renesas Electronics Corporation, Tokyo, Japan*
Vivienne Sze, *Massachusetts Institute of Technology, Cambridge, MA*
Wenyuan Xu, *Zhejiang University, Hangzhou, China*

Plenary Session — Invited Papers

Chair: ***Jan van der Spiegel,*** *University of Pennsylvania, Philadelphia, PA*
ISSCC Conference Chair

Associate Chair: ***Eugenio Cantatore,*** *Eindhoven University of Technology, Eindhoven, The Netherlands*
ISSCC International Technical Program Chair

FORMAL OPENING OF THE CONFERENCE **8:30 AM**

1.1 Deep Learning Hardware: Past, Present, and Future — 8:45 AM

Yann LeCun, *Facebook AI Research & New York University, New York, NY*

Deep learning has caused revolutions in computer understanding of images, audio, and text, enabling new applications such as information search and filtering, autonomous driving, radiology screening, real-time language translation, and virtual assistants. But almost all these successes largely use supervised learning, which requires human-annotated data, or reinforcement learning, which requires too many trials to be practical in most real-world situations. In contrast, animals and humans seem to learn vast amounts of background knowledge about the world through mere observation and occasional actions in a self-supervised manner. Making progress in self-supervised learning is the main challenge of AI for the next decade. Success may result in machines with some level of common sense. But they will be built around deep learning architectures that are considerably larger than current ones, requiring vastly more powerful hardware than what we have today.

1.2 Intelligence on Silicon: From Deep Neural Network Accelerators to Brain-Mimicking AI-SoCs — 9:20 AM

Hoi-Jun Yoo, *KAIST, Daejeon, Korea*

Deep learning is influencing not only the technology itself but also our everyday lives. Formerly, most AI functionalities and applications were centralized on datacenters. However, the primary platform for AI has recently shifted to mobile devices. With the increasing demand on mobile AI, conventional hardware solutions face their ordeal because of their low energy efficiency on such power hungry applications. For the past few years, dedicated DNN accelerators inference have been under the spotlight. However, with the rising emphasis on privacy and personalization, ability to learn on mobile platform is becoming the second hurdle for "on-device AI." Going hand in hand, the brain mimicking is also a highlighted field in AI. Fundamentals of neuromorphic architecture start from the synapses and the neurons, which are realized with custom memories including non-volatile memories. The brain mimicking AI is not restricted to the naïve neuron implementation, but it extends further to mimic the behavioral characteristics such as "connectome" or "visual attention." In conclusion, mobile learning and brain mimicking will be the two horses driving the carriage called AI, thus opening up new requirements for the next generation deep learning SoCs.

ISSCC, SSCS, IEEE AWARD PRESENTATIONS **9:55 AM**

BREAK **10:20 AM**

1.3 Integration of Photonics and Electronics 10:40 AM

Meint K. Smit, *Eindhoven University of Technology, Eindhoven, The Netherlands*

The application market for Photonic Integrated Circuits (PICs) is rapidly growing. Photonic Integration is the dominant technology in high bandwidth communications and is set to become dominant in many fields of photonics, just like microelectronics in the field of electronics. Photonic integrated circuits offer compelling performance advances in terms of precision, bandwidth and energy efficiency. To enable uptake in new sectors, the availability of highly standardized (generic) photonic integration platform technologies is of key importance as this separates design from technology, reducing barriers for new entrants. The major platform technologies today are InP-based monolithic integration and Silicon Photonics. In this perspective paper we will describe the current status and future developments of InP-based generic integration platforms.

1.4 5G Wireless Communication: An Inflection Point 11:15 AM

Vida Ilderem, *Intel, Hillsboro, OR*

The 5G era is upon us, ushering in new opportunities for technology innovation across the computing and connectivity landscape. 5G presents an inflection point where wireless communication technology is driven by application and expected use cases, and where the network will set the stage for data-rich services and sophisticated cloud apps, delivered faster and with lower latency. This paper will highlight the disruptive architectures and technology innovations required to make 5G and beyond a reality.

PRESENTATION TO PLENARY SPEAKERS **11:50 AM**

CONCLUSION **11:55 AM**

Processors

Session Chair: ***Ingrid Verbauwhede,*** *KU Leuven, Leuven, Belgium*
Associate Chair: ***James Myers,*** *ARM, Cambridge, United Kingdom*

1:30 PM

2.1 Summit and Sierra: Designing AI/HPC Supercomputers
J. A. Kahle[1], J. Moreno[2], D. Dreps[3]
[1]IBM Research, Austin, TX; [2]IBM Research, Yorktown Heights, NY
[3]IBM Systems and Technology, Austin, TX

2:00 PM

2.2 A 978GOPS/W Flexible Streaming Processor for Real-Time Image Processing Applications in 22nm FDSOI
S. Smets[1], T. Goedemé[1], A. Mittal[2], M. Verhelst[1]
[1]KU Leuven, Heverlee, Belgium; [2]San Jose, CA

2:30 PM

2.3 An Energy-Efficient Configurable Lattice Cryptography Processor for the Quantum-Secure Internet of Things DS1
U. Banerjee[1], A. Pathak[2], A. P. Chandrakasan[1]
[1]Massachusetts Institute of Technology, Cambridge, MA
[2]Indian Institute of Technology Delhi, New Delhi, India

Break 3:00 PM

3:15 PM

2.4 A Distributed Autonomous and Collaborative Multi-Robot System Featuring a Low-Power Robot SoC in 22nm CMOS for Integrated Battery-Powered Minibots DS1
V. Honkote[1], D. Kurian[1], S. Muthukumar[1], D. Ghosh[1], S. Yada[1], K. Jain[1], B. Jackson[2], I. Klotchkov[2], M. R. Nimmagadda[1], S. Dattawadkar[1], P. Deshmukh[1], A. Gupta[1], J. Timbadiya[1], R. Pali[1], K. Narayanan[1], S. Soni[1], S. Chhabra[1], P. Dhama[1], N. Sreenivasulu[1], J. Kollikunnel[1], S. Kadavakollu[1], V. D. Sivaraj[1], P. Aseron[2], L. Azarenkov[2], N. Robinson[2], A. Radhakrishnan[3], M. Moiseev[2], G. Nandakumar[1], A. Madhukumar[4], R. Popov[2], K. P. Sahu[1], R. Peguvandla[1], A. Del Rio Ruiz[3], M. Bhartiya[1], A. Srinivasan[2], V. De[2]
[1]Intel, Bangalore, India; [2]Intel, Hillsboro, OR; [3]Intel, Guadalajara, Mexico
[4]Intel, Toronto, Canada

3:45 PM

2.5 A 40×40 Four-Neighbor Time-Based In-Memory Computing Graph ASIC Chip Featuring Wavefront Expansion and 2D Gradient Control
L. R. Everson, S. S. Sapatnekar, C. H. Kim
University of Minnesota, Minneapolis, MN

4:15 PM

2.6 A 2×30k-Spin Multichip Scalable Annealing Processor Based on a Processing-In-Memory Approach for Solving Large-Scale Combinatorial Optimization Problems DS1
T. Takemoto[1], M. Hayashi[2], C. Yoshimura[2], M. Yamaoka[2]
[1]Hitachi, Sapporo, Japan; [2]Hitachi, Tokyo, Japan

4:45 PM

2.7 A 28nm 600MHz Automotive Flash Microcontroller with Virtualization-Assisted Processor for Next-Generation Automotive Architecture Complying with ISO26262 ASIL-D
S. Otani, N. Otsuki, Y. Suzuki, N. Okumura, S. Maeda, T. Yanagita, T. Koike, Y. Shimazaki, M. Ito, M. Uemura, T. Hattori, T. Yamauchi, H. Kondo
Renesas Electronics, Kodaira, Japan

Conclusion 5:15 PM

Nyquist-Rate ADCs

Session Chair: ***Seng-Pan (Ben) U,*** *University of Macau, Macau, China*
Associate Chair: ***Ahmed Ali,*** *Analog Devices, Greensboro, NC*

1:30 PM

3.1 A 3.2GS/s 10 ENOB 61mW Ringamp ADC in 16nm with Background Monitoring of Distortion

B. Hershberg, D. Dermit, B. van Liempd, E. Martens, N. Markulic, J. Lagos, J. Craninckx
imec, Leuven, Belgium

2:00 PM

3.2 A 7.6mW 1GS/s 60dB SNDR Single-Channel SAR-Assisted Pipelined ADC with Temperature-Compensated Dynamic Gm-R-Based Amplifier

W. Jiang[1], Y. Zhu[1], M. Zhang[1], C-H. Chan[1], R. P. Martins[1,2]
[1]University of Macau, Macau, China
[2]Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

2:30 PM

3.3 A 5GS/s 158.6mW 12b Passive-Sampling 8×-Interleaved Hybrid ADC with 9.4 ENOB and 160.5dB FoM$_S$ in 28nm CMOS

A. Ramkaj[1], J. C. Pena Ramos[1], Y. Lyu[1], M. Strackx[2], M. J. Pelgrom[1], M. Steyaert[1], M. Verhelst[1], F. Tavernier[1]
[1]KU Leuven, Heverlee, Belgium; [2]Nokia Bell Labs, Antwerpen, Belgium

Break 3:00 PM

3:15 PM

3.4 A 0.01mm² 25µW 2MS/s 74dB-SNDR Continuous-Time Pipelined-SAR ADC with 120fF Input Capacitor

L. Shen[1], Y. Shen[1,2], X. Tang[1], C-K. Hsu[1], W. Shi[1], S. Li[1], W. Zhao[1], A. Mukherjee[1], N. Sun[1]
[1]University of Texas, Austin, TX; [2]Xidian University, Xi'an, China

3:45 PM

3.5 A 0.6V 13b 20MS/s Two-Step TDC-Assisted SAR ADC with PVT Tracking and Speed-Enhanced Techniques DS1

M. Zhang[1], C-H. Chan[1], Y. Zhu[1], R. P. Martins[1,2]
[1]University of Macau, Macau, China
[2]Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

4:15 PM

3.6 A 6-to-600MS/s Fully Dynamic Ringamp Pipelined ADC with Asynchronous Event-Driven Clocking in 16nm

B. Hershberg, B. van Liempd, N. Markulic, J. Lagos, E. Martens, D. Dermit, J. Craninckx
imec, Leuven, Belgium

4:45 PM

3.7 A 10mW 16b 15MS/s Two-Step SAR ADC with 95dB DR Using Dual-Deadzone Ring-Amplifier

A. ElShater[1], C. Y. Lee[1], P. K. Venkatachala[1], J. Muhlestein[1], S. Leuenberger[1], K. Sobue[2], K. Hamashita[2], U-K. Moon[1]
[1]Oregon State University, Corvallis, OR; [2]Asahi Kasei Microdevices, Atsugi, Japan

Conclusion 5:15 PM

Power Amplifiers

Session Chair: ***Krzysztof Dufrêne,*** *Intel, Linz, Austria*
Associate Chair: ***Harish Krishnaswamy,*** *Columbia University, New York, NY*

1:30 PM

4.1 A Watt-Level Phase-Interleaved Multi-Subharmonic Switching Digital Power Amplifier Achieving 31.4% Average Drain Efficiency
A. Zhang, M-W. Chen, University of Southern California, Los Angeles, CA

2:00 PM

4.2 A Broadband Switched-Transformer Digital Power Amplifier for Deep Back-Off Efficiency Enhancement
L. Xiong, T. Li, Y. Yin, H. Min, N. Yan, H. Xu, Fudan University, Shanghai, China

2:15 PM

4.3 A Multiphase Interpolating Digital Power Amplifier for TX Beamforming in 65nm CMOS
Z. Bai, W. Yuan, A. Azam, J. S. Walling, University of Utah, Salt Lake City, UT

2:30 PM

4.4 A Highly Linear High-Power 802.11ac/ax WLAN SiGe HBT Power Amplifier Using a Compact 2nd-Harmonic-Shorting Four-Way Transformer and Integrated Thermal Sensors
I. Ju[1], M. McPartlin[2], C-W. P. Huang[2], C. D. Cheon[1], M. Doherty[2], J. D. Cressler[1]
[1]Georgia Institute of Technology, Atlanta, GA; [2]Skyworks Solutions, Andover, MA

2:45 PM

4.5 A 13.5dBm Fully Integrated 200-to-255GHz Power Amplifier with a 4-Way Power Combiner in SiGe:C BiCMOS
M. H. Eissa[1], D. Kissinger[1,2]
[1]IHP, Frankfurt (Oder), Germany; [2]Technische Universität Berlin, Berlin, Germany

Break 3:00 PM

3:15 PM

4.6 A mm-Wave 3-Way Linear Doherty Radiator with Multi-Antenna Coupling and On-Antenna Current-Scaling Series Combiner for Deep Power Back-Off Efficiency Enhancement
H. T. Nguyen, S. Li, H. Wang, Georgia Institute of Technology, Atlanta, GA

3:45 PM

4.7 DS1 A Compact DC-to-108GHz Stacked-SOI Distributed PA/Driver Using Multi-Drive Inter-Stack Coupling, Achieving 1.525THz GBW, 20.8dBm Peak P_{1dB}, and Over 100Gb/s in 64-QAM and PAM-4 Modulation
O. El-Aassar, G. M. Rebeiz, University of California, San Diego, La Jolla, CA

4:15 PM

4.8 DS1 A Highly Linear Super-Resolution Mixed-Signal Doherty Power Amplifier for High-Efficiency mm-Wave 5G Multi-Gb/s Communications
F. Wang, T-W. Li, H. Wang, Georgia Institute of Technology, Atlanta, GA

4:45 PM

4.9 A 60GHz CMOS Power Amplifier with Cascaded Asymmetric Distributed-Active-Transformer Achieving Watt-Level Peak Output Power with 20.8% PAE and Supporting 2Gsym/s 64-QAM Modulation
H. T. Nguyen, D. Jung, H. Wang, Georgia Institute of Technology, Atlanta, GA

Conclusion 5:15 PM

Image Sensors

Session Chair: ***Kazuko Nishimura,*** *Panasonic Corporation, Moriguchi, Japan*
Associate Chair: ***Jun Deguchi,*** *Toshiba Memory Corporation, Kawasaki, Japan*

1:30 PM

5.1 A Stacked Global-Shutter CMOS Imager with SC-Type Hybrid-GS Pixel and Self-Knee Point Calibration Single-Frame HDR and On-Chip Binarization Algorithm for Smart Vision Applications DS1

C. Xu[1], Y. Mo[1], G. Ren[2], W. Ma[2], X. Wang[1], W. Shi[2], J. Hou[2], K. Shao[2], H. Wang[2], P. Xiao[2], Z. Shao[2], X. Xie[1], X. Wang[1], C. Yiu[1]
[1]SmartSens Technology, San Jose, CA; [2]SmartSens Technology, Shanghai, China

2:00 PM

5.2 Energy-Efficient Low-Noise CMOS Image Sensor with Capacitor Array-Assisted Charge-Injection SAR ADC for Motion-Triggered Low-Power IoT Applications DS1

K. D. Choo, L. Xu, Y. Kim, J-H. Seol, X. Wu, D. Sylvester, D. Blaauw
University of Michigan, Ann Arbor, MI

2:30 PM

5.3 A Data-Compressive 1.5b/2.75b Log-Gradient QVGA Image Sensor with Multi-Scale Readout for Always-On Object Detection DS1

C. Young[1], A. Omid-Zohoor[1,2], P. Lajevardi[3], B. Murmann[1]
[1]Stanford University, Stanford, CA; [2*]now with K-Motion Interactive, San Francisco, CA
[3]Robert Bosch, Sunnyvale, CA

Break 3:00 PM

3:15 PM

5.4 A 76mW 500fps VGA CMOS Image Sensor with Time-Stretched Single-Slope ADCs Achieving 1.95e- Random Noise

I. Park[1], C. Park[1], J. Cheon[2], Y. Chae[1], [1]Yonsei University, Seoul, Korea
[2]Kumoh National Institute of Technology, Gyeongbuk, Korea

3:30 PM

5.5 Dual-Tap Pipelined-Code-Memory Coded-Exposure-Pixel CMOS Image Sensor for Multi-Exposure Single-Frame Computational Imaging DS1

N. Sarhangnejad[1], N. Katic[2], Z. Xia[1], M. Wei[1], N. Gusev[1], G. Dutta[1], R. Gulve[1], H. Haim[1], M. Moreno Garcia[3], D. Stoppa[4], K. N. Kutulakos[1], R. Genov[1]
[1]University of Toronto, Toronto, Canada; [2]Synopsys, Toronto, Canada
[3]Fondazione Bruno Kessler, Trento, Italy; [4]ams AG, Ruschlikon, Switzerland

3:45 PM

5.6 A 400×400-Pixel 6μm-Pitch Vertical Avalanche Photodiodes CMOS Image Sensor Based on 150ps-Fast Capacitive Relaxation Quenching in Geiger Mode for Synthesis of Arbitrary Gain Images DS1

Y. Hirose, S. Koyama, T. Okino, A. Inoue, S. Saito, Y. Nose, M. Ishii, S. Yamahira, S. Kasuga, M. Mori, T. Kabe, K. Nakanishi, M. Usuda, A. Odagawa, T. Tanaka
Panasonic, Nagaokakyo, Japan

4:15 PM

5.7 A 256×256 40nm/90nm CMOS 3D-Stacked 120dB-Dynamic-Range Reconfigurable Time-Resolved SPAD Imager DS1

R. K. Henderson[1], N. Johnston[1], S. W. Hutchings[1], I. Gyongy[1], T. Al Abbas[1], N. Dutton[2], M. Tyler[3], S. Chan[3], J. Leach[3]
[1]University of Edinburgh, Edinburgh, United Kingdom
[2]STMicroelectronics, Edinburgh, United Kingdom
[3]Heriot-Watt University, Edinburgh, United Kingdom

4:45 PM

5.8 A 32×32-Pixel 0.9THz Imager with Pixel-Parallel 12b VCO-Based ADC in 0.18μm CMOS

S. Yokoyama[1], M. Ikebe[1], Y. Kanazawa[1], T. Ikegami[1], P. Ambalathankandy[1], S. Hiramatsu[1], E. Sano[1], Y. Takida[2], H. Minamide[2]
[1]Hokkaido University, Sapporo, Japan; [2]RIKEN, Sendai, Japan

Conclusion 5:15 PM

Ultra-High-Speed Wireline

Session Chair: ***Tony Chan Carusone,*** *University of Toronto, Toronto, Canada*
Associate Chair: ***Takayuki Shibasaki,*** *Fujitsu Laboratories, Kawasaki, Japan*

1:30 PM

6.1 A 100Gb/s 1.1pJ/b PAM-4 RX with Dual-Mode 1-Tap PAM-4 / 3-Tap NRZ Speculative DFE in 14nm CMOS FinFET

A. Cevrero, I. Ozkaya, P. A. Francese, M. Brandli, C. Menolfi, T. Morf, M. Kossel, L. Kull, D. Luu, M. Dazzi, T. Toifl, IBM Research, Ruschlikon, Switzerland

2:00 PM

6.2 A 60Gb/s PAM-4 ADC-DSP Transceiver in 7nm CMOS with SNR-Based Adaptive Power Scaling Achieving 6.9pJ/b at 32dB Loss

M-A. LaCroix, H. Wong, Y. H. Liu, H. Ho, S. Lebedev, P. Krotnev, D. A. Nicolescu, D. Petrov, C. Carvalho, S. Alie, E. Chong, F. A. Musa, D. Tonietto
Huawei Technologies, Ottawa, Canada

2:30 PM

6.3 A Sub-250mW 1-to-56Gb/s Continuous-Range PAM-4 42.5dB IL ADC/DAC-Based Transceiver in 7nm FinFET DS1

M. Pisati, F. De Bernardinis, P. Pascale, C. Nani, M. Sosio, E. Pozzati, N. Ghittori, F. Magni, M. Garampazzi, G. Bollati, A. Milani, A. Minuti, F. Giunco, P. Uggetti, I. Fabiano, N. Codega, A. Bosi, N. Carta, D. Pellicone, G. Spelgatti, M. Cutrupi, A. Rossini, R. Massolini, G. Cesura, I. Bietti, eSilicon Italy, Pavia, Italy

Break 3:00 PM

3:15 PM

6.4 A 180mW 56Gb/s DSP-Based Transceiver for High-Density IOs in Data Center Switches in 7nm FinFET Technology DS1

T. Ali[1], R. Yousry[1], H. Park*[1], E. Chen*[1], P-S. Weng[2], Y-C. Huang[2], C-C. Liu[2], C-H. Wu[2], S-H. Huang[2], C. Lin[2], K-C. Wu[2], K-H. Tsai[2], K-W. Tan[2], A. ElShater[1], K-R. Chen[2], W-H. Tsai[2], H-S. Chen[2], W. Leng[1], M. Soliman[1]*
[1]MediaTek, Irvine, CA; [2]MediaTek, Hsinchu, Taiwan; *Equally-Credited Authors (ECAs)

3:45 PM

6.5 A 400Gb/s Transceiver for PAM-4 Optical Direct-Detect Application in 16nm FinFET

C. Loi[1], A. Mellati[2], A. Tan[3], A. Farhoodfar[3], A. Tiruvur[3], B. Helal[3], B. Killips[4], F. Rad[3], J. Riani[3], J. Pernillo[3], J. Sun[1], J. Wong[3], K. Abdelhalim[2], K. Gopalakrishnan[3], K. Kim[2], L. Tse[3], M. Davoodi[2], M. Le[2], M. Zhang[3], M. Talegaonkar[2], P. Prabha[2], R. Mohanavelu[3], S. Chong[1], S. Forey[4], S. Netto[3], S. Bhoja[3], W. Liew[1], Y. Duan[3], Y. Liao[3]
[1]Inphi Corporation, Singapore; [2]Inphi Corporation, Irvine, CA
[3]Inphi Corporation, Santa Clara, CA; [4]Inphi Corporation, Northants, United Kingdom

4:15 PM

6.6 A 128Gb/s 1.3pJ/b PAM-4 Transmitter with Reconfigurable 3-Tap FFE in 14nm CMOS

Z. Toprak-Deniz, J. E. Proesel, J. F. Bulzacchelli, H. A. Ainspan, T. O. Dickson, M. P. Beakes, M. Meghelli, IBM T. J. Watson Research Center, Yorktown Heights, NY

4:45 PM

6.7 A 112Gb/s PAM-4 Voltage-Mode Transmitter with 4-Tap Two-Step FFE and Automatic Phase Alignment Techniques in 40nm CMOS DS1

P-J. Peng[1], Y-T. Chen[1], S-T. Lai[1], C-H. Chen[1], H-E. Huang[1], T. Shih[2]
[1]Yuan Ze University, Taoyuan City, Taiwan; [2]Teletrx, Taipei, Taiwan

5:00 PM

6.8 A 36Gb/s Adaptive Baud-Rate CDR with CTLE and 1-Tap DFE in 28nm CMOS

D. Yoo[1], M. Bagherbeik[1], W. Rahman[1], A. Sheikholeslami[1], H. Tamura[2], T. Shibasaki[2]
[1]University of Toronto, Toronto, Canada; [2]Fujitsu Laboratories, Kawasaki, Japan

Conclusion 5:15 PM

Demonstration Session 1, Monday February 18th, 5:00-7:00 PM

This year, the Demonstration Session extending in selected regular papers, both Academic and Industrial, will take place on Monday February 18th, and Tuesday February 19th, from 5 pm until 7 pm in the Golden Gate Hall. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2019, as noted by the symbol **DS1**

2.3 An Energy-Efficient Configurable Lattice Cryptography Processor for the Quantum-Secure Internet of Things

2.4 A Distributed Autonomous and Collaborative Multi-Robot System Featuring a Low-Power Robot SoC in 22nm CMOS for Integrated Battery-Powered Minibots

2.6 A 2×30k-Spin Multichip Scalable Annealing Processor Based on a Processing-In-Memory Approach for Solving Large-Scale Combinatorial Optimization Problems

3.5 A 0.6V 13b 20MS/s Two-Step TDC-Assisted SAR ADC with PVT Tracking and Speed-Enhanced Techniques

4.7 A Compact DC-to-108GHz Stacked-SOI Distributed PA/Driver Using Multi-Drive Inter-Stack Coupling, Achieving 1.525THz GBW, 20.8dBm Peak P_{1dB}, and Over 100Gb/s in 64-QAM and PAM-4 Modulation

4.8 A Highly Linear Super-Resolution Mixed-Signal Doherty Power Amplifier for High-Efficiency mm-Wave 5G Multi-Gb/s Communications

5.1 A Stacked Global-Shutter CMOS Imager with SC-Type Hybrid-GS Pixel and Self-Knee Point Calibration Single-Frame HDR and On-Chip Binarization Algorithm for Smart Vision Applications

5.2 Energy-Efficient Low-Noise CMOS Image Sensor with Capacitor Array-Assisted Charge-Injection SAR ADC for Motion-Triggered Low-Power IoT Applications

5.3 A Data-Compressive 1.5b/2.75b Log-Gradient QVGA Image Sensor with Multi-Scale Readout for Always-On Object Detection

5.5 Dual-Tap Pipelined-Code-Memory Coded-Exposure-Pixel CMOS Image Sensor for Multi-Exposure Single-Frame Computational Imaging

5.6 A 400×400-Pixel 6μm-Pitch Vertical Avalanche Photodiodes CMOS Image Sensor Based on 150ps-Fast Capacitive Relaxation Quenching in Geiger Mode for Synthesis of Arbitrary Gain Images

5.7 A 256×256 40nm/90nm CMOS 3D-Stacked 120dB-Dynamic-Range Reconfigurable Time-Resolved SPAD Imager

6.3 A Sub-250mW 1-to-56Gb/s Continuous-Range PAM-4 42.5dB IL ADC/DAC-Based Transceiver in 7nm FinFET

6.4 A 180mW 56Gb/s DSP-Based Transceiver for High-Density IOs in Data Center Switches in 7nm FinFET Technology

6.7 A 112Gb/s PAM-4 Voltage-Mode Transmitter with 4-Tap Two-Step FFE and Automatic Phase Alignment Techniques in 40nm CMOS

7.2 A 20.5TOPS and 217.3GOPS/mm^2 Multicore SoC with DNN Accelerator and Image Signal Processor Complying with ISO26262 for Automotive Applications

7.3 An 879GOPS 243mW 80fps VGA Fully Visual CNN-SLAM Processor for Wide-Range Autonomous Exploration

7.4 A 2.1TFLOPS/W Mobile Deep RL Accelerator with Transposable PE Array and Experience Compression

7.6 A 65nm 236.5nJ/Classification Neuromorphic Processor with 7.5% Energy Overhead On-Chip Learning Using Direct Spike-Only Feedback

7.7 LNPU: A 25.3TFLOPS/W Sparse Deep-Neural-Network Learning Processor with Fine-Grained Mixed Precision of FP8-FP16

8.1 A 93.8% Peak Efficiency, 5V-Input, 10A Max I_{LOAD} Flying Capacitor Multilevel Converter in 22nm CMOS Featuring Wide Output Voltage Range and Flying Capacitor Precharging

8.3 A 10.9W 93.4%-Efficient (27W 97%-Efficient) Flying-Inductor Hybrid DC-DC Converter Suitable for 1-Cell (2-Cell) Battery Charging Applications

8.5 A Fully Integrated Voltage Regulator in 14nm CMOS with Package-Embedded Air-Core Inductor Featuring Self-Trimmed, Digitally Controlled Variable On-Time Discontinuous Conduction Mode Operation

EE3: Making a Career Choice 7:00 PM

This evening interactive event will include several distinguished panelists representing a broad variety of career choices in the areas of start-ups, industry, research, and academia available to graduates in electrical and computer engineering. Following short introductory remarks by each panelist, this forum will open for audience interaction in which the audience is invited to express a broad range of questions to the panelists.

EE4: Industry Showcase 8:00 PM

Chair: ***Eugenio Cantatore,*** *Eindhoven University of Technology, Eindhoven, The Netherlands*

Organizers: ***Alison Burdett,*** *Sensium Healthcare, Abingdon, United Kingdom*
Kush Gulati, *Omni Design Technologies, Milpitas, CA*
Un-Ku Moon, *Oregon State University Corvallis, OR*

Committee: ***Ahmed Ali,*** *Analog Devices, Greensboro, NC*
Min Chen, *Analog Devices, Milpitas, CA*
Muhammad Khellah, *Intel, Hillsboro, OR*
Yan Li, *Western Digital, Milpitas, CA*
Yao-Hong Liu, *imec, Eindhoven, The Netherlands*
Michael Perrott, *TDK-Invensense, Boston, MA*
Bruce Rae, *ST Microelectronics, Edinburgh, United Kingdom*
Jiayoon Ru, *Broadcom, Irvine, CA*
Takayuki Shibasaki, *Fujitsu Laboratories, Kawasaki, Japan*
Youngmin Shin, *Samsung, Hwansung, Korea*

The event will begin with a Showcase Keynote "Accelerated Platforms: The Future of Computing" by Bill Dally, Chief Scientist and Senior Vice President of Research, NVIDIA, Santa Clara, CA and Professor (Research) of EE and CS, Stanford University, Stanford, CA.

Following the keynote, the Industry Showcase will feature short presentations as well as interactive demonstrations from each of the Industry Showcase participants, and represent an exciting introduction to the next generation of applications and products enabled by advances in solid-state integrated circuits.

The list below highlights the list of participants in the Industry Showcase.

Altia Systems, Cupertino, CA
180° Real-time Immersive, Intelligent Vision Systems

ams AG, Premstätten, Austria
Direct Time-of-Flight Module in CMOS 55nm HV for Mobile Applications

Ayar Labs, Emeryville, CA
TeraPHY: A high-density electronic-photonic chiplet for co-packaged optical I/O

Healthrian, Daejeon, Korea
Impedance-based Sensor Chip for Non-invasive Blood Pressure Monitoring

IBM T. J. Watson Research Center, Yorktown Heights, NY
Fast channel sounding and beam optimization for 5G using software defined phased array radios

Mediatek, HsinChu, Taiwan
Future Driving with Better Safety Inside-Out

NUFRONT, Beijing, China
The world's first deployed URLLC wireless communication system and SoCs

NVIDIA, Santa Clara, CA
Deep Learning Inference on NVIDIA GPUs and Accelerators

Ouster, San Francisco, CA
Native camera imaging on LiDAR and deep learning enablement

PsiKick, Santa Clara, CA
PsiKick's Batteryless Sensor Network Platform for the Industrial IoT

Samsung Electronics, Hwaseong, Korea
A Fully Integrated 10nm Multi-Mode 5G Modem Chipset Compatible with 3GPP NR Standards

Samsung Electronics, Hwaseong, Korea
Motion Artifact Free Dynamic Vision Sensor for Machine Vision

SiFive, San Mateo, CA
Unleashed Acceleration: AI on RISC-V

Machine Learning

Session Chair: ***Dejan Markovic,*** *University of California, Los Angeles, Los Angeles, CA*

Associate Chair: ***Mahesh Mehendale,*** *Texas Instruments, Dallas, TX*

8:30 AM

7.1 An 11.5TOPS/W 1024-MAC Butterfly Structure Dual-Core Sparsity-Aware Neural Processing Unit in 8nm Flagship Mobile SoC

J. Song[1], Y. Cho[1], J-S. Park[1], J-W. Jang[2], S. Lee[2], J-H. Song[2], J-G. Lee[1], I. Kang[1]
[1]Samsung Electronics, Hwaseong, Korea
[2]Samsung Advanced Institute of Technology, Suwon, Korea

9:00 AM

7.2 A 20.5TOPS and 217.3GOPS/mm² Multicore SoC with DNN Accelerator and Image Signal Processor Complying with ISO26262 for Automotive Applications DS1

Y. Yamada, T. Sano, Y. Tanabe, Y. Ishigaki, S. Hosoda, F. Hyuga, A. Moriya, R. Hada, A. Masuda, M. Uchiyama, T. Koizumi, T. Tamai, N. Sato, J. Tanabe, K. Kimura, R. Murakami, T. Yoshikawa
Toshiba Electronic Devices & Storage, Kawasaki, Japan

9:30 AM

7.3 An 879GOPS 243mW 80fps VGA Fully Visual CNN-SLAM Processor for Wide-Range Autonomous Exploration DS1

Z. Li, Y. Chen, L. Gong, L. Liu, D. Sylvester, D. Blaauw, H-S. Kim
University of Michigan, Ann Arbor, MI

Break 10:00 AM

10:15 AM

7.4 A 2.1TFLOPS/W Mobile Deep RL Accelerator with Transposable PE Array and Experience Compression DS1

C. Kim, S. Kang, D. Shin, S. Choi, Y. Kim, H-J. Yoo
KAIST, Daejeon, Korea

10:45 AM

7.5 A 65nm 0.39-to-140.3TOPS/W 1-to-12b Unified Neural-Network Processor Using Block-Circulant-Enabled Transpose-Domain Acceleration with 8.1× Higher TOPS/mm² and 6T HBST-TRAM-Based 2D Data-Reuse Architecture

J. Yue[1], R. Liu[1], W. Sun[1], Z. Yuan[1], Z. Wang[1], Y-N. Tu[2], Y-J. Chen[2], A. Ren[3], Y. Wang[3], M-F. Chang[2], X. Li[1], H. Yang[1], Y. Liu[1]
[1]Tsinghua University, Beijing, China
[2]National Tsing Hua University, Hsinchu, Taiwan
[3]Northeastern University, Boston, MA

11:15 AM

7.6 A 65nm 236.5nJ/Classification Neuromorphic Processor with 7.5% Energy Overhead On-Chip Learning Using Direct Spike-Only Feedback DS1

J. Park, J. Lee, D. Jeon
Seoul National University, Seoul, Korea

11:45 AM

7.7 LNPU: A 25.3TFLOPS/W Sparse Deep-Neural-Network Learning Processor with Fine-Grained Mixed Precision of FP8-FP16 DS1

J. Lee, J. Lee, D. Han, J. Lee, G. Park, H-J. Yoo
KAIST, Daejeon, Korea

Conclusion 12:15 PM

DC-DC Converters

Session Chair: ***Gerard Villar Pique,*** *NXP Semiconductor, Eindhoven, The Netherlands*

Associate Chair: ***Jason Stauth,*** *Dartmouth Colege, Hanover, NH*

8:30 AM

8.1 A 93.8% Peak Efficiency, 5V-Input, 10A Max I_{LOAD} Flying Capacitor Multilevel Converter in 22nm CMOS Featuring Wide Output Voltage Range and Flying Capacitor Precharging DS1

C. Schaef[1], S. Weng[1], B. Choi[2], W. Lambert[2], K. Radhakrishnan[2], K. Ravichandran[1], J. Tschanz[1], V. De[1]
[1]Intel, Hillsboro, OR
[2]Intel, Chandler, AZ

9:00 AM

8.2 A Continuous-Input-Current Passive-Stacked Third-Order Buck Converter Achieving 0.7W/mm² Power Density and 94% Peak Efficiency

A. Abdulslam, P. P. Mercier, University of California, San Diego, La Jolla, CA

9:30 AM

8.3 A 10.9W 93.4%-Efficient (27W 97%-Efficient) Flying-Inductor Hybrid DC-DC Converter Suitable for 1-Cell (2-Cell) Battery Charging Applications DS1

C. Hardy, H-P. Le
University of Colorado, Boulder, CO

Break 10:00 AM

10:15 AM

8.4 Fully Integrated Buck Converter with 78% Efficiency at 365mW Output Power Enabled by Switched-Inductor-Capacitor Topology and Inductor Current Reduction Technique

N. Tang[1], B. Nguyen[1], Y. Tang[2], W. Hong[1], Z. Zhou[1], D. Heo[1]
[1]Washington State University, Pullman, WA
[2]HiSilicon, Shenzhen, China

10:45 AM

8.5 A Fully Integrated Voltage Regulator in 14nm CMOS with Package-Embedded Air-Core Inductor Featuring Self-Trimmed, Digitally Controlled Variable On-Time Discontinuous Conduction Mode Operation DS1

C. Schaef[1], N. Desai[1], H. Krishnamurthy[1], S. Weng[1], H. Do[2], W. Lambert[2], K. Radhakrishnan[2], K. Ravichandran[1], J. Tschanz[1], V. De[1]
[1]Intel, Hillsboro, OR; [2]Intel, Chandler, AZ

11:15 AM

8.6 A Fully Integrated 85%-Peak-Efficiency Hybrid Multi-Ratio Resonant DC-DC Converter with 3.0-to-4.5V Input and 500µA-to-120mA Load Range

P. Renz[1], M. Kaufmann[1], M. Lueders[2], B. Wicht[1]
[1]Leibniz University Hannover, Hannover, Germany
[2]Texas Instruments, Freising, Germany

11:45 AM

8.7 A 2MHz 4-to-60V_{IN} Buck-Boost Converter for Automotive Use Achieving 95% Efficiency and CISPR 25 Class 5 Standard

J. Xue, M. K. Song, X. Ke, M. Chen, L. Shtargot
Analog Devices, Milpitas, CA

Conclusion 12:15 PM

High-Frequency Transceivers for Radar and Communications

Session Chair: ***Nagendra Krishnapura,*** *Indian Institute of Technology Madras, Chennai, India*

Associate Chair: ***Yuu Watanabe,*** *Waseda University, Atsugi, Japan*

8:30 AM

9.1 Toward Automotive Surround-View Radars

C-M. Hung[1], A. T. Lin[1], B. Peng[1], H. Wang[2], J-L. Hsu[1], Y-J. Lu[1], W. Hsu[1], J-H. C. Zhan[1], B. Juan[1], C-H. Lok[1], S. Lee[1], P. Hsiao[1], Q. Zhou[2], M. Wei[1], H-Y. Chu[1], Y-L. Chen[1], C-C. Hung[1], K. Fong[1], P-C. Huang[1], P. Chen[1], S-Y. Su[1], Y-J. Chen[1], K. Chen[1], C-C. Tung[1], Y-J. Hsieh[1], T-C. Tsai[1], Y-F. Chen[1], W-K. Hsin[1], L. Guo[3], H. Liu[3], D. Jin[3]

[1]MediaTek, Hsinchu, Taiwan; [2]MediaTek, San Jose, CA; [3]MediaTek, Hefei, China

9:00 AM

9.2 A 192-Virtual-Receiver 77/79GHz GMSK Code-Domain MIMO Radar System-on-Chip

V. Giannini, M. Goldenberg, A. Eshraghi, J. Maligeorgos, L. Lim, R. Lobo, D. Welland, C-K. Chow, A. Dornbusch, T. Dupuis, S. Vaz, F. Rush, P. Bassett, H. Kim, M. Maher, O. Schmid, C. Davis, M. Hegde, Uhnder, Austin, TX

9:30 AM

9.3 A 680μW Burst-Chirp UWB Radar Transceiver for Vital Signs and Occupancy Sensing up to 15m Distance DS2

Y-H. Liu[1], S. Sheelavant[1,2], M. Mercuri[1], P. Mateman[1], J. Dijkhuis[1], W. Zomagboguelou[1,3], A. Breeschoten[1], S. Traferro[1], Y. Zhan[1], T. Torf[4], C. Bachmann[1], M. Babaie[2]

[1]imec - Netherlands, Eindhoven, The Netherlands

[2]Delft University of Technology, Delft, The Netherlands

[3]TU Eindhoven, Eindhoven, The Netherlands; [4]imec, Leuven, Belgium

Break 10:00 AM

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9.4 A 145GHz FMCW-Radar Transceiver in 28nm CMOS DS2

A. Visweswaran, K. Vaesen, S. Sinha, I. Ocket, M. Glassee, C. Desset, A. Bourdoux, P. Wambacq, imec, Leuven, Belgium

10:30 AM

9.5 An 80Gb/s 300GHz-Band Single-Chip CMOS Transceiver DS2

S. Lee[1], R. Dong[1], T. Yoshida[1], S. Amakawa[1], S. Hara[2], A. Kasamatsu[2], J. Sato[3], M. Fujishima[1], [1]Hiroshima University, Higashihiroshima, Japan

[2]National Institute of Information and Communications Technology, Koganei, Japan

[3]Panasonic, Yokohama, Japan

10:45 AM

9.6 A 42.2Gb/s 4.3pJ/b 60GHz Digital Transmitter with 12b/Symbol Polarization MIMO

C. Thakkar, S. Shopov, A. Chakrabarti, S. Yamada, D. Choudhury, J. Jaussi, B. Casper Intel, Hillsboro, OR

11:15 AM

9.7 A Scalable 71-to-76GHz 64-Element Phased-Array Transceiver Module with 2×2 Direct-Conversion IC in 22nm FinFET CMOS Technology DS2

S. Pellerano[1], S. Callender[1], W. Shin[1], Y. Wang[2], S. Kundu[1], A. Agrawal[1], P. Sagazio[1], B. Carlton[1], F. Sheikh[1], A. Amadjikpe[1], W. Lambert[3], D. S. Vemparala[1], M. Chakravorti[1], S. Suzuki[1], R. Flory[1], C. Hull[1], [1]Intel, Hillsboro, OR; [2]Hillsboro, OR; [3]Intel, Chandler, AZ

11:45 AM

9.8 A 28GHz 20.3%-Transmitter-Efficiency 1.5°-Phase-Error Beamforming Front-End IC with Embedded Switches and Dual-Vector Variable-Gain Phase Shifters

*J. Park *[1], S. Lee *[1], D. Lee[2], S. Hong[1]*, [1]KAIST, Daejeon, Korea

[2]Hanbat National University, Daejeon, Korea; *Equally-Credited Authors (ECAs)

Conclusion 12:15 PM

Sensor Interfaces

Session Chair: ***Tim Piessens,*** *ICsense, Leuven, Belgium*
Associate Chair: ***Wen-Chieh Wang,*** *MediaTek, Hsinchu City, Taiwan*

8:30 AM

10.1 An Energy Measurement Front-End with Integrated In-Situ Background Full System Accuracy Monitoring Including the Current and Voltage Sensors DS2

S. Danesh[1], W. Holland[1], J. Spalding[1], M. Guidry[2], J. Hurwitz[1]
[1]Analog Devices, Edinburgh, United Kingdom
[2]Analog Devices, Wilmington, MA

9:00 AM

10.2 A 22ng/√Hz 17mW MEMS Accelerometer with Digital Noise-Reduction Techniques DS2

Y. Furubayashi, T. Oshima, T. Yamawaki, K. Watanabe, K. Mori, N. Mori, A. Matsumoto, H. Kazama, Y. Kamada, A. Isobe, T. Sekiguchi
Hitachi, Tokyo, Japan

9:30 AM

10.3 A 0.12mm² Wien-Bridge Temperature Sensor with 0.1°C (3σ) Inaccuracy from -40°C to 180°C

S. Pan, Ç. Gürleyük, M. F. Pimenta, K. A. A. Makinwa
Delft University of Technology, Delft, The Netherlands

9:45 AM

10.4 A Wheatstone-Bridge Temperature Sensor with a Resolution FoM of 20fJ·K²

S. Pan, K. A. A. Makinwa
Delft University of Technology, Delft, The Netherlands

Break 10:00 AM

Diagnostics

Session Chair: ***Joonsung Bae,*** *Kangwon National University, Chuncheon, Korea*
Associate Chair: ***Michael Kraft,*** *KULeuven, Leuven, Belgium*

10:15 AM

11.1 A 5.37mW/Channel Pitch-Matched Ultrasound ASIC with Dynamic-Bit-Shared SAR ADC and 13.2V Charge-Recycling TX in Standard CMOS for Intracardiac Echocardiography

J. Lee[1], K-R. Lee[1], B. E. Eovino[2], J. H. Park[3], L. Lin[2], H-J. Yoo[1], J. Yoo[3,4]
[1]KAIST, Daejeon, Korea
[2]University of California, Berkeley, CA
[3]National University of Singapore, Singapore
[4]Singapore Institute for Neurotechnology, Singapore

10:45 AM

11.2 A CMOS Biosensor Array with 1024 3-Electrode Voltammetry Pixels and 93dB Dynamic Range

A. Manickam[1], K-D. You[2], N. Wood[1], L. Pei[1], Y. Liu[1], R. Singh[1], N. Gamini[1], D. Shahrjerdi[2], R. G. Kuimelis[1], A. Hassibi[1]
[1]InSilixa, Sunnyvale, CA
[2]New York University, New York, NY

11:15 AM

11.3 A Capacitive Biosensor for Cancer Diagnosis Using a Functionalized Microneedle and a 13.7b-Resolution Capacitance-to-Digital Converter from 1 to 100nF

S. Song, J. Na, M. Jang, H. Lee, H. Lee, Y. Lim, H. Choi, Y. Chae
Yonsei University, Seoul, Korea

11:45 AM

11.4 A Fast-Readout Mismatch-Insensitive Magnetoresistive Biosensor Front-End Achieving Sub-ppm Sensitivity

X. Zhou, M. Sveiven, D. A. Hall
University of California, San Diego, La Jolla, CA

12:00 PM

11.5 A 512-Pixel 3kHz-Frame-Rate Dual-Shank Lensless Filterless Single-Photon-Avalanche-Diode CMOS Neural Imaging Probe DS2

C. Lee[1,2], A. J. Taal[1], J. Choi[1], K. Kim[1], K. Tien[1], L. Moreaux[3], M. L. Roukes[3], K. L. Shepard[1]
[1]Columbia University, New York, NY
[2]KIST, Seoul, Korea
[3]California Institute of Technology, Pasadena

Conclusion 12:15 PM

Emerging Technologies

Session Chair: ***Wim Dehaene,*** *Kuleuven-MICAS, Leuven, Belgium*
Associate Chair: ***Sriram Vangal,*** *Intel, Hillsboro, OR*

8:30 AM

12.1 An FPGA-Accelerated Fully Nonvolatile Microcontroller Unit for Sensor-Node Applications in 40nm CMOS/MTJ-Hybrid Technology Achieving 47.14µW Operation at 200MHz

M. Natsui[1], D. Suzuki[1], A. Tamakoshi[1], T. Watanabe[1,2], H. Honjo[1,2], H. Koike[1,2], T. Nasuno[1,2], Y. Ma[1], T. Tanigawa[1,2], Y. Noguchi[1,2], M. Yasuhira[1,2], H. Sato[1], S. Ikeda[1,2], H. Ohno[1], T. Endoh[1,2], T. Hanyu[1]
[1]Tohoku University, Miyagi, Japan
[2]JST/ACCEL, Tokyo, Japan

9:00 AM

12.2 Micro Short-Circuit Detector Including S/H Circuit for 1hr Retention and 52dB Comparator Composed of C-Axis Aligned Crystalline IGZO FETs for Li-Ion Battery Protection IC DS2

H. Inoue[1], T. Aoki[1], F. Akasawa[1], T. Hamada[1], T. Takeuchi[1], K. Nei[1], T. Seki[1], Y. Yakubo[1], K. Takahashi[1], S. Fukai[1], T. Ishizu[1], M. Kozuma[1], R. Tajima[1], T. Matsuzaki[1], T. Ikeda[1], M. Ikeda[2], S. Yamazaki[1]
[1]Semiconductor Energy Laboratory, Kanagawa, Japan
[2]University of Tokyo, Tokyo, Japan

9:30 AM

12.3 Memory Solutions for Flexible Thin-Film Logic: up to 8kb, >105.9kb/s LPROM and SRAM with Integrated Timing Generation Meeting the ISO NFC Standard

F. De Roose[1,2], J. Genoe[1,2], A. J. Kronemeijer[3], K. Myny[2], W. Dehaene[1,2]
[1]KU Leuven, Heverlee, Belgium
[2]imec, Heverlee, Belgium
[3]Holst Centre/TNO, Eindhoven, The Netherlands

Break 10:00 AM

Non-Volatile Memories

Session Chair: ***Yan Li,*** *Western Digital, Milpitas, CA*

Associate Chair: ***Jongmin Park,*** *SK Hynix, Icheon-si, Gyeonggi-do, Korea*

10:15 AM

13.1 A 1.33Tb 4-bit/Cell 3D-Flash Memory on a 96-Word-Line-Layer Technology

N. Shibata[1], K. Kanda[1], T. Shimizu[1], J. Nakai[1], O. Nagao[1], N. Kobayashi[1], M. Miakashi[1], Y. Nagadomi[1], T. Nakano[1], T. Kawabe[1], T. Shibuya[1], M. Sako[1], K. Yanagidaira[1], T. Hashimoto[1], H. Date [1], M. Sato[1], T. Nakagawa[1], H. Takamoto[1], J. Musha[1], T. Minamoto[1], M. Uda[1], D. Nakamura[1], K. Sakurai[1], T. Yamashita[1], J. Zhou[1], R. Tachibana[1], T. Takagiwa[1], T. Sugimoto[1], M. Ogawa[1], Y. Ochi[1], K. Kawaguchi[1], M. Kojima[1], T. Ogawa[1], T. Hashiguchi[1], R. Fukuda[1], M. Masuda[1], K. Kawakami[1], T. Someya[1], Y. Kajitani[1], Y. Matsumoto[1], N. Morozumi[1], J. Sato[1], N. Raghunathan[2], Y. L. Koh[2], S.Chen[2], J. Lee[2], H. Nasu[2], H. Sugawara[2], K. Hosono[1], T. Hisada[1], T. Kaneko[1], H. Nakamura[1]

[1]Toshiba Memory, Yokohama, Japan; [2]Western Digital, Milpitas, CA

10:45 AM

13.2 A 3.6Mb 10.1Mb/mm² Embedded Non-Volatile ReRAM Macro in 22nm FinFET Technology with Adaptive Forming/Set/Reset Schemes Yielding Down to 0.5V with Sensing Time of 5ns at 0.7V

P. Jain, U. Arslan, M. Sekhar, B. C. Lin, L. Wei, T. Sahu, J. Alzate-vinasco, A. Vangapaty, M. Meterelliyoz, N. Strutt, A. B. Chen, P. Hentges, P. A. Quintero, C. Connor, O. Golonzka, K. Fischer, F. Hamzaoglu

Intel, Hillsboro, OR

11:15 AM

13.3 A 7Mb STT-MRAM in 22FFL FinFET Technology with 4ns Read Sensing Time at 0.9V Using Write-Verify-Write Scheme and Offset-Cancellation Sensing Technique

L. Wei, J. G. Alzate, U. Arslan, J. Brockman, N. Das, K. Fischer, T. Ghani, O. Golonzka, P. Hentges, R. Jahan, P. Jain, B. Lin, M. Meterelliyoz, J. ODonnell, C. Puls, P. Quintero, T. Sahu, M. Sekhar, A. Vangapaty, C. Wiegand, F. Hamzaoglu

Intel, Hillsboro, OR

11:30 AM

13.4 A 512Gb 3-bit/Cell 3D 6th-Generation V-NAND Flash Memory with 82MB/s Write Throughput and 1.2Gb/s Interface

D. Kang, M. Kim, S. C. Jeon, W. Jung, J. park, G. Choo, D-K. Shim, A. Kavala, S-B. Kim, K-M. Kang, J. Lee , K. Ko, H-W. Park, B-J. Min, C. Yu, S. Yun, N. Kim, Y. Jung, S. Seo, S. Kim, M. K. Lee, J-Y. Park, J. C. Kim, Y. S. Cha, K. Kim, Y. Jo, H. Kim, Y. Choi, J. Byun, J-H. Park, K. Kim, T-H. Kwon, Y. Min, C. Yoon, Y. Kim, D-H. Kwak, E. Lee, W-G. Hahn, K-S. Kim, K. Kim, E. Yoon, W-T. Kim, I. Lee, S. H. Moon, J. Ihm, D. S. Byeon, K-W. Song, S. Hwang, K. H. Kyung

Samsung Electronics, Hwasung, Korea

11:45 AM

13.5 A 512Gb 3-bit/Cell 3D Flash Memory on 128-Wordline-Layer with 132MB/s Write Performance Featuring Circuit-Under-Array Technology

C. Siau[1], K-H. Kim[1], S. Lee[1], K. Isobe[2], N. Shibata[2], K. Verma[1], T. Ariki[1], J. Li[1], J. Yuh[1], A. Amarnath[1], Q. Nguyen[1], O. Kwon[1], S. Jeong[1], H. Li[1], H-L. Hsu[1], T-Y. Tseng[1], S. Choi[1], S. Darne[1], P. Anantula[1], A. Yap[1], H. Chibvongodze[1], H. Miwa[1], M. Yamashita[1], M. Watanabe[1], K. Hayashi[1], Y. Kato[1], T. Miwa[1], J. Y. Kang[1], M. Okumura[1], N. Ookuma[1], M. Balaga[1], V. Ramachandra[1], A. Matsuda[1], S. Kulkani[1], R. Rachineni[1], P. K. Manjunath[1], M. Takehara[1], A. Pai[1], S. Rajendra[1], T. Hisada[2], R. Fukuda[2], N. Tokiwa[2], K. Kawaguchi[2], M. Yamaoka[2], H. Komai[2], T. Minamoto[2], M. Unno[2], S. Ozawa[2], H. Nakamura[2], T. Hishida[2], Y. Kajitani[2], L. Lin[1]

[1]Western Digital, Milpitas, CA; [2]Toshiba Memory, Yokohama, Japan

Conclusion 12:15 PM

Machine Learning & Digital LDO Circuits

Session Chair: ***Vivek De,*** *Intel, Beaverton, OR*
Associate Chair: ***Ping-Ying Wang,*** *CMOS-Crystal Technology, Zhubei City, Hsinchu County, Taiwan*

1:30 PM

14.1 A 65nm 1.1-to-9.1TOPS/W Hybrid-Digital-Mixed-Signal Computing Platform for Accelerating Model-Based and Model-Free Swarm Robotics DS2

N. Cao, M. Chang, A. Raychowdhury
Georgia Institute of Technology, Atlanta, GA

2:00 PM

14.2 A Compute SRAM with Bit-Serial Integer/Floating-Point Operations for Programmable In-Memory Vector Acceleration

J. Wang, X. Wang, C. Eckert, A. Subramaniyan, R. Das, D. Blaauw, D. Sylvester
University of Michigan, Ann Arbor, MI

2:30 PM

14.3 A 43pJ/Cycle Non-Volatile Microcontroller with 4.7µs Shutdown/Wake-up Integrating 2.3-bit/Cell Resistive RAM and Resilience Techniques DS2

T. F. Wu[1], B. Q. Le[1], R. Radway[1], A. Bartolo[1], W. Hwang[1], S. Jeong[1], H. Li[1], P. Tandon[1], E. Vianello[2], P. Vivet[2], E. Nowak[2], M. K. Wootters[1], H-S. P. Wong[1], M. M. Sabry Aly[3], E. Beigne[2], S. Mitra[1]
[1]Stanford University, Stanford, CA
[2]CEA-LETI-MINATEC, Grenoble, France
[3]Nanyang Technological University, Singapore

Break 3:00 PM

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14.4 All-Digital Time-Domain CNN Engine Using Bidirectional Memory Delay Lines for Energy-Efficient Edge Computing

A. Sayal, S. Fathima, S. T. Nibhanupudi, J. P. Kulkarni
University of Texas, Austin, TX

3:45 PM

14.5 A 0.6-to-1.1V Computationally Regulated Digital LDO with 2.79-Cycle Mean Settling Time and Autonomous Runtime Gain Tracking in 65nm CMOS

X. Sun, A. Boora, W. Zhang, V. R. Pamula, V. Sathe
University of Washington, Seattle, WA

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14.6 A 745pA Hybrid Asynchronous Binary-Searching and Synchronous Linear-Searching Digital LDO with 3.8×10^5 Dynamic Load Range, 99.99% Current Efficiency, and 2mV Output Voltage Ripple

S. Li, B. H. Calhoun
University of Virginia, Charlottesville, VA

4:45 PM

14.7 A Modular Hybrid LDO with Fast Load-Transient Response and Programmable PSRR in 14nm CMOS Featuring Dynamic Clamp Tuning and Time-Constant Compensation

X. Liu, H. K. Krishnamurthy, T. Na, S. Weng, K. Z. Ahmed, K. Ravichandran, J. Tschanz, V. De
Intel, Hillsboro, OR

Conclusion 5:15 PM

Power for 5G, Wireless Power, and GaN Converters

Session Chair: ***Min Chen,*** *Analog Devices, Milpitas, CA*
Associate Chair: ***Johan Janssens,*** *ON Semiconductor, Mechelen, Belgium*

1:30 PM

15.1 An 88%-Efficiency Supply Modulator Achieving 1.08µs/V Fast Transition and 100MHz Envelope-Tracking Bandwidth for 5G New Radio RF Power Amplifier
J-S. Paek, D. Kim, J-S. Bang, J. Baek, J. Choi, T. Nomiyama, J. Han, Y. Choo, Y. Youn, E. Park, S. Lee, I-H. Kim, J. Lee, T. B. Cho, I. Kang
Samsung Electronics, Hwaseong, Korea

2:00 PM

15.2 A 90ns/V Fast-Transition Symbol-Power-Tracking Buck Converter for 5G mm-Wave Phased-Array Transceiver
J-S. Paek, T. Nomiyama, J. Han, I-H. Kim, Y. Lee, D. Kim, E. Park, S. Lee, J. Lee, T. B. Cho, I. Kang, Samsung Electronics, Hwaseong, Korea

2:30 PM

15.3 A 100W and 91% GaN-Based Class-E Wireless-Power-Transfer Transmitter with Differential-Impedance-Matching Control for Charging Multiple Devices
C-Y. Xie[1], S-H. Yang[1], S-F. Lu[1], F-Y. Lin[1], Y-A. Lin[1], Y-Z. Ou-Yang[1], K-H. Chen[1], K-C. Liu[1], Y-H. Lin[2]
[1]National Chiao Tung University, Hsinchu, Taiwan
[2]Realtek Semiconductor, Hsinchu, Taiwan

Break 3:00 PM

3:15 PM

15.4 A 52% Peak-Efficiency >1W Isolated Power Transfer System Using Fully Integrated Magnetic-Core Transformer
Z. Yue[1], M. Shaoyu[2], Z. Tianting[1], Q. Wenhui[2], Z. Yuanyuan[3], G. Yingjie[1], C. Baoxing[3]
[1]Analog Devices, Beijing, China; [2]Analog Devices, Shanghai, China
[3]Analog Devices, Wilmington, MA

3:45 PM

15.5 An 800mW Fully Integrated Galvanic Isolated Power Transfer System Meeting CISPR 22 Class-B Emission Levels with 6dB Margin
W. Qin[1], X. Yang[2], S. Ma[1], F. Liu[2], Y. Zhao[3], T. Zhao[2], B. Chen[3]
[1]Analog Devices, Shanghai, China; [2]Analog Devices, Beijing, China
[3]Analog Devices, Wilmington, MA

4:15 PM

15.6 A 10MHz *i*-Collapse Failure Self-Prognostic GaN Power Converter with T_J-Independent In-Situ Condition Monitoring and Proactive Temperature Frequency Scaling
Y. Chen, D. B. Ma, University of Texas at Dallas, Richardson, TX

4:45 PM

15.7 An 8.3MHz GaN Power Converter Using Markov Continuous RSSM for 35dBµV Conducted EMI Attenuation and One-Cycle T_{ON} Rebalancing for 27.6dB V_0 Jittering Suppression
Y. Chen, D. B. Ma, University of Texas at Dallas, Richardson, TX

5:00 PM

15.8 A 4.5V/ns Active Slew-Rate-Controlling Gate Driver with Robust Discrete-Time Feedback Technique for 600V Superjunction MOSFETs
S. Kawai, T. Ueno, K. Onizuka, Toshiba, Kawasaki, Japan

Conclusion 5:15 PM

Frequency Synthesizers

Session Chair: ***Xiang Gao,*** *Zhejiang University, Hangzhou, China*
Associate Chair: ***Jaehyouk Choi,*** *Ulsan National Institute of Science Technology, Ulsan, Korea*

1:30 PM

16.1 A 265µW Fractional-N Digital PLL with Seamless Automatic Switching Subsampling/Sampling Feedback Path and Duty-Cycled Frequency-Locked Loop in 65nm CMOS
H. Liu, Z. Sun, H. Huang, W. Deng, T. Siriburanon, J. Pang, Y. Wang, R. Wu, T. Someya, A. Shirane, K. Okada
Tokyo Institute of Technology, Tokyo, Japan

2:00 PM

16.2 A 76fs$_{rms}$ Jitter and —40dBc Integrated-Phase-Noise 28-to-31GHz Frequency Synthesizer Based on Digital Sub-Sampling PLL Using Optimally Spaced Voltage Comparators and Background Loop-Gain Optimization
J. Kim, H. Yoon*, Y. Lim*, Y. Lee, Y. Cho, T. Seong, J. Choi*
Ulsan National Institute of Science and Technology, Ulsan, Korea; *Equally-Credited Authors (ECAs)

2:15 PM

16.3 A -246dB Jitter-FoM 2.4GHz Calibration-Free Ring-Oscillator PLL Achieving 9% Jitter Variation Over PVT
X. Yang[1], C-H. Chan[1], Y. Zhu[1], R. P. Martins[1,2]
[1]University of Macau, Macau, China
[2]Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

2:30 PM

16.4 A 0.5-to-2.5GHz Multi-Output Fractional Frequency Synthesizer with 90fs Jitter and –106dBc Spurious Tones Based on Digital Spur Cancellation
S-Y. Hung, S. Pamarti
University of California, Los Angeles, CA

Break 3:00 PM

3:15 PM

16.5 DS2 A Fractional-N Synthesizer with 110fs$_{rms}$ Jitter and a Reference Quadrupler for Wideband 802.11ax
F. Song[1], Y. Zhao[1], B. Wu[1], L. Tang[1], L. Lin[1], B. Razavi[2]
[1]Ubilinx Technology, San Jose, CA; [2]University of California, Los Angeles, CA

3:30 PM

16.6 A Calibration-Free Triple-Loop Bang-Bang PLL Achieving 131fs$_{rms}$ Jitter and -70dBc Fractional Spurs
D. Yang[1], A. Abidi[1], H. Darabi[2], H. Xu[1], D. Murphy[2], H. Wu[2], Z. Wang[3]
[1]University of California, Los Angeles, CA; [2]Broadcom, Irvine, CA
[3]Columbia University, New York, NY

4:00 PM

16.7 A 30GHz Digital Sub-Sampling Fractional-N PLL with 198fs$_{rms}$ Jitter in 65nm LP CMOS
L. Grimaldi, L. Bertulessi, S. Karman, D. Cherniak, A. Garghetti, C. Samori, A. L. Lacaita, S. Levantino
Politecnico di Milano, Milan, Italy

4:30 PM

16.8 A 25.4-to-29.5GHz 10.2mW Isolated Sub-Sampling PLL Achieving -252.9dB Jitter-Power FoM and -63dBc Reference Spur
Z. Yang[1], Y. Chen[1], S. Yang[1], P-I. Mak[1], R. P. Martins[1,2]
[1]University of Macau, Macau, China
[2]Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

4:45 PM

16.9 4.48GHz 0.18µm SiGe BiCMOS Exact-Frequency Fractional-N Frequency Synthesizer with Spurious-Tone Suppression Yielding a -80dBc In-Band Fractional Spur
M. P. Kennedy[1,2], Y. Donnelly[1,3], J. Breslin[4], S. Tulisi[4], S. Patil[4], C. Curtin[4], S. Brookes[4], B. Shelly[4], P. Griffin[4], M. Keaveney[4]
[1]University College Dublin, Dublin, Ireland; [2]Microelectronic Circuits Centre Ireland, Dublin, Ireland
[3]Microelectronic Circuits Centre Ireland, Cork, Ireland; [4]Analog Devices, Limerick, Ireland

Conclusion 5:15 PM

Technologies for Human Interaction & Health

Session Chair: ***Patrick Mercier,*** *University of California, San Diego, La Jolla, CA*
Associate Chair: ***Shuichi Nagai,*** *Panasonic, Moriguchi, Osaka, Japan*

1:30 PM

17.1 AI x Robotics: Technology Challenges and Opportunities in Sensors, Actuators, and Integrated Circuits DS2
M. Fujita
Sony, Tokyo, Japan

2:00 PM

17.2 A 142nW Voice and Acoustic Activity Detection Chip for mm-Scale Sensor Nodes Using Time-Interleaved Mixer-Based Frequency Scanning
M. Cho, S. Oh*, Z. Shi, J. Lim, Y. Kim, S. Jeong, Y. Chen, D. Blaauw, H-S. Kim, D. Sylvester*
University of Michigan, Ann Arbor, MI; *Equally-Credited Authors (ECAs)

2:30 PM

17.3 Hybrid System for Efficient LAE-CMOS Interfacing in Large-Scale Tactile-Sensing Skins via TFT-Based Compressed Sensing
L. E. Aygun, P. Kumar*, Z. Zheng*, T-S. Chen*, S. Wagner, J. C. Sturm, N. Verma*
Princeton University, Princeton, NJ; *Equally-Credited Authors (ECAs)

Break 3:00 PM

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17.4 16MHz FRAM Micro-Controller with a Low-Cost Sub-1μA Embedded Piezo-Electric Strain Sensor for ULP Motion Detection DS2
S. Khanna[1], M. Zwerg[1], B. Elies[1], J. Luebbe[1], N. Krishnasawamy[1], H. Najar[2], S. Bellary[2], W-Y. Shih[1], S. Summerfelt[1], S. Bartling[1]
[1]Texas Instruments, Dallas, TX
[2]Texas Instruments, Santa Clara, CA

3:30 PM

17.5 A 0.8mm³ Ultrasonic Implantable Wireless Neural Recording System with Linear AM Backscattering
M. M. Ghanbari, D. K. Piech, K. Shen, S. Faraji Alamouti, C. Yalcin, B. C. Johnson, J. M. Carmena, M. M. Maharbiz, R. Muller
University of California, Berkeley, CA

3:45 PM

17.6 A Sub-40μW 5Mb/s Magnetic Human Body Communication Transceiver Demonstrating Trans-Body Delivery of High-Fidelity Audio to a Wearable In-Ear Headphone
J. Park, P. P. Mercier
University of California, San Diego, La Jolla, CA

4:15 PM

17.7 A 7.0fps Optical and Electrical Dual Tomographic Imaging SoC for Skin-Disease Diagnosis System
Y. Lee, K. Kim, J. Lee, K-R. Lee, S. Gweon, M. Kim, H-J. Yoo
KAIST, Daejeon, Korea

4:45 PM

17.8 A 2.6μW Monolithic CMOS Photoplethysmographic Sensor Operating with 2μW LED Power DS2
A. Caizzone, A. Boukhayma, C. Enz
EPFL, Neuchâtel, Switzerland

Conclusion 5:15 PM

Analog Techniques

Session Chair: ***David Blaauw,*** *University of Michigan, Ann Arbor, MI*
Associate Chair: ***Byungsub Kim,*** *POSTECH, Pohang, Gyeongbuk, Korea*

1:30 PM

18.1 A -105dBc THD+N (-114dBc HD2) at 2.8V_{PP} Swing and 120dB DR Audio Decoder with Sample-and-Hold Noise Filtering and Poly Resistor Linearization Schemes
S-H. Wen, K-D. Chen, C-H. Hsiao, Y-C. Chen, MediaTek, Hsinchu, Taiwan

2:00 PM

18.2 A 16fJ/Conversion-Step Time-Domain Two-Step Capacitance-to-Digital Converter
X. Tang[1], S. Li[1], L. Shen[1], W. Zhao[1], X. Yang[1], R. Williams[1], J. Liu[2], Z. Tan[3], N. Hall[1], N. Sun[1]
[1]University of Texas, Austin, TX
[2]University of Electronic Science and Technology of China, Chengdu, China
[3]Analog Devices, Boston, MA

2:30 PM

18.3 An Auto-Zero Stabilized Voltage Buffer with a Quiet Chopping Scheme and Constant Input Current
T. Rooijers, J. H. Huijsing, K. A. A. Makinwa
Delft University of Technology, Delft, The Netherlands

Break 3:00 PM

3:15 PM

18.4 A 0.55nW/0.5V 32kHz Crystal Oscillator Based on a DC-Only Sustaining Amplifier for IoT DS2
H. Esmaeelzadeh, S. Pamarti, University of California, Los Angeles, CA

3:45 PM

18.5 A 54MHz Crystal Oscillator with 30× Start-Up Time Reduction Using 2-Step Injection in 65nm CMOS
K. M. Megawer[1], N. Pal[1], A. Elkholy[1], M. G. Ahmed[1], A. Khashaba[1], D. Griffith[2], P. K. Hanumolu[1]
[1]University of Illinois, Urbana-Champaign, IL; [2]Texas Instruments, Dallas, TX

4:15 PM

18.6 A 32MHz Crystal Oscillator with Fast Startup Using Synchronized Signal Injection
B. Verhoef[1], J. Prummel[2], W. Kruiskamp[2], R. Post[2]
[1]Dialog Semiconductor, Hengelo, The Netherlands
[2]Dialog Semiconductor, 's-Hertogenbosch, The Netherlands

4:30 PM

18.7 A 0.7V, 2.35% 3σ-Accuracy Bandgap Reference in 12nm CMOS
Y-W. Chen, J-J. Horng, C-H. Chang, A. Kundu, Y-C. Peng, M. Chen
TSMC, Hsinchu, Taiwan

4:45 PM

18.8 A 192pW Hybrid Bandgap-V_{th} Reference with Process Dependence Compensated by a Dimension-Induced Side-Effect
Y. Ji, J. Lee, B. Kim, H-J. Park, J-Y. Sim
Pohang University of Science and Technology, Pohang, Korea

Conclusion 5:15 PM

Demonstration Session 2, Tuesday, February 19th, 5:00-7:00 PM

This year, the Demonstration Session extending in selected regular papers, both Academic and Industrial, will take place on Monday February 18th, and Tuesday February 19th, from 5 pm until 7 pm in the Golden Gate Hall. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2019, as noted by the symbol DS2

9.3 A 680µW Burst-Chirp UWB Radar Transceiver for Vital Signs and Occupancy Sensing up to 15m Distance

9.4 A 145GHz FMCW-Radar Transceiver in 28nm CMOS

9.5 An 80Gb/s 300GHz-Band Single-Chip CMOS Transceiver

9.7 A Scalable 71-to-76GHz 64-Element Phased-Array Transceiver Module with 2×2 Direct-Conversion IC in 22nm FinFET CMOS Technology

10.1 An Energy Measurement Front-End with Integrated In-Situ Background Full System Accuracy Monitoring Including the Current and Voltage Sensors

10.2 A 22ng/√Hz 17mW MEMS Accelerometer with Digital Noise-Reduction Techniques

11.5 A 512-Pixel 3kHz-Frame-Rate Dual-Shank Lensless Filterless Single-Photon-Avalanche-Diode CMOS Neural Imaging Probe

12.2 Micro Short-Circuit Detector Including S/H Circuit for 1hr Retention and 52dB Comparator Composed of C-Axis Aligned Crystalline IGZO FETs for Li-Ion Battery Protection IC

14.1 A 65nm 1.1-to-9.1TOPS/W Hybrid-Digital-Mixed-Signal Computing Platform for Accelerating Model-Based and Model-Free Swarm Robotics

14.3 A 43pJ/Cycle Non-Volatile Microcontroller with 4.7µs Shutdown/Wake-up Integrating 2.3-bit/Cell Resistive RAM and Resilience Techniques

16.5 A Fractional-N Synthesizer with 110fs$_{rms}$ Jitter and a Reference Quadrupler for Wideband 802.11ax

17.1 AI x Robotics: Technology Challenges and Opportunities in Sensors, Actuators, and Integrated Circuits

17.4 16MHz FRAM Micro-Controller with a Low-Cost Sub-1µA Embedded Piezo-Electric Strain Sensor for ULP Motion Detection

17.8 A 2.6µW Monolithic CMOS Photoplethysmographic Sensor Operating with 2µW LED Power

18.4 A 0.55nW/0.5V 32kHz Crystal Oscillator Based on a DC-Only Sustaining Amplifier for IoT

21.1 A 28GHz CMOS Phased-Array Beamformer Utilizing Neutralized Bi-Directional Technique Supporting Dual-Polarized MIMO for 5G NR

22.1 A 769µW Battery-Powered Single-Chip SoC with BLE for Multi-Modal Vital Sign Health Patches

22.4 A 27.8µW Biopotential Amplifier Tolerant to 30V$_{pp}$ Common-Mode Interference for Two-Electrode ECG Recording in 0.18µm CMOS

23.4 A 512GB 1.1V Managed DRAM Solution with 16GB ODP and Media Controller

25.3 A 128b AES Engine with Higher Resistance to Power and Electromagnetic Side-Channel Attacks Enabled by a Security-Aware Integrated All-Digital Low-Dropout Regulator

27.4 Multi-Beam Shared-Inductor Reconfigurable Voltage/SECE-Mode Piezoelectric Energy Harvesting of Multi-Axial Human Motion

28.1 A 0.42nW 434MHz -79.1dBm Wake-Up Receiver with a Time-Domain Integrator

29.2 A Scalable Quantum Magnetometer in 65nm CMOS with Vector-Field Detection Capability

29.4 Ultra-Low-Power Atomic Clock for Satellite Constellation with 2.2×10^{-12} Long-Term Allan Deviation Using Cesium Coherent Population Trapping

TIMETABLE OF ISSCC 2019 SESSIONS

ISSCC 2019 • Sunday February 17th

Tutorials

8:30 AM	**T1:** Fundamentals of Integrated Radars	**T2:** Fundamentals of Power-Conversion Topologies	**T3:** Advances and Prospects for In-Memory Computing
10:30 AM	**T4:** Fundamentals of Efficient IoT Microcontrollers	**T5:** Noise-Shaping in Data Converters	**T6:** Basics of Clock-and-Data-Recovery Circuits
1:30 PM	**T7:** Hardware Security – from Basics to ASICs	**T8:** Current-Sensing Techniques	
3:30 PM	**T9:** Calibration Techniques for Wireless Transceivers	**T10:** Low-Noise Sensor Interfaces	

Forums

8:00 AM	**F1:** Sub-6GHz 5G Radio Circuits and Systems: From Concepts to Silicon	**F2:** Memory-Centric Computing from IoT to Artificial Intelligence and Machine Learning

Events Below in Bold Box are Included with your Conference Registration

Evening Events

7:30 PM EE1: Student Research Preview: Short Presentations with Poster Session

6:00 PM **EE2:** How to Save Lives With Circuits

ISSCC 2019 • Monday February 18th • Paper Sessions

8:30 AM	**Session 1:** Plenary Session				
1:30 PM	**Session 2:** Processors	**Session 3:** Nyquist-Rate ADCs	**Session 4:** Power Amplifiers	**Session 5:** Image Sensors	**Session 6:** Ultra-High-Speed Wireline

12noon to 7:00 PM – Book Displays • 5:00 PM to 7:00 PM – Demonstration Session • 5:15 PM – Author Interviews • Social Hour

Evening Events

7:00 PM **EE3:** Making a Career Choice

8:00 PM **EE4:** Industry Showcase

ISSCC 2019 • Tuesday February 19th • Paper Sessions

8:30 AM	**Session 7:** Machine Learning	**Session 8:** DC-DC Converters	**Session 9:** High-Frequency Transceivers for Radar and Communications	**Session 10:** Sensor Interfaces **Session 11:** Diagnostics	**Session 12:** Emerging Technologies **Session 13:** Non-Volatile Memories
1:30 PM	**Session 14:** Machine Learning & Digital LDO Circuits	**Session 15:** Power for 5G, Wireless Power, and GaN Converters	**Session 16:** Frequency Synthesizers	**Session 17:** Technologies for Human Interaction & Health	**Session 18:** Analog Techniques

10:00 AM to 7:00 PM – Book Displays • 5:00 PM to 7:00 PM – Demonstration Session • 5:15 PM – Author Interviews • Social Hour

Evening Events

8:00 PM **EE5:** Moving to 'The Dark Side'!

EE6: How Can Hardware Designers Reclaim the Spotlight?

ISSCC 2019 • Wednesday February 20th • Paper Sessions

8:30 AM	**Session 19:** Adaptive Digital & Clocking Techniques	**Session 20:** Noise-Shaped & VCO-Based ADCs	**Session 21:** 4G/5G Transceivers	**Session 22:** Physiological Monitoring	**Session 23:** DRAM **Session 24:** SRAM & Computation-in-Memory
1:30 PM	**Session 25:** Circuits Enabling Security **Session 26:** Frequency Generation & Interference Mitigation	**Session 27:** Energy Harvesting & DC/DC Control Techniques	**Session 28:** Techniques for Low-Power & High-Performance Wireless	**Session 29:** Quantum & Photonics Technologies	**Session 30:** Advanced Wireline Techniques

10:00 AM to 3:00 PM – Book Displays • 5:15 PM – Author Interviews

ISSCC 2019 • Thursday February 21st

8:00 AM	**Short Course:** Integrated Phased Arrays: Theory, Practice, and Implementation for 5G and Beyond	**F3:** The Complete Advanced Driver-Assistance System (ADAS) Sensing Network	**F4:** Intelligence at the Edge: How Can We Make Machine Learning More Energy Efficient?	**F5:** 56Gb/s to 112Gb/s and Beyond – Design Challenges and Solutions in Wireline Communications	**F6:** The Right Tool for the Job: Application-Optimized Data Converters

EE5: "Moving to The Dark Side"

Organizers: **Jan Westra,** *Broadcom, Bunnik, The Netherlands*
Matt Straayer, *Maxim, North Chelmsford, MA*

Many practicing engineers view management and business as 'The Dark Side', and executive decisions often baffle them. Can engineers do a good job on 'The Dark Side' in management and business? Is it possible to return to engineering from 'The Dark Side'?

The relation between business and management on one side and engineering on the other side has always been complex. On one hand, innovative engineers often don't understand the limitations imposed on them by more financially driven business managers. On the other hand, business needs solid engineering, within their budgetary boundaries, in order to be successful. Is it possible to transform from a good engineer to a good business manager? Can business managers return to engineering and be successful engineers after having spent time on 'The Dark Side'? Can engineers and business managers peacefully coexist, and are they able to understand each other? Is that a situation we should work towards or, is a world where each side sees the other as a necessary evil perfectly balanced and sustainable?

In an entertaining and educational discussion between the panelists, the audience will get a closer look into the hearts and minds of Captains of Industry, sharing their views on the subject. How do they view the world after moving to 'The Dark Side' and have they truly moved to 'The Dark Side'?

Join this panel discussion with active audience interaction, take a seat in the tribunal and make your vote count!

Moderator: Matt Straayer, *Maxim, North Chelmsford, MA*

Panelists

Anthony Collins, *Xilinx, Dublin, Ireland*
Kavé Kianush, *Catena, Delft, The Netherlands*
Curtis Ling, *MaxLinear, Carlsbad, CA*
Jen Lloyd, *Analog Devices, San Jose, CA*
Tyson Tuttle, *Silicon Labs, Austin, TX*
Patrick Yue, *Hong Kong University of Science and Technology (HKUST), Hong Kong*

EE6: "How Can Hardware Designers Reclaim the Spotlight?"

Organizers: **Sudhakar Pamarti,** *UCLA, Los Angeles, CA*
Nagendra Krishnapura, *IIT Madras, Chennai, India*
Mike Shuo-Wei Chen, *USC, Los Angeles, CA*

Gone seem the heady days when hardware innovation drove entrepreneurship in communications, computing, and other domains. The bar for circuit innovation and design has been inexorably climbing higher, even as circuit components are becoming increasingly commoditized and seemingly losing relevance in the larger scheme of things.

Is this trend here to stay? Should we do something about it? What should we do? Are long hardware design cycles to blame? Can we learn something from software design practices? Or, are there new opportunities where hardware innovation can still play a central role? If so, how far out is the horizon? How do we prepare for these opportunities?

This evening panel assembles a galaxy of international experts from academia, government, and both the hardware and software industries to discuss these issues. The experts will diagnose the situation, offer insightful prognoses, and engage in a lively discussion with each other, and with the audience. Come join us to see if you agree with our experts and for an opportunity to enlighten us with your opinion.

Moderator: Mike Shuo-Wei Chen, *University of Southern California, Los Angeles, CA*

Panelists

Luca Benini, *ETH Zurich, Zurich, Switzerland, and Universita di Bologna, Bologna, Italy*
Bill Dally, *NVIDIA, Santa Clara, CA*
Varada Gopalakrishnan, *Amazon Lab126, Sunnyvale, CA*
Colin Lyden, *Analog Devices, Limerick, Ireland*
Liam Madden, *Xilinx, San Jose, CA*
Andreas Olofsson, *DARPA, Arlington, VA*
***Shaojun Wei**, Tsinghua University, Beijing, China*

Adaptive Digital & Clocking Techniques

Session Chair: ***John Maneatis,*** *True Circuits, Los Altos, CA*
Associate Chair: ***Alicia Klinefelter,*** *Nvidia, Durham, NC*

8:30 AM

19.1 Computationally Enabled Total Energy Minimization Under Performance Requirements for a Voltage-Regulated 0.38-to-0.58V Microprocessor in 65nm CMOS

F. U. Rahman, R. Pamula, A. Boora, X. Sun, V. Sathe
University of Washington, Seattle, WA

9:00 AM

19.2 A 6.4pJ/Cycle Self-Tuning Cortex-M0 IoT Processor Based on Leakage-Ratio Measurement for Energy-Optimal Operation Across Wide-Range PVT Variation

J. Lee[1], Y. Zhang[1], Q. Dong[1], W. Lim[1], M. Saligane[1], Y. Kim[1], S. Jeong[1], J. Lim[1], M. Yasuda[2], S. Miyoshi[3], M. Kawaminami[2,3], D. Blaauw[1], D. Sylvester[1]
[1]University of Michigan, Ann Arbor, MI
[2]Mie Fujitsu Semiconductor Limited, Kuwana, Japan
[3]Fujitsu Electronics America, Inc., Sunnyvale, CA

9:30 AM

19.3 A 7nm All-Digital Unified Voltage and Frequency Regulator Based on a High-Bandwidth 2-Phase Buck Converter with Package Inductors

F. I. Atallah[1], K. A. Bowman[1], H. H. Nguyen[1], J. Jeong[1], D. Yingling[1], Y. Sun[1], B. Appel[1], A. Polomik[1], M. Harinath[1], J. Morelli[1], T. Moore[1], N. Reeves[2], A. Cassier[2], A. Raychoudhury[3]
[1]Qualcomm, Raleigh, NC; [2]Qualcomm, San Diego, CA
[3]Georgia Institute of Technology, Atlanta, GA

Break 10:00 AM

10:15 AM

19.4 An Adaptive Clock Management Scheme Exploiting Instruction-Based Dynamic Timing Slack for a General-Purpose Graphics Processor Unit with Deep Pipeline and Out-of-Order Execution

T. Jia, R. Joseph, J. Gu, Northwestern University, Evanston, IL

10:45 AM

19.5 Digital Leakage Compensation for a Low-Power and Low-Jitter 0.5-to-5GHz PLL in 10nm FinFET CMOS Technology

Y. Fan, B. Xiang, D. Zhang, J. S. Ayers, K-Y. J. Shen, A. Mezhiba, Intel, Hillsboro, OR

11:15 AM

19.6 A 40-to-80MHz Sub-4µW/MHz ULV Cortex-M0 MCU SoC in 28nm FDSOI with Dual-Loop Adaptive Back-Bias Generator for 20µs Wake-Up From Deep Fully Retentive Sleep Mode

D. Bol[1], M. Schramme[1], L. Moreau[1], T. Haine[1], P. Xu[1], C. Frenkel[1], R. Dekimpe[1], F. Stas[2], D. Flandre[1]
[1]UCLouvain, Louvain-la-Neuve, Belgium
[2]e-peas semiconductors, Louvain-la-Neuve, Belgium

11:45 AM

19.7 A Scalable Pipelined Time-Domain DTW Engine for Time-Series Classification Using Multibit Time Flip-Flops with 140Giga-Cell-Updates/s Throughput

Z. Chen, J. Gu, Northwestern University, Evanston, IL

Conclusion 12:15 PM

Noise-Shaped & VCO-Based ADCs

Session Chair: ***Yun-Shiang Shu,*** *Mediatek, Hsinchu, Taiwan*
Associate Chair: ***Bob Verbruggen,*** *Xilinx, Saggart, Ireland*

8:30 AM

20.1 A 5GS/s 7.2 ENOB Time-Interleaved VCO-Based ADC Achieving 30.5fJ/conv-step
M. Baert, W. Dehaene
KU Leuven, Heverlee, Belgium

9:00 AM

20.2 A 40MHz-BW 320MS/s Passive Noise-Shaping SAR ADC with Passive Signal-Residue Summation in 14nm FinFET
Y-Z. Lin, C-Y. Lin*, S-C. Tsou, C-H. Tsai, C-H. Lu*
MediaTek, Hsinchu, Taiwan; *Equally-Credited Authors (ECAs)

9:30 AM

20.3 A 50MHz-Bandwidth 70.4dB-SNDR Calibration-Free Time-Interleaved 4th-Order Noise-Shaping SAR ADC
L. Jie, B. Zheng, M. P. Flynn
University of Michigan, Ann Arbor, MI

Break 10:00 AM

10:15 AM

20.4 An 8×-OSR 25MHz-BW 79.4dB/74dB DR/SNDR CT ΔΣ Modulator Using 7b Linearized Segmented DACs with Digital Noise-Coupling-Compensation Filter in 7nm FinFET CMOS
T-Y. Lo, C-H. Weng, H-Y. Hsieh, T-Y. Wang, Y-S. Shu, P-C. Chiu
MediaTek, Hsinchu, Taiwan

10:45 AM

20.5 A 76.6dB-SNDR 50MHz-BW 29.2mW Noise-Coupling-Assisted CT Sturdy MASH ΔΣ Modulator with 1.5b/4b Quantizers in 28nm CMOS
L. Qi[1], A. Jain[2], D. Jiang[1], S-W. Sin[1], R. P. Martins[1,3], M. Ortmanns[2]
[1]University of Macau, Macau, China
[2]University of Ulm, Ulm, Germany
[3]Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

11:15 AM

20.6 An 80MHz-BW 31.9fJ/conv-step Filtering ΔΣ ADC with a Built-In DAC-Segmentation/ELD-Compensation 6b 960MS/s SAR-Quantizer in 28nm LP for 802.11ax Applications
C-Y. Wang, J-H. Tsai, S-Y. Su, J-C. Tsai, J-R. Chen, C-H. Lou
MediaTek, Hsinchu, Taiwan

11:45 AM

20.7 A 72.6dB-SNDR 100MHz-BW 16.36mW CTDSM with Preliminary Sampling and Quantization Scheme in Backend Subranging QTZ
W. Wang[1], C-H. Chan[1], Y. Zhu[1], R. P. Martins[1,2]
[1]University of Macau, Macau, China
[2]Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

Conclusion 12:15 PM

4G/5G Transceivers

Session Chair: ***Yiwu Tang,*** *Qualcomm Technologies, San Diego, CA*
Associate Chair: ***Kyoo Hyun Lim,*** *FCI, Seongnam, Korea*

8:30 AM

21.1 A 28GHz CMOS Phased-Array Beamformer Utilizing Neutralized Bi-Directional Technique Supporting Dual-Polarized MIMO for 5G NR DS2

J. Pang[1], Z. Li[1], R. Kubozoe[1], X. Luo[1], R. Wu[1], Y. Wang[1], D. You[1], A. A. Fadila[1], R. Saengchan[1], T. Nakamura[1], J. Alvin[1], D. Matsumoto[1], A. T. Narayanan[1], B. Liu[1], J. Qiu[1], H. Liu[1], Z. Sun[1], H. Huang[1], K. K. Tokgoz[1], K. Motoi[2], N. Oshima[2], S. Hori[2], K. Kunihiro[2], T. Kaneko[2], A. Shirane[1], K. Okada[1]
[1]Tokyo Institute of Technology, Tokyo, Japan; [2]NEC, Kawasaki, Japan

9:00 AM

21.2 A 27-to-41GHz MIMO Receiver with N-Input-N-Output Using Scalable Cascadable Autonomous Array-Based High-Order Spatial Filters for Instinctual Full-FoV Multi-Blocker/Signal Management

M-Y. Huang, H. Wang, Georgia Institute of Technology, Atlanta, GA

9:30 AM

21.3 A Reconfigurable Bidirectional 28/37/39GHz Front-End Supporting MIMO-TDD, Carrier Aggregation TDD and FDD/Full-Duplex with Self-Interference Cancellation in Digital and Fully Connected Hybrid Beamformers

S. Mondal, R. Singh, J. Paramesh, Carnegie Mellon University, Pittsburgh, PA

Break 10:00 AM

10:15 AM

21.4 An LTE-A Multimode Multiband RF Transceiver with 4RX/2TX Inter-Band Carrier Aggregation, 2-Carrier 4×4 MIMO with 256QAM and HPUE Capability in 28nm CMOS

C-C. Tang[1], Y-B. Lee[1], C-H. E. Sun[1], C-C. Lin[1], J-S. Syu[1], M-H. Wu[1], Y. Chen[2], T-C. Chueh[1], C. Bryant[3], M. Collados[3], M. Hassan[3], J. Ramos[3], Y-L. Hsieh[1], H-H. Chen[1], X. Guo[4], H. Chen[4], C. Cao[4], D. Li[4], J. Strange[3], C. Wang[4], G-K. Dehng[1]
[1]MediaTek, Hsinchu, Taiwan; [2]MediaTek, San Diego, CA
[3]MediaTek, Kent, United Kingdom, [4]MediaTek, Austin, TX

10:45 AM

21.5 A 5G Sub-6GHz Zero-IF and mm-Wave IF Transceiver with MIMO and Carrier Aggregation

B. Jann[1], G. Chance[2], A. Guha Roy[1], A. Balakrishnan[1], N. Karandikar[2], T. Brown[1], X. Li[2], B. Davis[2], J. L. Ceballos[3], N. Tanzi[2], K. Hausmann[2], H. Yoon[2], Y-L. Huang[2], A. Freiman[4], B. Geren[2], P. Pawliuk[2], W. Ballantyne[2]
[1]Intel, Hillsboro, OR; [2]Intel, Chandler, AZ; [3]Intel, Villach, Austria
[4]Intel, Santa Clara, CA

11:15 AM

21.6 A Sub-6GHz 5G New Radio RF Transceiver Supporting EN-DC with 3.15Gb/s DL and 1.27Gb/s UL in 14nm FinFET CMOS

J. Lee, S. Han, J. Lee, B. Kang, J. Bae, J. Jang, S. Oh, S. Ahn, S. Kang, Q-D. Bui, K. Son, H. Lim, D. Jeong, R. Ni, Y. Zuo, I. Jong, C-W. Yao, S. Heo, T. B. Cho, I. Kang
Samsung Electronics, Hwaseong, Korea

11:45 AM

21.7 A Mixed-Signal Circuit Technique for Cancellation of Multiple Modulated Spurs in 4G/5G Carrier-Aggregation Transceivers

S. Sadjina[1,2], K. Dufrêne[1], R. S. Kanumalli[1], M. Huemer[2], H. Pretl[1,2]
[1]Intel DMCE, Linz, Austria; [2]Johannes Kepler University, Linz, Austria

Conclusion 12:15 PM

Physiological Monitoring

Session Chair: ***Esther Rodriguez-Villegas,*** *Imperial College, London, United Kingdom*

Associate Chair: ***Rikky Muller,*** *University of California, Berkeley, Berkeley, CA*

8:30 AM

22.1 DS2 A 769µW Battery-Powered Single-Chip SoC with BLE for Multi-Modal Vital Sign Health Patches

M. Konijnenburg[1], R. van Wegberg[1], S. Song[2], H. Ha[1], W. Sijbers[2], J. Xu[1], S. Stanzione[1], C. van Liempd[1], D. Biswas[2], A. Breeschoten[1], P. Vis[1], C. Van Hoof[1,2,3], N. Van Helleputte[2]
[1]imec - Netherlands, Eindhoven, The Netherlands; [2]imec, Leuven, Belgium
[3]KU Leuven, Heverlee, Belgium

9:00 AM

22.2 A Rugged Wearable Modular ExG Platform Employing a Distributed Scalable Multi-Channel FM-ADC Achieving 101dB Input Dynamic Range and Motion-Artifact Resilience

J. Warchall[1], P. Theilmann[2], Y. Ouyang[2], H. Garudadri[1], P. P. Mercier[1]
[1]University of California, San Diego, La Jolla, CA
[2]MaXentric Technologies, La Jolla, CA

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22.3 A 0.5V 9.26µW 15.28mΩ/√Hz Bio-Impedance Sensor IC with 0.55° Overall Phase Error

K. Kim, J-H. Kim, S. Gweon, J. Lee, M. Kim, Y. Lee, S. Kim, H-J. Yoo
KAIST, Daejeon, Korea

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22.4 DS2 A 27.8µW Biopotential Amplifier Tolerant to 30V_{pp} Common-Mode Interference for Two-Electrode ECG Recording in 0.18µm CMOS

N. Koo, S. Cho, KAIST, Daejeon, Korea

Break 10:00 AM

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22.5 A Bio-Impedance Readout IC with Digital-Assisted Baseline Cancellation for 2-Electrode Measurement

H. Ha[1], W. Sijbers[2], R. van Wegberg[1], J. Xu[1], M. Konijnenburg[1], P. Vis[1], A. Breeschoten[1], S. Song[2], C. Van Hoof[2,3], N. Van Helleputte[2]
[1]imec - Netherlands, Eindhoven, The Netherlands
[2]imec, Heverlee, Belgium; [3]KU Leuven, Heverlee, Belgium

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22.6 A 13-Channel 1.53-mW 11.28-mm² Electrical Impedance Tomography SoC Based on Frequency Division Multiplexing with 10× Throughput Reduction

B. Liu[1,2], G. Wang[1], Y. Li[1], H. Li[1], Y. Gao[1], L. Zeng[2], Y. Ma[1], Y. Lian[1], C. H. Heng[2]
[1]Shanghai Jiao Tong University, Shanghai, China
[2]National University of Singapore, Singapore

11:15 AM

22.7 A Programmable Wireless EEG Monitoring SoC with Open/Closed-Loop Optogenetic and Electrical Stimulation for Epilepsy Control

S-Y. Lee, C. Tsou, P-W. Huang, P-H. Cheng, C-C. Liao, Z-X. Liao, H-Y. Lee, C-C. Lin, C-H. Hsieh
National Cheng Kung University, Tainan, Taiwan

11:45 AM

22.8 Adaptively Clock-Boosted Auto-Ranging Responsive Neurostimulator for Emerging Neuromodulation Applications

M. R. Pazhouhandeh[*1], G. O'Leary*[*1], I. Weisspapir[2], D. Groppe[2], X-T. Nguyen[1], K. Abdelhalim[1,3], H. M. Jafari[1,4], T. A. Valiante[5], P. Carlen[5], N. Verma[6], R. Genov[1]*
[1]University of Toronto, Toronto, Canada; [2]Krembil Neuroscience Center, Toronto, Canada
[3]now at Sitrus Technology, Irvine, CA; [4]now at Envirosen, Toronto, Canada
[5]Toronto Western Hospital, Toronto, Canada; [6]Princeton University, Princeton, NJ
*Equally-Credited Authors (ECAs)

Conclusion 12:15 PM

DRAM

Session Chair: ***Wolfgang Spirkl,*** *Micron Semiconductor Deutschland, Munich, Germany*
Associate Chair: ***Dong Uk Lee,*** *SK hynix, Gyeonggi-do, Korea*

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23.1 A 7.5Gb/s/pin LPDDR5 SDRAM with WCK Clocking and Non-Target ODT for High Speed and with DVFS, Internal Data Copy, and Deep-Sleep Mode for Low Power

K-S. Ha, C-K. Lee, D. Lee, D. Moon, J-H. Jang, H-R. Hwang, H. Chi, J. Park, S. Shin, D. Park, S-Y. Kim, S. Lim, K. Park, Y. Choi, Y-H. Kim, Y. Son, H. Cho, B. Na, H-J. Ahn, S. Lee, S-K. Choi, Y-S. Park, S-H. Hyun, S. Chang, H-J. Kwon, J-H. Choi, T-Y. Oh, Y-S. Sohn, K-I. Park, S-J. Jang
Samsung Electronics, Hwaseong, Korea

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23.2 A 1.1V 1ynm 6.4Gb/s/pin 16Gb DDR5 SDRAM with a Phase-Rotator-Based DLL, High-Speed SerDes and RX/TX Equalization Scheme

D. Kim, M. Park, S. Jang, J-Y. Song, H. Chi, G. Choi, S. Choi, J. Kim, C. Kim, K. Kim, K. Koo, S. Song, Y. Kim, D. U. Lee, J. Lee, D. Kim, K. Kwon, M. Han, B. Choi, H. Kim, S. Ku, Y. Kim, J. Kim, S. Kim, Y. Seo, S. Oh, D. Im, H. Kim, J. Choi, J. Chung, C. Lee, Y. Lee, J-H. Cho, J. Chun, J. Oh
SK hynix, Icheon, Korea

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23.3 A 3-bit/2UI 27Gb/s PAM-3 Single-Ended Transceiver Using One-Tap DFE for Next-Generation Memory Interface

H. Park[1], J. Song[2], Y. Lee[1], J. Sim[1], J. Choi[1], C. Kim[1]
[1]Korea University, Seoul, Korea
[2]Incheon National University, Incheon, Korea

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23.4 A 512GB 1.1V Managed DRAM Solution with 16GB ODP and Media Controller DS2

S. Lee, B. Jeon, K. Kang, D. Ka, N. Kim, Y. Kim, Y. Hong, M. Kang, J. Min, M. Lee, C. Jeong, K. Kim, D. Lee, J. Shin, Y. Han, Y. Shim, Y. Kim, Y. Kim, H. Kim, J. Yun, B. Kim, S. Han, C. Lee, J. Song, H. Song, I. Park, Y. Kim, J. Chun, J. Oh
SK hynix, Icheon, Korea

Break 10:00 AM

SRAM & Computation-in-Memory

Session Chair: ***Shinichiro Shiratake,*** *Toshiba Memory, Yokohama, Japan*
Associate Chair: ***Kyu-hyoun Kim,*** *IBM T.J. Watson, Yorktown Heights, NY*

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24.1 A 1Mb Multibit ReRAM Computing-In-Memory Macro with 14.6ns Parallel MAC Computing Time for CNN-Based AI Edge Processors

C-X. Xue, W-H. Chen, J-S. Liu, J-F. Li, W-Y. Lin, W-E. Lin, J-H. Wang, W-C. Wei, T-W. Chang, T-C. Chang, T-Y. Huang, H-Y. Kao, S-Y. Wei, Y-C. Chiu, C-Y. Lee, C-C. Lo, Y-C. King, C-J. Lin, R-S. Liu, C-C. Hsieh, K-T. Tang, M-F. Chang
National Tsing Hua University, Hsinchu, Taiwan

10:45 AM

24.2 A 7nm 2.1GHz Dual-Port SRAM with WL-RC Optimization and Dummy-Read-Recovery Circuitry to Mitigate Read-Disturb-Write Issue

H. Fujiwara, C-Y. Lin, H-Y. Pan, C-H. Lin, P-Y. Huang, K-C. Lin, J-J. Liaw, Y-H. Chen, H-J. Liao, J. Chang
TSMC, Hsinchu, Taiwan

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24.3 A Voltage and Temperature Tracking SRAM Assist Supporting 740mV Dual-Rail Offset for Low-Power and High-Performance Applications in 7nm EUV FinFET Technology

I. Lee, H. Jeong, S. Baeck, S. Gupta, C. Park, D. Seo, J. Choi, J. Kim, H. Kim, J. Kang, S. Jang, D. Moon, S. Han, T. Kim, J. Lim, Y. Park, H. Hwang, J. Kang, J. Choi, T. Song
Samsung Electronics, Hwaseong, Korea

11:30 AM

24.4 Sandwich-RAM: An Energy-Efficient In-Memory BWN Architecture with Pulse-Width Modulation

J. Yang[1], Y. Kong[1], Z. Wang[2], Y. Liu[1], B. Wang[1], S. Yin[3], L. Shi[1]
[1]Southeast University, Nanjing, China
[2]Boxing Electronics, Nanjing, China
[3]Tsinghua University, Beijing, China

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24.5 A Twin-8T SRAM Computation-In-Memory Macro for Multiple-Bit CNN-Based Machine Learning

X. Si[1,2], J-J. Chen[1], Y-N. Tu[1], W-H. Huang[1], J-H. Wang[1], W-C. Wei[1], S-Y. Wu[1], X. Sun[3], R. Liu[3], S. Yu[4], R-S. Liu[1], C-C. Hsieh[1], K-T. Tang[1], Q. Li[2], M-F. Chang[1]
[1]National Tsing Hua University, Hsinchu, Taiwan
[2]University of Electronic Science and Technology of China, Chengdu, China
[3]Arizona State University, Tempe, AZ
[4]Georgia Institute of Technology, Atlanta, GA

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Circuits Enabling Security

Session Chair: ***Hirofumi Shinohara,*** *Waseda University, Kitakyushu, Japan*
Associate Chair: ***Dennis Sylvester,*** *University of Michigan, Ann Arbor, MI*

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25.1 A 562F² Physically Unclonable Function with a Zero-Overhead Stabilization Scheme

D. Li, K. Yang
Rice University, Houston, TX

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25.2 A Reconfigurable RRAM Physically Unclonable Function Utilizing Post-Process Randomness Source with <6×10⁻⁶ Native Bit Error Rate

Y. Pang[1], B. Gao[1], D. Wu[1], S. Yi[1], Q. Liu[1], W-H. Chen[2], T-W. Chang[2], W-E. Lin[2], X. Sun[3], S. Yu[3], H. Qian[1], M-F. Chang[2], H. Wu[1]
[1]Tsinghua University, Beijing, China
[2]National Tsing Hua University, Hsinchu, Taiwan
[3]Georgia Institute of Technology, Atlanta, GA

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25.3 DS2 A 128b AES Engine with Higher Resistance to Power and Electromagnetic Side-Channel Attacks Enabled by a Security-Aware Integrated All-Digital Low-Dropout Regulator

A. Singh[1], M. Kar[2], S. Mathew[2], A. Rajan[2], V. De[2], S. Mukhopadhyay[1]
[1]Georgia Institute of Technology, Atlanta, GA
[2]Intel, Hillsboro, OR

Break 3:00 PM

Frequency Generation & Interference Mitigation

Session Chair: ***Ramesh Harjani,*** *University of Minnesota, Minneapolis, MN*
Associate Chair: ***Andrea Mazzanti,*** *Università degli Studi di Pavia, Pavia, Italy*

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26.1 A Self-Calibrated 16GHz Subsampling-PLL-Based 30µs Fast Chirp FMCW Modulator with 1.5GHz Bandwidth and 100kHz rms Error

Q. Shi[1], K. Bunsen[2], N. Markulic[1], J. Craninckx[1]
[1]imec, Heverlee, Belgium
[2]Sony Semiconductor Solutions, Atsugi, Japan

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26.2 A 0.08mm² 25.5-to-29.9GHz Multi-Resonant-RLCM-Tank VCO Using a Single-Turn Multi-Tap Inductor and CM-Only Capacitors Achieving 191.6dBc/Hz FoM and 130kHz 1/f³ PN Corner

H. Guo[1], Y. Chen[1], P-I. Mak[1], R. P. Martins[1,2]
[1]University of Macau, Macau, China
[2]Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

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26.3 A 25-to-38GHz, 195dB FoM_T LC QVCO in 65nm LP CMOS Using a 4-Port Dual-Mode Resonator for 5G Radios

A. Bhat, N. Krishnapura
Indian Institute of Technology Madras, Chennai, India

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26.4 A 2.4GHz 65nm CMOS Mixer-First Receiver Using 4-Stage Cascaded Inverter-Based Envelope-Biased LNAs Achieving 66dB In-Band Interference Tolerance and -83dBm Sensitivity

D. Ye[1], R. Xu[1], C-J. R. Shi[1,2]
[1]Fudan University, Shanghai, China
[2]University of Washington, Seattle, WA

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26.5 A 0.1-to-0.2V Transformer-Based Switched-Mode Folded DCO in 22nm FDSOI with Active Step-Down Impedance Achieving 197dBc/Hz Peak FoM and 40MHz/V Frequency Pushing

O. El-Aassar, G. M. Rebeiz
University of California, San Diego, La Jolla, CA

Conclusion 5:15 PM

Energy Harvesting & DC/DC Control Techniques

Session Chair: ***Yuan Gao,*** *Institute of Microelectronics, Singapore*
Associate Chair: ***Chan-Hong Chern,*** *TSMC, Hsinchu, Taiwan*

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27.1 An 84% Peak Efficiency Bipolar-Input Boost/Flyback Hybrid Converter with MPPT and On-Chip Cold Starter for Thermoelectric Energy Harvesting
P. Cao[1], Y. Qian[1], P. Xue[1], D. Lv[2], J. He[2], Z. Hong[1]
[1]Fudan University, Shanghai, China; [2]Analog Devices, Shanghai, China

2:00 PM

27.2 An Adiabatic Sense and Set Rectifier for Improved Maximum-Power-Point Tracking in Piezoelectric Harvesting with 541% Energy Extraction Gain
Y. Peng, D. K. Choo, S. Oh, I. Lee, T. Jang, Y. Kim, J. Lim, D. Blaauw, D. Sylvester
University of Michigan, Ann Arbor, MI

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27.3 A Piezoelectric Energy-Harvesting Interface Using Split-Phase Flipping-Capacitor Rectifier and Capacitor Reuse Multiple-VCR SC DC-DC Achieving 9.3× Energy-Extraction Improvement
Z. Chen[1,2], Y. Jiang[1], M-K. Law[1], P-I. Mak[1], X. Zeng[2], R. P. Martins[1,3]
[1]University of Macau, Macau, China; [2]Fudan University, Shanghai, China
[3]Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

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27.4 DS2 Multi-Beam Shared-Inductor Reconfigurable Voltage/SECE-Mode Piezoelectric Energy Harvesting of Multi-Axial Human Motion
M. Meng[1], A. Ibrahim[1], T. Xue[2], H. G. Yeo[3], D. Wang[1], S. Roundy[2], S. Trolier-McKinstry[1], M. Kiani[1]
[1]Pennsylvania State University, University Park, PA
[2]University of Utah, Salt Lake City, UT
[3]Daegu- Gyeongbuk Institute of Science and Technology, DaeguKorea

Break 3:00 PM

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27.5 A 91%-Efficiency Envelope-Tracking Modulator Using Hysteresis-Controlled Three-Level Switching Regulator and Slew-Rate-Enhanced Linear Amplifier for LTE-80MHz Applications
P. Mahmoudidaryan, D. Mandal, B. Bakkaloglu, S. Kiaei
Arizona State University, Tempe, AZ

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27.6 Background Capacitor-Current-Sensor Calibration of DC-DC Buck Converter with DVS for Accurately Accelerating Load-Transient Response
T-H. Kuo, Y-W. Huang, P-Y. Wang, National Cheng Kung University, Tainan, Taiwan

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27.7 A Synthesizable Digital AOT 4-Phase Buck Voltage Regulator for Digital Systems with 0.0054mm² Controller and 80ns Recovery Time
M. Choi[1,2], C-H. Kye[1], J. Oh[1], M-S. Choo[1], D-K. Jeong[1]
[1]Seoul National University, Seoul, Korea; [2]Samsung Electronics, Hwaseong, Korea

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27.8 Dynamic-Charging Current-Scaling Technique with Dual Accurate Current Control and Temperature Loops with Charging-Current Accuracy up to 99.6% for 1.6× Faster Lithium-Ion Battery Charging
W-T. Lin[1], Z-Y. Lin[1], C-H. Liu[1], C-M. Huang[1], L-C. Chu[1], K-H. Chen[1], Y-H. Lin[2], S-R. Lin[2], T-Y. Tsai[2], H-H. Tsai[1], Y-Z. Juang[1]
[1]National Chiao Tung University, Hsinchu, Taiwan
[2]Realtek Semiconductor, Hsinchu, Taiwan

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Techniques for Low-Power & High-Performance Wireless

Session Chair: ***Danielle Griffith,*** *Texas Instruments, Dallas, TX*
Associate Chair: ***Alan Wong,*** *EnSilica, Abingdon, United Kingdom*

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28.1 A 0.42nW 434MHz -79.1dBm Wake-Up Receiver with a Time-Domain Integrator DS2
V. Mangal, P. R. Kinget, Columbia University, New York, NY

2:00 PM

28.2 A 220µW -85dBm Sensitivity BLE-Compliant Wake-up Receiver Achieving -60dB SIR via Single-Die Multi-Channel FBAR-Based Filtering and a 4-Dimentional Wake-Up Signature
P-H. P. Wang, P. P. Mercier, University of California, San Diego, La Jolla, CA

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28.3 A 606µW mm-Scale Bluetooth Low-Energy Transmitter Using Co-Designed 3.5×3.5mm² Loop Antenna and Transformer-Boost Power Oscillator
Y. Shi, X. Chen, H-S. Kim, D. Blaauw, D. Wentzloff
University of Michigan, Ann Arbor, MI

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28.4 A High-Q Resonant Inductive Link Transmit Modulator/Driver for Enhanced Power and FSK/PSK Data Transfer Using Adaptive-Predictive Phase-Continuous Switching Fractional-Capacitance Tuning
H. Kennedy, R. Bodnar, T. Lee, W. Redman-White
University of Southampton, Southampton, United Kingdom

Break 3:00 PM

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28.5 Non-Magnetic 60GHz SOI CMOS Circulator Based on Loss/Dispersion-Engineered Switched Bandpass Filters
A. Nagulu, H. Krishnaswamy, Columbia University, New York, NY

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28.6 Full-Duplex 2×2 MIMO Circulator-Receiver with High TX Power Handling Exploiting MIMO RF and Shared-Delay Baseband Self-Interference Cancellation
M. Baraani Dastjerdi[1], S. Jain[2], N. Reiskarimian[1], A. Natarajan[2], H. Krishnaswamy[1]
[1]Columbia University, New York, NY; [2]Oregon State University, Corvallis, OR

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28.7 A Wideband Blocker-Tolerant Receiver with High-Q RF-Input Selectivity and <-80dBm LO Leakage
H. Wang, Z. Wang, P. Heydari, University of California, Irvine, CA

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28.8 A 21dBm-OP_{1dB} 20.3%-Efficiency -131.8dBm/Hz-Noise X-band Cartesian-Error-Feedback Transmitter with Fully Integrated Power Amplifier in 65nm CMOS
J. Li[1], Z. Xu[2], Q. J. Gu[1]
[1]University of California, Davis, CA; [2]Zhejiang University, Hangzhou, China

Conclusion 5:15 PM

Quantum & Photonics Technologies

Session Chair: ***Edoardo Charbon,*** *EPFL, Neuchatel, Switzerland*
Associate Chair: ***Pui-In Mak,*** *University of Macau, Macau, China*

1:30 PM

29.1 A 28nm Bulk-CMOS 4-to-8GHz <2mW Cryogenic Pulse Modulator for Scalable Quantum Computing

J. C. Bardin[1,2], E. Jeffrey[2], E. Lucero[2], T. Huang[2], O. Naaman[2], R. Barends[2], T. White[2], M. Giustina[2], D. Sank[2], P. Roushan[2], K. Arya[2], B. Chiaro[3], J. Kelly[2], J. Chen[2], B. Burkett[2], Y. Chen[2], A. Dunsworth[3], A. Fowler[2], B. Foxen[3], C. Gidney[2], R. Graff[2], P. Klimov[2], J. Mutus[2], M. McEwen[3], A. Megrant[2], M. Neeley[2], C. Neill[2], C. Quintana[2], A. Vainsencher[2], H. Neven[4], J. Martinis[2,3]
[1]University of Massachusetts, Amherst, MA; [2]Google, Goleta, CA
[3]University of California, Santa Barbara, CA; [4]Google, Los Angeles, CA

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29.2 A Scalable Quantum Magnetometer in 65nm CMOS with Vector-Field Detection Capability DS2

M. I. Ibrahim, C. Foy, D. R. Englund, R. Han
Massachusetts Institute of Technology, Cambridge, MA

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29.3 A 48GHz 5.6mW Gate-Level-Pipelined Multiplier Using Single-Flux Quantum Logic

I. Nagaoka[1], M. Tanaka[1], K. Inoue[2], A. Fujimaki[1]
[1]Nagoya University, Nagoya, Japan; [2]Kyushu University, Fukuoka, Japan

Break 3:00 PM

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29.4 Ultra-Low-Power Atomic Clock for Satellite Constellation with 2.2×10^{-12} Long-Term Allan Deviation Using Cesium Coherent Population Trapping DS2

H. Zhang[1], H. Herdian[1], A. T. Narayanan[1], A. Shirane[1], M. Suzuki[2], K. Harasaka[2], K. Adachi[2], S. Yanagimachi[3], K. Okada[1]
[1]Tokyo Institute of Technology, Tokyo, Japan; [2]Ricoh, Miyagi, Japan
[3]National Institute of Advanced Industrial Science and Technology, Ibaraki, Japan

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29.5 A Single-Chip Optical Phased Array in a 3D-Integrated Silicon Photonics/65nm CMOS Technology

T. Kim[1], P. Bhargava[1], C. V. Poulton[2], J. Notaros[2], A. Yaacobi[2], E. Timurdogan[2], C. Baiocco[3], N. Fahrenkopf[3], S. Kruger[3], T. Ngai[3], Y. Timalsina[3], M. R. Watts[2], V. Stojanovic[1]
[1]University of California, Berkeley, CA; [2]Massachusetts Institute of Technology, Cambridge, MA
[3]Colleges of Nanoscale Science and Engineering, Albany, NY

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29.6 A Digital-Type GaN Driver with Current-Pulse-Balancer Technique Achieving Sub-Nanosecond Current Pulse Width for High-Resolution and Dynamic Effective Range LiDAR System

Y-S. Ma[1], Z-Y. Lin[1], Y-T. Lin[1], C-Y. Lee[1], T-P. Huang[1], K-H. Chen[1], Y-H. Lin[2], S-R. Lin[2], T-Y. Tsai[2]
[1]National Chiao Tung University, Hsinchu, Taiwan; [2]Realtek Semiconductor, Hsinchu, Taiwan

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29.7 A 500Mb/s -46.1dBm CMOS SPAD Receiver for Laser Diode Visible-Light Communications

J. Kosman[1,2], O. Almer[1], T. Al Abbas[1], N. Dutton[2], R. Walker[3], S. Videv[1], K. Moore[2], H. Haas[1], R. Henderson[1]
[1]University of Edinburgh, Edinburgh, United Kingdom;
[2]STMicroelectronics, Edinburgh, United Kingdom; [3]Photon Force, Edinburgh, United Kingdom

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29.8 SHARC: Self-Healing Analog with RRAM and CNFETs

A. G. Amer, R. Ho, G. Hills, A. P. Chandrakasan, M. M. Shulaker
Massachusetts Institute of Technology, Cambridge, MA

Conclusion 5:15 PM

Advanced Wireline Techniques

Session Chair: ***Yohan Frans,*** *Xilinx, San Jose, CA*
Associate Chair: ***Friedel Gerfers,*** *Technische Universitaet Berlin, Berlin, Germany*

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30.1 Single-Pair Automotive PHY Solutions from 10Mb/s to 10Gb/s and Beyond
G. W. den Besten, NXP Semiconductors, Eindhoven, The Netherlands

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30.2 A 161mW 56Gb/s ADC-Based Discrete Multitone Wireline Receiver Data-Path in 14nm FinFET
G. Kim[1,2,3], L. Kull[2], D. Luu[2,4], M. Braendli[2], C. Menolfi[2], P-A. Francese[2], H. Yueksel[5], C. Aprile[1,2], T. Morf[2], M. Kossel[2], A. Cevrero[2], I. Ozkaya[1,2], A. Burg[1], T. Toifl[2], Y. Leblebici[1]
[1]EPFL, Lausanne, Switzerland; [2]IBM Zurich Research Laboratory, Rueschlikon, Switzerland
[3]*now with KAIST, Daejeon, Korea; [4]ETH Zürich, Zurich, Switzerland
[5]IBM T. J. Watson Research Center, Yorktown Heights, NY

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30.3 A 25.6Gb/s Uplink-Downlink Interface Employing PAM-4-Based 4-Channel Multiplexing and Cascaded CDR Circuits in Ring Topology for High-Bandwidth and Large-Capacity Storage Systems
T. Toi, J. Wadatsumi, H. Kobayashi, Y. Shimizu, Y. Satoh, M. Morimoto, R. Ito, M. Ashida, Y. Tsubouchi, M. Nozawa, G. Urakawa, J. Deguchi
Toshiba Memory, Kawasaki, Japan

Break 3:00 PM

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30.4 A 32Gb/s 2.9pJ/b Transceiver for Sequence-Coded PAM-4 Signalling with 4-to-6dB SNR Gain in 28nm FDSOI CMOS
Aurangozeb[1], C. Dick[1], M. Mohammad[2], M. Hossain[1]
[1]University of Alberta, Edmonton, Canada; [2]Intel, Santa Clara, CA

3:45 PM

30.5 A 1.41pJ/b 56Gb/s PAM-4 Wireline Receiver Employing Enhanced Pattern Utilization CDR and Genetic Adaptation Algorithms in 7nm CMOS
S. Shahramian[1], B. Dehlaghi*[1], J. Liang[1], R. Bespalko[1], D. Dunwell[1], J. Bailey[1], B. Wang[1], A. Sharif-Bakhtiar[1], M. O'Farrell[1], K. Tang[1], A. Chan Carusone[2], D. Cassan[1], D. Tonietto[3]*
[1]Huawei Technologies, Toronto, Canada; [2]University of Toronto, Toronto, Canada
[3]Huawei Technologies, Ottawa, Canada; *Equally-Credited Authors (ECAs)

4:15 PM

30.6 A 6V Swing 3.6% THD >40GHz Driver with 4.5× Bandwidth Extension for a 272Gb/s Dual-Polarization 16-QAM Silicon Photonic Transmitter
A. H. Ahmed[1,2], D. Lim[2], A. Elmoznine[2], Y. Ma[2], T. Huynh[2], C. Williams[2], L. Vera[2], Y. Liu[2], R. Shi[2], M. Streshinsky[2], A. Novack[2], R. Ding[2], R. Younce[2], R. Sukkar[2], J. Roman[2], M. Hochberg[2], S. Shekhar[1], A. Rylyakov[2]
[1]University of British Columbia, Vancouver, Canada; [2]Elenion Technologies, New York, NY

4:30 PM

30.7 An 8b Injection-Locked Phase Rotator with Dynamic Multiphase Injection for 28/56/112Gb/s Serdes Application
Y-C. Huang, B-J. Chen, MediaTek, Hsinchu, Taiwan

4:45 PM

30.8 A 0.65V 12-to-16GHz Sub-Sampling PLL with 56.4fs$_{rms}$ Integrated Jitter and -256.4dB FoM
Z. Zhang, G. Zhu, C. P. Yue; Hong Kong University of Science and Technology, Hong Kong, China

5:00 PM

30.9 A 140fs$_{rms}$-Jitter and -72dBc-Reference-Spur Ring-VCO-Based Injection-Locked Clock Multiplier Using a Background Triple-Point Frequency/Phase/Slope Calibrator
S. Yoo, S. Choi, Y. Lee, T. Seong, Y. Lim, J. Choi
Ulsan National Institute of Science and Technology, Ulsan, Korea

Conclusion 5:15 PM

Short Course: Integrated Phased Arrays: Theory, Practice, and Implementation for 5G and Beyond

Time:	Topic:
8:00 AM	Breakfast
8:20 AM	Introduction by Chair, ***Daniel Friedman*** *IBM Thomas J. Watson Research Center, Yorktown Heights, NY*
8:30 AM	**Introduction to Phased-Array Technology from mm-Wave to Optics** ***Hossein Hashemi,*** *University of Southern California, Los Angeles, CA*
10:00 AM	Break
10:30 AM	**Scalable mm-Wave Phased Arrays for Imaging and 5G Communications** ***Bodhisatwa Sadhu,*** *IBM T. J. Watson Research Center, Yorktown Heights, NY*
12:15 PM	Lunch
1:20 PM	**Challenges and Architectures for Large-Scale Next-Generation Phased Arrays and 5G Systems** ***Shahriar Shahramian,*** *Nokia, Murray Hill, NJ*
2:50 PM	Break
3:20 PM	**Emerging Topics in Phased Arrays and the Path to THz** ***Ehsan Afshari,*** *University of Michigan, Ann Arbor, MI*
4:50 PM	Conclusion

Introduction

Phased array technology is a staple in specialized radar and long reach communications applications. With the rise of mmWave circuits and associated dense packaging, integrated, scalable phased arrays are key technology elements in a new wave of emerging broad-based commercial applications in the communication and imaging spaces. In this short course, we first introduce the concept of electronically steered arrays, describe how to analyze such designs, discuss analog, digital, and hybrid beamforming phased array tradeoffs, and introduce both mmWave and optical examples. We next discuss some of the key circuits enabling these designs, scalability of such designs, and emerging opportunities for systems leveraging these designs. We continue with a discussion of paths to realizing very large scale arrays, including physical design, packaging, verification, and test. Finally, we conclude with a discussion of emerging topics in phased arrays and the opportunities for even higher radio frequency phased array solutions.

8:30 AM

SC1: Introduction to Phased-Array Technology from mm-Wave to Optics

Hossein Hashemi, *University of Southern California, Los Angeles, CA*

This talk will cover the basic principles, architectures, applications, and associated building blocks of phased arrays from radio frequencies up to optical frequencies.

Hossein Hashemi is a Professor of Electrical Engineering at the University of Southern California. His research interests include analog, mixed-signal, radio-frequency and photonic integrated circuits. He received the B.S. and M.S. degrees in Electronics Engineering from the Sharif University of Technology, Tehran, Iran, in 1997 and 1999, respectively, and the M.S. and Ph.D. degrees in Electrical Engineering from the California Institute of Technology, Pasadena, in 2001 and 2003, respectively. Hossein is an Associate Editor for the IEEE Journal of Solid state Circuits. He was a co-recipient of the 2004 IEEE Journal of Solid-State Circuits Best Paper Award and the 2007 IEEE ISSCC Lewis Winner Award for Outstanding Paper.

10:30 AM

SC2: Scalable mm-Wave Phased Arrays for Imaging and 5G Communications

Bodhisatwa Sadhu, *IBM T. J. Watson Research Center, Yorktown Heights, NY*

Large numbers of millimeter-wave antenna elements (typically from 10s to 100s) can be supported using multiple integrated circuits (ICs) that are further integrated at the package level to create a phased-array module. This talk motivates the need for millimeter-wave phased-array scaling to realize such large apertures and outlines key challenges toward their implementation. Various aspects of phased array scaling, including beamforming architectures and functional partitioning, signal distribution among multiple ICs, module-level implementation of antennas and packaging, and digital control will be discussed. Two recently introduced scaled 64-element dual-polarized phased array designs will be reviewed as implementation examples: 1) A phased-array transceiver module operating at 28GHz supporting 5G applications, and 2) TX and RX phased arrays operating at 94GHz, suitable for backhaul and imaging applications. Design techniques implementing requirements relevant to these applications will be discussed, and measurement results validating the designs will be presented. Finally, an emerging approach to managing the rich control space associated with highly integrated phased-array designs will be discussed.

Bodhisatwa Sadhu is currently a Research Staff Member at IBM T. J. Watson Research Center. He received the Ph.D. degree in Electrical Engineering from University of Minnesota, Minneapolis, in 2012, working on cognitive radio circuits. Since 2012, Dr. Sadhu has been working on RF and mm-wave transceivers at IBM T. J. Watson Research, where he has led the design and demonstration of a self-healing frequency synthesizer, a low-power 60GHz transceiver IC, and a mm-wave 5G phased array base-station IC. In the last five years, he has authored and co-authored 10+ journal papers, 20+ conference papers, and a book on cognitive radio circuits, and holds 20 issued US patents with 20+ pending. He is currently an Adjunct Assistant Professor at Columbia University, serves as a TPC member of the IEEE RFIC Symposium and IEEE BCICTS, and a guest editor of IEEE JSSC. Dr. Sadhu is the recipient of the 2017 ISSCC Lewis Winner Award for Outstanding Paper, the 2017 Pat Goldberg Memorial Award for the best paper in computer science, electrical engineering, and mathematics published by IBM Research, two IBM A-level Accomplishment awards, six IBM Patent Plateau Awards, the University of Minnesota Graduate School Fellowship in 2007, the 3M Science and Technology Fellowship in 2009, the University of Minnesota Doctoral Dissertation Fellowship in 2011, and stood 2nd in India in the Indian School Certificate (ISC) examination in 2003. He was recognized as an IBM Master Inventor in 2017.

1:20 PM

SC3: Challenges and Architectures for Large-Scale Next-Generation Phased Arrays and 5G Systems

Shahriar Shahramian, *Nokia, Murray Hill, NJ*

The wireless communications industry is at the verge of an exciting transformation: a shift from broadcast-mode to directed-beam communication in the form of large-scale mm-wave phased arrays. In order to enable mass deployment of phased array systems, every layer of our future networks must undergo a transformation. This workshop discusses the challenges associated with the design and architecture of mm-wave phased-array systems up to and beyond the W-band. The impact of technology, circuit topology and chipset architecture on the overall system is examined alongside state-of-the-art reported communication platforms. Furthermore, packaging, calibration and cost reductions techniques are explored.

Shahriar Shahramian received his Ph.D. degree from University of Toronto in 2010, where he focused on the design of mm-wave data converters and transceivers. Dr. Shahramian has been with the Bell Laboratories division of Alcatel-Lucent (now Nokia), Murray Hill, NJ, since 2009 and is currently the Director of the mm-Wave ASIC Research Department. He is also a member of the technical program committee of the IEEE Compound Semiconductor Integrated Circuits Symposium (CSICS) and the IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS). He is also a guest Editor of the IEEE Journal of Solid-State Circuits (JSSC). His research focus includes the design of mm-wave wireless and wireline integrated circuits. He is the lead designer of several state-of-the-art ASICs for optical coherent and wireless backhaul products at Bell Laboratories.

Dr. Shahramian has been the recipient of Ontario Graduate Scholarship, University of Toronto Fellowship and the Best Paper Award at the CSICS Symposium in 2005, 2015, and the RFIC Symposium in 2015. He also holds an Adjunct Associate Professor position at Columbia University, has received several teaching awards, and is the founder and host of The Signal Path educational video series.

3:20 PM

SC4: Emerging Topics in Phased Arrays and the Path to THz

Ehsan Afshari, *University of Michigan, Ann Arbor, MI*

The design and implementation of phased arrays at mmWave and THz frequencies has several challenges, including loss of passives, phase mismatch, limited efficiency of active devices, and the antenna implementation. In this short course, we demonstrate that as we get closer to the cut-off frequency of transistors, new approaches that combine the device physics, circuit techniques, and EM theory are needed. We will discuss several scalable phased arrays for communication and radar applications.

Ehsan Afshari received his Ph.D. in Electrical Engineering from Caltech in 2006, and joined the ECE Department of Cornell University. Ten years later, he joined the EECS department of the University of Michigan, Ann Arbor. His team is engaged in the theoretical foundations, design and experimental validation of analog, RF, mm-wave, and THz integrated devices, circuits and systems for a variety of applications, including communications, imaging and sensing. His work is funded by federal agencies, such the NSF, DARPA, ONR, and the ARL, as well as companies like Intel, TI, Raytheon, and Qualcomm. He has been the recipient of several awards and honors, including a 2008 DARPA Young Faculty Award, a 2010 NSF CAREER Award, a first place at the Stanford-Berkeley-Caltech Innovation Challenge in 2005, and several best paper awards at the leading conferences in his field. He has also served as a Distinguished Lecturer for the IEEE Solid-State Circuits Society. He was selected as one of the 50 most distinguished alumni of Sharif University. His doctoral students have also received several prestigious awards and fellowships, including: 2018, 2017, 2012, 2011, and 2010 Solid-State Circuit Society Predoctoral Achievement Award; 2011, 2013, and 2017 IEEE MTT-S Microwave Engineering Graduate Fellowships; the Cornell Best Ph.D. Thesis Award in 2011 and 2014; as well as many best paper awards. The Ph.D. graduates of his group are leaders in the field, including faculty members at MIT, UC Davis and the University of Minnesota, and companies such as IBM, Bell Labs, Qualcomm and Broadcom.

F3: The Complete Advanced Driver-Assistance System (ADAS) Sensing Network

Organizer: **Bruce Rae,** *STMicroelectronics, Edinburgh, United Kingdom*

Co-Organizers: **Pedram Lajevardi,** *Robert Bosch, Sunnyvale, CA*
Tim Piessens, *ICsense, Leuven, Belgium*
Gerard Villar Pique, *NXP Semiconductor, Eindhoven, The Netherlands*

Committee: **Chris Van Hoof,** *IMEC, Leuven, Belgium*
Kofi Makinwa, *Delft University of Technology, Delft, The Netherlands*
Yogesh Ramadass, *Texas Instruments, San Jose, CA*

As the automotive industry continues its intensive commercial and R&D drive towards ever more sophisticated advanced driver-assistance systems, the focus on sensor quality, reliability and security has never been greater. Such systems comprise a multi-sensor network and decision engine capable of processing high volumes of data, in real-time to take safety critical, vehicle actions. In this forum, we will review the ADAS system and the requirements of OEMs and system integrators before presentations on state-of-the-art automotive sensors covering CIS, inertial sensors, LiDAR, RADAR and ultrasonics.

Forum Agenda

Time	Topic
8:00 AM	Breakfast
8:20 AM	**Introduction** ***Bruce Rae,*** *STMicroelectronics, Edinburgh, United Kingdom*
8:30 AM	**Overview of ADAS Systems** ***Patrick Denny,*** *Valeo, Galway, Ireland*
9:20 AM	**ADAS - AV Central Processing Hub** ***Richard Bramley,*** *Nvidia, Santa Clara, CA*
10:10 AM	Break
10:30 AM	**Intelligent Sensors for Autonomous Driving** ***Sergey Velichko,*** *ON Semiconductor, Meridian, ID*
11:20 AM	**Achieving High-Performance and Robustness: Technologies for Automotive MEMS Gyroscopes** ***Deyou Fang,*** *STMicroelectronics, Coppell, TX*
12:10 PM	Lunch
1:10 PM	**LiDAR Sensor Systems** ***Ming Wu,*** *UC Berkeley, Berkeley, CA*
2:00 PM	**The Evolving Landscape in Automotive Radars: Waveform, System Implementation, and IC Technologies** ***Cicero Vaucher,*** *NXP Semiconductor, Eindhoven, The Netherlands*
2:50 PM	Break
3:10 PM	**Ultrasonic Sensors and Their Role in ADAS** ***Ajit Sharma,*** *Texas Instruments, Dallas, TX*
4:00 PM	**Battery Management IC Design Complying with Functional Safety** ***Pieter De Muyter,*** *ICsense, Leuven, Belgium*
4:50 PM	Conclusion

F4: Intelligence at the Edge: How Can We Make Machine Learning More Energy Efficient?

Organizer: **Masato Motomura,** *Hokkaido University, Sapporo, Japan*

Committee: **Vivek De,** *Intel, Hilsboro, Oregon*
Long Yan, *Samsung Electronics, Hwaseong, Korea*
Dong Uk Lee, *SK hynix, Icheon, Korea*
Kyu-hyoun Kim, *IBM T. J .Watson, Yoktown Heights, NY*

Deep learning algorithms mainly used today in Machine Learning applications are very costly in terms of energy consumption, due to their large amount of required computations and large model sizes. Many issues like connectivity to the cloud, latency, privacy, and public safety could be resolved by establishing intelligent computing at the edge. This forum brings together architecture, circuit, and integrated design solutions to minimize the energy consumption of edge learning systems. Various approaches from different perspectives will be covered: neuro-inspired architectures, in memory computation, embedded sensing, and spiking neural networks.

Forum Agenda

Time	Topic
8:00 AM	Breakfast
8:20 AM	**Introduction** ***Masato Motomura,*** Hokkaido University, Sapporo, Japan
8:30 AM	**Enabling Embedded Intelligence: Application, Architecture and Design Solutions** ***Bert Moons,*** *Synopsys, Leuven, Belgium*
9:20 AM	**Mixed-Signal Circuits for Inference at the Edge** ***Daniel Bankman,*** *Stanford University, Stanford, CA*
10:10 AM	Break
10:30 AM	**Processing Data Where It Makes Sense in Modern Computing Systems: Enabling In-Memory Computation** ***Onur Mutlu,*** ETH Zurich, Zurich, Switzerland
11:20 AM	**Bandwidth-Efficient Deep Learning with Algorithm and Hardware Co-Design** ***Song Han,*** *Massachusetts Institute of Technology, Cambridge, MA*
12:10 PM	Lunch
1:10 PM	**On-Chip Epilepsy Detection: Where Machine Learning Enables Patient-Specific Pervasive Healthcare** ***Jerald Yoo,*** *National University of Singapore, Singapore*
2:00 PM	**Applying Principles of Neural Computation for Efficient Learning in Silicon** ***Mike Davies,*** *Intel Labs, Hillsboro, OR*
2:50 PM	Break
3:10 PM	**Energy-Efficient Deep Learning for Intelligent Embedded Systems** ***Nitin Chawla,*** *ST Microelectronics, Greater Noida, India*
4:00 PM	**Energy-Efficient Intelligent Vision Sensor for Next Generation Mobile and Autonomous Applications** ***Eric Ryu,*** *Samsung Electronics, Hwasung, Korea*
4:50 PM	Conclusion

F5: 56Gb/s to 112Gb/s and Beyond – Design Challenges and Solutions in Wireline Communications

Organizer: **Andrew Joy,** *Cavium, Northampton, United Kingdom*

Committee: **Amir Amirkhany,** *Samsung, San Jose, CA*
Mounir Meghelli, *IBM, Yorktown Heights, NY*
Samuel Palermo, *Texas A&M University, College Station, TX*
Hyeon-min Bae, *KAIST, Daejong, Korea*
Takayuki Shibasaki, *Fujitsu Laboratories, Kanagawa, Japan*

This forum brings together experts from the forefront of all areas in the design of high-speed wireline SerDes. The talks will take you through a detailed review of current and next generation serial link designs and the associated challenges in each area, as well as where the industry and roadmap maybe heading beyond 112Gb/s.

The forum is a circuit- and algorithm-oriented review of high-performance tranceivers, focussing on all aspects of SerDes design including analog front-end circuits, high-speed ADC design for receivers, high-speed DAC design for transmitters, clock-and-data recovery techniques, wide-range PLLs and clocking, and adaptive equalization. Talks include the Forward Error Correction techniques that are essential for the future and those that are currently employed, as well as the error statistics and how solutions can be tailored around them. Short-reach links and their challenges are included, as well as longer-reach backplane links, together with the modeling techniques used with IBIS AMI for the verification of how well they will operate in practise. Finally, some non-standard techniques are also discussed to solving the bandwidth limitation problem.

Forum Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Introduction, *Andrew Joy,*** *Cavium, Northampton, United Kingdom*
8:20 AM	**Signaling Techniques and Trends for 56+Gb/s Electrical Links** ***Brian Ji,*** *Avera Semi, Hopewell Junction, New York*
9:05 AM	**ADCs for High-Speed Communication - Architectures and Circuit Implementations** ***Filip Tavernier,*** *KU Leuven, Leuven, Belgium*
9:50 AM	Break
10:00 AM	**Design Techniques for a 112Gb/s PAM-4 Transmitter** ***Jihwan Kim,*** *Intel, Hillsboro, OR*
10:45 AM	**Equalization Techniques/Trends for 56+Gb/s and the Efficacy of Forward Error Correction, *Cathy Liu,*** *Broadcom,San Jose, CA*
11:30 AM	**High-Speed Clock and Data Recovery Circuit: Architecture, Modeling, Specifications, and Consideration** ***Jri Lee,*** *National Taiwan University, Taiwan*
12:15 PM	Lunch
1:30 PM	**Challenges and Solutions for High-Bandwidth Density, Energy-Efficient, Short-Reach Signaling that Enables Massively Scalable Parallelism** ***John Wilson,*** *Nvidia, Durham, NC*
2:15 PM	**Clock Generation and Distribution for 56Gb/s, 112Gb/s and Beyond Serial Links, *Didem Turker,*** *Xilinx, San Jose, CA*
3:00 PM	Break
3:15 PM	**Link Modelling and the Challenges and Limitations for IBIS AMI for 56+Gb/s in Matching Circuit Performance** ***Mike Steinberger,*** *Signal Integrity Software, Chippewa Falls, WI*
4:00 PM	**Non-Differential Techniques: Multi-Wire Multi-Level I/O** ***Armin Tajalli,*** *University of Utah, Salt Lake City, Utah*
4:45 PM	Conclusion

F6: The Right Tool for the Job: Application-Optimized Data Converters

Organizers: **Kostas Doris,** *NXP Semiconductors, Eindhoven, The Netherlands*
Seng-Pan (Ben) U, *University of Macau and Synopsys Macau, Macau*
Jan Westra, *Broadcom, Bunnik, The Netherlands*

Committee: **Yiannos Manoli,** *University of Freiburg - IMTEK, Germany*
David Robertson, *Analog Devices, Wilmington, MA*
Michael Flynn, *University of Michigan, Ann Arbor, MI*

Moderator: **David Robertson,** *Analog Devices, Wilmington, MA*

Conditioning the data converter function to the properties of evolving CMOS technologies through architectural, algorithmic and circuit innovation enabled the last decades making radical steps in accuracy, speed and power efficiency. In analogy to this, optimizing the data converter for the unique requirements of emerging applications such as 5G mobile, biomedical and IoT, imaging, automotive radars and wireline communications offers the designer new degrees of freedom to improve performance and power efficiency of the data converter.

This forum addresses the unique challenges of application-specific data converters and presents the best tradeoffs and optimum architectures for each application.

Forum Agenda

Time	Topic
8:00 AM	Breakfast
8:20 AM	**Introduction** ***Kostas Doris,*** *NXP Semiconductors, Eindhoven, The Netherlands*
8:30 AM	**Application-Optimized Data Converters: An Introduction** ***Boris Murmann,*** *Stanford University, Pallo Alto, CA*
9:20 AM	**ADCs for Biomedical and IoT Applications** ***Chih-Cheng Hsieh,*** *National Tsing Hua University, Hsinchu, Taiwan*
10:10 AM	Break
10:30 AM	**Filtering Delta-Sigma ADCs for Mobile Receivers** ***Maurits Ortmanns,*** *University of Ulm, Ulm, Germany*
11:20 AM	**Data Converter Design Considerations for Mobile Transceivers: Benchmark and Trends from 4G LTE to 5G NR** ***Tien-Yu Lo,*** Tien-Yu Lo, *MediaTek, Hsinchu, Taiwan*
12:10 PM	Lunch
1:10 PM	**Analog-to-Digital Conversion for Imaging, from 2-D to Lidar** ***Ron Kapusta,*** *Analog Devices, Wilmington, MA*
2:00 PM	**Analog-to-Digital Converters for Automotive Radar** ***Erwin Janssen,*** *NXP Semiconductors, Eindhoven, The Netherlands*
2:50 PM	Break
3:10 PM	**Multi-GS/s Data Converters for High-Speed Wireline and Optical Links** ***Jun Cao,*** *Broadcom, Irvine, CA*
4:00 PM	**Panel Discussion - All speakers** **Moderator:** ***David Robertson,*** *Analog Devices, Wilmington, MA*
4:50 PM	Closing Remarks

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HOW TO REGISTER FOR ISSCC

Online: This is the fastest, most convenient way to register and will give you immediate email confirmation of your events. To register online (which requires a credit card), go to the ISSCC website at www.isscc.org and select the link to the registration website.

FAX, mail or email: Use the "2019 IEEE ISSCC Registration Form" which can be downloaded from the registration website. All payments must be made in U.S. Dollars, by credit card or check. Checks must be made payable to "ISSCC 2019". It will take several days before you receive email confirmation when you register using the form. **Registration forms received without full payment will not be processed until payment is received at YesEvents.** Please read the descriptions and instructions on the back of the form carefully.

On site: The On-site Registration and Advance Registration Pickup Desks at ISSCC 2019 will be located in the Yerba Buena Ballroom Foyer at the San Francisco Marriott Marquis. All participants, except as noted below, should register or pick up their registration materials at these desks as soon as possible. **Pre-registered Presenting Authors and pre-registered members of the ISSCC Program and Executive Committees must go to the Nob Hill Room, Ballroom level, to collect their conference materials.**

REGISTRATION DESK HOURS:

Saturday,	February 16	4:00 pm to 7:00 pm
Sunday,	February 17	7:00 am to 8:30 pm
Monday,	February 18	6:30 am to 3:00 pm
Tuesday,	February 19	8:00 am to 3:00 pm
Wednesday,	February 20	8:00 am to 3:00 pm
Thursday,	February 21	7:00 am to 2:00 pm

Students must present their Student ID at the Registration Desk to receive the student rates. Those registering at the IEEE Member rate must provide their IEEE Membership number.

Deadlines: The deadline for registering at the Early Registration rates is 11:59 pm Pacific Time **Tuesday January 8, 2019.** After January 8th, and on or before 11:59 pm Pacific Time **Sunday January 27, 2019**, registrations will be processed **at the Late Registration rates. After January 27th, you must register at the on-site rates.** You are urged to register early to obtain the lowest rates and ensure your participation in all aspects of ISSCC.

Cancellations/Adjustments/Substitutions: Prior to 11:59 pm Pacific Time **Sunday January 27, 2019,** conference registration can be cancelled. Fees paid will be refunded (less a processing fee of $75). Send an email to the registration contractor at ISSCCinfo@yesevents.com to cancel or make other adjustments. **No refunds will be made after 11:59 pm Pacific Time January 27, 2019.** Paid registrants who do not attend the conference will be sent all relevant conference materials. Transfer of registration to someone else is allowed with **WRITTEN** permission from the original registrant.

IEEE Membership Saves on ISSCC Registration

Take advantage of reduced ISSCC fees by joining the Solid-State Circuits Society today, or by using your IEEE membership number. If you're an IEEE member and have forgotten your member number, simply phone IEEE at 1(800) 678-4333 and ask. IEEE membership staff will take about two minutes to look up your number for you. If you come to register on site without your membership card, you can phone IEEE then, too. Or you can request a membership number look-up by email by using the online form at: www.ieee.org/about/help/member_support.html. If you're not an IEEE member, consider joining before you register to save on your fees. Join online at www.ieee.org/join any time and you'll receive your member number by email. If you join IEEE at the conference, you can also select a free Society membership. This offer is not available to existing IEEE members.

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This year, SSCS members will again receive an exclusive benefit of a $30 discount on the registration fee for ISSCC in addition to the IEEE discount. Also, the SSCS will again reward our members with a $10 Starbucks gift card when they attend the Conference as an SSCS member in good standing.

Join or renew your membership with IEEE's Solid-State Circuits Society today at sscs.ieee.org – you will not want to miss out on the opportunities and benefits your membership will provide now and throughout your career.

ITEMS INCLUDED IN REGISTRATION

Technical Sessions: Registration includes admission to all technical and evening sessions starting Sunday evening and continuing throughout Monday, Tuesday and Wednesday. ISSCC does not offer partial conference registrations.

Technical Book Display: Several technical publishers will have collections of professional books and textbooks for sale during the Conference. The Book Display will be open on Monday from Noon to 7:00 pm; on Tuesday from 10:00 am to 7:00 pm; and on Wednesday from 10:00 am to 3:00 pm.

Demonstration Sessions: Hardware demonstrations will support selected papers on Monday and Tuesday evenings.

Author Interviews: Author Interviews will be held Monday, Tuesday and Wednesday evenings. Authors from each day's papers will be available to discuss their work.

Social Hour: Social Hour refreshments will be available starting at 5:15 pm.

University Events: Several universities are planning social events during the Conference. Check the University Events display at the conference for the list of universities, locations and times of these events.

ISSCC Lunch Bag: An insulated lunch bag will be given to all Conference registrants.

Publications: Conference registration includes:

-The **Digest of Technical Papers** in hard copy and by download. The Digest book will be distributed beginning on Sunday at 10:00 am.

-**Papers Visuals:** The visuals from all papers presented will be available by download.

-**Demonstration Session Guidebook:** A descriptive guide to the Demonstration Session will be available by download.

-**Note:** Instructions will be provided for access to all downloads. Downloads will be available both during the Conference and for a limited time afterwards.

OPTIONAL EVENTS

Educational Events: Many educational events are available at ISSCC for an additional fee. There are ten 90-minute Tutorials and two all-day Forums on Sunday. There are four additional all-day Forums on Thursday as well as an all-day Short Course. All events include a course handout in color. The Forums and Short Course include breakfast, lunch and break refreshments. The Tutorials include break refreshments. See the schedule for details of the topics and times. A "Thursday All-Access Pass" is available that provides access to all Thursday educational events and a copy of each course handout. Pick just the speakers you want to hear!

OPTIONAL PUBLICATIONS

ISSCC 2019 Publications: The following ISSCC 2019 publications can be purchased in advance or on site:

2019 ISSCC Download USB: All of the downloads included in conference registration **(mailed in March).**

2019 Tutorials USB: All of the 90 minute Tutorials **(mailed in June).**

2019 Short Course USB: "Hardware Approaches to Machine Learning and Inference" **(mailed in June)**.

The Short Course and Tutorial USBs contain audio and written English transcripts synchronized with the presentation visuals. In addition, the USBs contain a pdf file of the presentations and pdf files of key reference material.

Earlier ISSCC Publications: Selected publications from earlier conferences can be purchased. There are several ways to purchase this material:

-Items listed on the registration form can be purchased with registration and picked up at the conference.

-Visit the ISSCC Publications Desk. This desk is located in the registration area and has the same hours as conference registration. With payment by cash, check or credit card, you can purchase materials at this desk. See the posted list at the Conference for titles and prices.

-Visit the ISSCC website at www.isscc.org and click on the link "About/Shop ISSCC/Shop Now" where you can order online or download an order form to mail, email or fax. For a small shipping fee, this material will be sent to you immediately and you will not have to wait until you attend the Conference to get it.

HOW TO MAKE HOTEL RESERVATIONS

Online: ISSCC participants are urged to make their hotel reservations at the San Francisco Marriott Marquis online. Go to the conference website and click on the Hotel Reservation link. **Conference room rates are $279 for a single/double, $304 for a triple and $329 for a quad** (per night plus tax). In addition, ISSCC attendees booked in the ISSCC group receive **in-room Internet access for free**. All online reservations require the use of a credit card. Online reservations are confirmed immediately. You should print the page containing your confirmation number and reservation details and bring it with you when you travel to ISSCC.

Telephone: Call 877-622-3056 (US) or 415-896-1600 and ask for "Reservations." When making your reservation, identify the group as ISSCC 2019 to get the group rate.

Hotel Deadline: Reservations must be received at the San Francisco Marriott Marquis no later than 5 pm Pacific Time January 28, 2019 to obtain the special ISSCC rates. A limited number of rooms are available at these rates. **Once this limit is reached or after January 28th the group rates may no longer be available and reservations will be filled at the best available rate.** Changes: Before the hotel deadline, your reservation can be changed by calling the telephone numbers above. After the hotel deadline, call the Marriott Marquis at 415-896-1600 (ask for "Reservations"). Have your hotel confirmation number ready.

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ISSCC Email:	ISSCC@ieee.org
Registration questions:	ISSCCinfo@yesevents.com
Hotel Information:	San Francisco Marriott Marquis 780 Mission Street San Francisco, CA 94103 Phone: 415-896-1600
Press Information:	Kenneth C. Smith University of Toronto Email: lcfujino@aol.com Phone: 416-418-3034
Registration:	YesEvents 1700 Reisterstown Road #236 Baltimore, MD 21208 Email: issccinfo@yesevents.com Phone: 410-559-2200 or 800-937-8728 Fax: 410-559-2217

Hotel Transportation: Visit the ISSCC website "Registration/Transportation from Airport" page for helpful travel information and links. You can get a map and driving directions from the hotel website at:

www.marriott.com/hotels/travel/sfodt-san-francisco-marriott-marquis/

Next ISSCC Dates and Location:
ISSCC 2020 will be held on February 16-20, 2020
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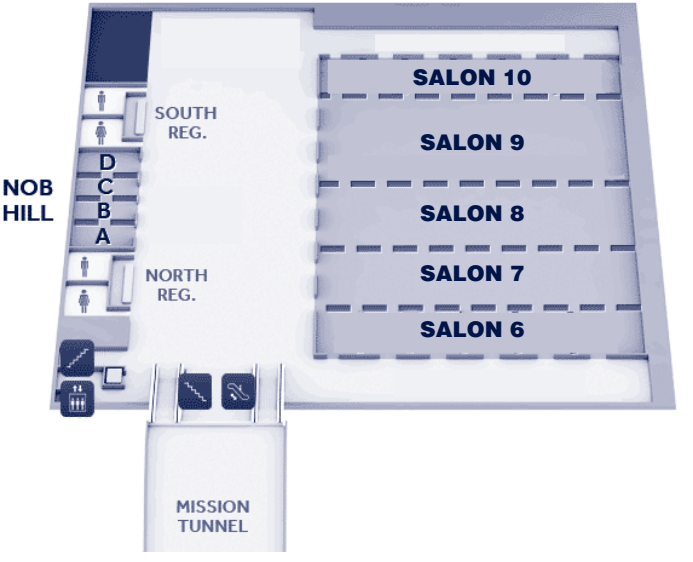
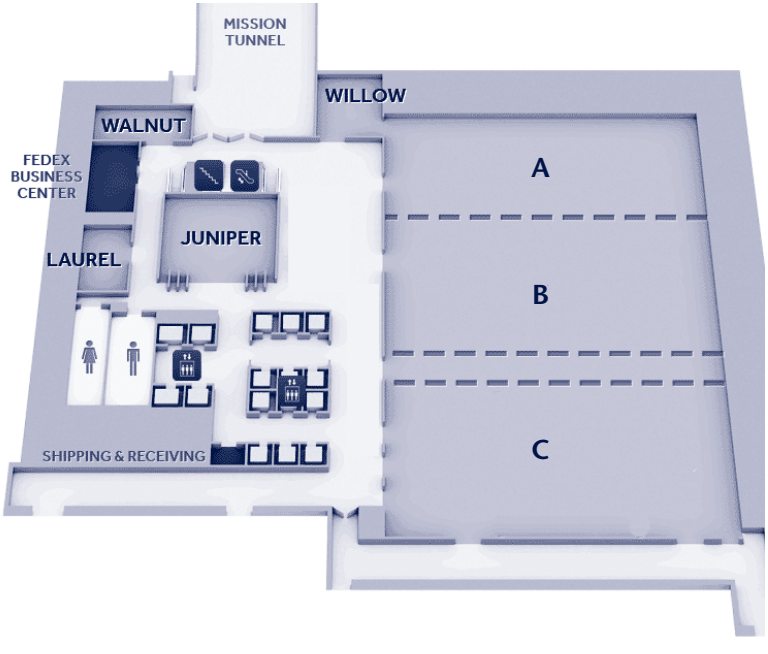
Lower B2 Level - Yerba Buena Ballroom



B2 Level - Golden Gate Hall



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