IEEE SOLID-STATE CIRCUITS SOCIETY

2019 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE
FEBRUARY 17, 18, 19, 20, 21
SAN FRANCISCO, MARRIOTT MARQUIS HOTEL

CONFERENCE THEME: ENVISIONING THE FUTURE

THURSDAY ALL-DAY: 4 FORUMS: COMPLETE ADAS SENSING NETWORK; POWER EFFICIENCY OF ML; WIRELINE FROM 56 TO 112G/s; APPLICATION-OPTIMIZED DATA CONVERTERS
SHORT-COURSE: INTEGRATED PHASED ARRAYS

SUNDAY ALL-DAY: 2 FORUMS: 5G SUB-6GHz Radio; MEMORY-CENTRIC COMPUTING
10 TUTORIALS: INTEGRATED RADARS; POWER-CONVERSION TOPOLOGIES; ADVANCED IN-MEMORY COMPUTING; EFFICIENT IoT MICROCONTROLLERS; NOISE-SHAPING IN DATA CONVERTERS; CLOCK- & DATA-RECOVERY CIRCUITS; ASICs FOR HARDWARE SECURITY; CURRENT-SENSING TECHNIQUES; CALIBRATION OF WIRELESS TRANSCIEVERS; LOW-NOISE SENSOR INTERFACES
2 EVENING EVENTS: GRADUATE STUDENT RESEARCH IN PROGRESS; WIC: "HOW TO SAVE LIVES WITH CIRCUITS"

NEW THIS YEAR!
INDUSTRY SHOWCASE: Featuring Future Industrial Products
STUDENT EVENT: Making a Career Choice

ADVANCE PROGRAM
ISSCC VISION STATEMENT
The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and application to maintain technical currency, and to network with leading experts.

CONFERENCE TECHNICAL HIGHLIGHTS
On Sunday, February 17th, the day before the official opening of the Conference, ISSCC 2019 offers:

• A choice of up to 4 of a total of 10 Tutorials, or
• A choice of 1 of 2 all-day Advanced-Circuit-Design Forums

The 90-minute tutorials offer background information and a review of the basics in specific circuit- and system-design topics. In the all-day Advanced-Circuit-Design Forums, leading experts present state-of-the-art design strategies in a workshop-like format. The Forums are targeted at designers experienced in the technical field.

On Sunday evening, there are two events: A WiC Workshop on “How to Save Lives with Circuits” will be offered starting at 6:00 pm. In addition, the Student-Research Preview, featuring 20 ninety-second introductory presentations followed by a poster session from selected graduate-student researchers from around the world will begin at 7:30 pm. Introductory remarks at the Preview will be provided by a distinguished member of the solid-state circuit community, Marian Verhelst, Professor, KU Leuven.

On Monday, February 18th, ISSCC 2019 at 8:30 am offers four plenary papers on the theme: “Envisioning the Future”. On Monday at 1:30 pm, there begin five parallel technical sessions, followed by a Social Hour at 5:15 pm open to all ISSCC attendees. The Social Hour, held in conjunction with Book Displays and Author Interviews, will also include a Demonstration Session, featuring posters and live demonstrations of selected papers from industry and academia. On Monday evening there are two separate events: At 7:00 pm Student Event: “Making a Career Choice”, in which panelists from diverse areas present brief remarks followed by a Q&A session. At 8:00 pm “Industry Showcase”, consisting of an introductory commentary followed by brief presentations by industrial contributors and subsequently an opportunity to participate in their demonstrations.

On Tuesday, February 19th, there are five parallel technical sessions, both morning and afternoon. A Social Hour open to all ISSCC attendees will follow. The Social Hour, held in conjunction with Book Displays and Author Interviews, will also include a second Demonstration Session. Tuesday evening includes two events, entitled “Moving to ‘The Dark Side’!” and “How Can Hardware Designers Reclaim the Spotlight?”.

On Wednesday, February 20th, there will be five parallel technical sessions, both morning and afternoon, followed by Author Interviews.

On Thursday, February 21st, ISSCC offers a choice of five all-day events:

• A Short Course entitled: “Integrated Phased Arrays: Theory, Practice, & Implementation for 5G & Beyond”
• Four Advanced-Circuit-Design Forums entitled:
  “The Complete ADAS Sensing Network”
  “Intelligence at the Edge: How Can we Make Machine Learning More Energy Efficient”
  “56Gs/s to 112Gb/s & Beyond — Design Challenges & Solutions in Wireline Communications”
  “The Right Tool for the Job: Application-Optimized Data Converters”

This year, for the second time, there is an option which allows an attendee to sample parts of all 5 Thursday offerings. Registration for educational events on Sunday and Thursday will be filled on a first-come first-served basis. Use of the ISSCC Web-Registration Site (http://www.isscc.org) is strongly encouraged. Registrants will be provided with immediate confirmation on registration for the Conference, Tutorials, Forums, and the Short Course.
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TUTORIALS Sunday February 17th, 8:30 AM

There are a total of 10 tutorials this year on 10 different topics. Each tutorial, selected through a competitive process within each subcommittee of the ISSCC, presents the basic concepts and working principles of a single topic. These tutorials are intended for non-experts, graduate students and practicing engineers who wish to explore and understand a new topic.

Ali Sheikholeslam
ISSCC Education Chair

8:30 AM

T1: Fundamentals of Integrated Radars
Brian Ginsburg, Texas Instruments, Dallas, TX

Radar is essential to modern aviation, meteorology, and automobiles, among others. This tutorial will cover the basic radar parameters including resolution, accuracy, and maximum range, and show how those are linked to fundamental system specifications. Modern highly integrated radars primarily use continuous-wave modulations, including FMCW and PMCW. High-level architectures and key circuits for a mm-wave implementation will be presented, along with a look at detection signal processing.

Brian Ginsburg received his S.B., M.Eng., and Ph.D. degrees from the Massachusetts Institute of Technology. He joined Texas Instruments, Dallas, Texas in 2007 working in its wireless terminals business unit and Kilby research labs. He is the systems manager of TI’s Radar and Analytics Processors organization, developing mm-wave sensors for automotive and industrial applications. He serves on the ISSCC and VLSI Circuits Symposium Technical Program Committees.

8:30 AM

T2: Fundamentals of Power-Conversion Topologies
Robert Pilawa-Podgurski, UC Berkeley, Berkeley, CA

This tutorial will provide an overview of various power-converter topologies, with a focus on techniques to achieve high-efficiency and high-power density. A brief summary of common power converters, such as buck, boost, single-input multiple-output (SIMO) and multi-phase converters will be presented followed by a detailed analysis and comparison to more recent topologies, such as switched-capacitor (SC) power converters, hybrid and resonant SC converters, and multi-level converters.

Robert Pilawa-Podgurski is currently an Associate Professor in the Electrical Engineering and Computer Sciences Department at the University of California, Berkeley. He received his B.S., M.Eng., and Ph.D. degrees from MIT. He performs research in the area of power electronics. Dr. Pilawa-Podgurski received the Google Faculty Research Award in 2013, and the 2014 Richard M. Bass Outstanding Young Power Electronics Engineer Award of the IEEE Power Electronics Society, given annually to one individual for outstanding contributions to the field of power electronics before the age of 35. He is co-author of nine IEEE prize papers.

8:30 AM

T3: Advances and Prospects for In-Memory Computing
Naveen Verma, Princeton University, Princeton, NJ

As applications become more data centric, the cost of accessing data from memory dominates energy and throughput. An emerging paradigm to address this is in-memory computing. Early approaches show the potential to reduce energy-delay product (EDP) by 2-to-3 orders of magnitude. However, architectures for enabling computation within the constrained structure of memory raise new challenges and opportunities. This tutorial will map out advances in these areas and examine recent demonstrations.

Naveen Verma received the B.A.Sc. degree in Electrical and Computer Engineering from the UBC, Vancouver, Canada, in 2003, and the M.S. and Ph.D. degrees in Electrical Engineering from MIT in 2005 and 2009, respectively. Since July 2009, he has been with the Department of Electrical Engineering at Princeton, where he is currently an Associate Professor. His research focuses on advanced sensing systems and on exploring how systems for learning, inference, and action planning can be enhanced by algorithms that exploit new sensing and computing technologies. This includes research on large-area, flexible sensors, energy-efficient statistical-computing architectures and circuits, and machine-learning and statistical-signal-processing algorithms.
T4: Fundamentals of Efficient IoT Microcontrollers

James Myers, ARM, Cambridge, United Kingdom

IoT microcontrollers are complex constrained SoCs with analog peripherals, DCDC converters, CPUs, accelerators, volatile/non-volatile memories, and radios—all well represented at ISSCC.

However, state-of-the-art circuits do not automatically translate to a state-of-the-art system. This tutorial presents an overview of system components and their system efficiency considerations, using published systems as examples. Future trends, such as battery-free energy harvesting, will also be covered.

James Myers leads the Devices, Circuits and Systems team within Arm Research, which seeks to push compute to the furthest extremes of cost, efficiency, performance, and integration. He joined Arm in 2007 initially responsible for reference implementation flows for the whole processor family. Joining R&D full time from 2009, he has since focused on deployable techniques for reduction of CPU and SoC power, embodied across more than a dozen tapeouts. James holds 20 granted and 16 pending US patents, co-authored one book chapter, and has presented at ISSCC and VLSI Circuits Symposium. His current interests include energy harvesting, printed electronics, sub-threshold circuits, and better-than-worst-case design.

T5: Noise-Shaping in Data Converters

Venkatesh Srinivasan, Texas Instruments, Dallas, TX

Noise shaping is a powerful technique that helps improve the overall accuracy of a data converter. While this technique is widely used in the context of $\Delta\Sigma$ modulators, noise shaping is also gaining popularity in other kinds of converters such as SARs. This tutorial will present the fundamentals of noise shaping along with the architectural view of their application in different data converters such as $\Delta\Sigma$ modulators and SARs. Circuit implementation of key building blocks along with challenges in realization and their mitigation strategies will be discussed as well.

Venkatesh Srinivasan received his B.E (Hons) in Electrical and Electronic Engineering from Birla Institute of Technology and Science, Pilani, India in 1999 and his M.S and Ph.D. degrees in Electrical and Computer Engineering from the University of Tennessee, Knoxville and Georgia Institute of Technology, Atlanta in 2002 and 2006 respectively. Since 2006, he has been with Texas Instruments leading the architecture, design and development of multiple RF, Analog and high-speed $\Delta\Sigma$ modulators for wireless transceivers. He is the author/co-author of 27 publications in IEEE Journals and Conferences and has been issued 14 US patents. He is the recipient of the Best Student Paper Award from IEEE CICC in 2005. He currently serves on the Technical Program Committee of ISSCC.
The choice of the clock-and-data-recovery (CDR) architecture in serial links dictates many of the block-level circuit specs. In the first half of this tutorial we will discuss the basics of CDR operation, CDR main performance metrics, and the relationship between circuit-level parameters and system-level performance metrics. In the second half, we will review various CDR architectures and their associated design trade-offs. We will conclude with the review of a few practical CDR design considerations.

Amir Amirkhany is a Director of Engineering at Samsung Display America Lab, San Jose, CA. He received his B.S. from Sharif University of Technology, M.S. from University of California, Los Angeles, and Ph.D. from Stanford University, all in Electrical Engineering. At Samsung Electronics, Dr. Amirkhany is in charge of the development of future generations of high-speed interfaces for Samsung displays. Prior to Samsung, he was an engineering manager at Rambus Inc., where he led the development of DDR and proprietary high-speed memory interfaces. Dr. Amirkhany has authored or co-authored over 25 IEEE conference and journal papers, including a best paper award, and has over 50 issued US patents.

Massimo Alioto directs the Integrated Circuits and Embedded Systems area, and leads the Green IC group at the National University of Singapore. He held visiting positions at the University of California Berkeley (BWRC), University of Michigan Ann Arbor, Intel Labs, EPFL, and positions at the University of Siena. He is author of 250+ publications and three books, focusing on ultra-low power integrated system design, widely energy-scalable circuits, and hardware security, among others. He is Editor in Chief of IEEE Transactions on VLSI Systems, and was Deputy Editor in Chief of IEEE JETCAS, Guest Editor of various IEEE journal special issues, Program Chair of several IEEE conferences, and an IEEE Distinguished Lecturer. He is an IEEE Fellow.
1:30 PM

**T8: Current-Sensing Techniques**  
*Mahdi Kashmiri, Robert Bosch, Sunnyvale, CA*

Current-sensing is an essential part of a wide range of applications from hand-held products to the electro-mobility drivetrains. The state of charge in a battery and the control of an electromotor or a power converter have specific demands for dynamic-range, precision, speed, isolation, size, and cost. This tutorial provides an overview of the principles of operation and readout techniques for the two current-sensing approaches: Contacted (shunt-based) and contactless (Hall, fluxgate, transformer, AMR/GMR based).

**Mahdi Kashmiri** received his B.Sc. from Tehran University and his M.Sc. and Ph.D. in Microelectronics from Delft University of Technology, Delft, The Netherlands. From 2010 to 2016 he was with Texas Instruments Inc. in Delft and Santa Clara locations, where he worked on precision products including AFEs for low-power ECG, shunt-based current and voltage monitor, contactless current sensor based on integrated Fluxgate and automotive and industrial ultrasound. Since 2016 he has been with the Mixed-signal ASICs group of Robert Bosch Research and Technology Center in Sunnyvale, CA, where he works on ASICs for automotive Lidar. He received the ESSCIRC 2009 Young Scientist Award and is an ISSCC member of the Analog technical program committee.

3:30 PM

**T9: Calibration Techniques for Wireless Transceivers**  
*David McLaurin, Analog Devices, Raleigh, NC*

Modern wireless transceivers are expected to meet aggressive performance, cost, and power consumption targets with adequate yield in short design cycles. To address these challenges, RFICs are relying extensively on calibration techniques. This tutorial presents the impact of analog/RF non-idealities on key radio metrics and will cover techniques to address topics such as IQ imbalance, LO feed-through, IIP2 nonlinearities, analog filter tuning, full duplex radio and phased array calibrations.

**David McLaurin** joined Analog Devices in 2000, designing high speed pipeline ADCs. In 2002 he joined an RF IC team in Raleigh, NC, where he architects and designs wideband reconfigurable wireless transceivers. David graduated from the Georgia Institute of Technology (MSEE 2000), and North Carolina State University (BSEE 1998). He has been serving as a member of the technical program committee of ISSCC since 2016.

3:30 PM

**T10: Low-Noise Sensor Interfaces**  
*Pedram Lajevardi, Robert Bosch, Sunnyvale, CA*

Applications, such as autonomous driving, rely on the perception of the environment around us based on extensive sensing. While most signals in the nature are not changing quickly and can be captured with relatively low-bandwidth sensors, most require low-noise sensors. This tutorial goes over the main sources of noise with a focus on capacitive and image sensors. Advanced noise-reduction circuit techniques, such as chopping, correlated-double sampling, and Boxcar sampling, are explained.

**Pedram Lajevardi** received B.A.Sc. degree in Electrical and Computer Engineering from the University of British Columbia and MS and Ph.D. in Electrical Engineering from Stanford University. He joined Bosch Research and Technology Center, Sunnyvale, CA in 2012 working on CMOS image sensors. Since 2015 he has been serving as a member of the technical program committee of ISSCC. His research interests are low-power and high-precision sensor interfaces.
The next-generation cellular (5G) will offer Gb/s data rates with high spectral efficiency and minimal latency. To meet these performance targets and provide an optimal balance between coverage and implementation cost, 5G deployments in sub-6GHz bands will coexist with LTE and employ broadband operation along with massive MIMO and beamforming. This forum will describe how 5G requirements affect radio designs below 6GHz, current state-of-the-art of 5G systems, and what the future directions of key circuits and system architectures are. In addition, power efficiency along with various challenges and solutions on silicon integration of 5G radios will be also addressed.

**Forum Agenda**

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<td>Breakfast</td>
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<tr>
<td>8:20 AM</td>
<td>Introduction</td>
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| 8:30 AM| Overview of Radio RF Systems Requirements and Challenges for Sub-6GHz 5G NR Commercialization  
Walid Ali-Ahmad, Facebook, Menlo Park, CA |
| 9:20 AM| Multiband Receivers for LTE-A/5G Systems  
Thomas Byunghak Cho, Samsung Electronics, Suwon, Korea |
| 10:10 AM| Break                                                                |
| 10:30 AM| Digital Transmitters for Sub-6GHz Wireless Applications  
Leo de Vreede, Delft University of Technology, Delft, The Netherlands |
| 11:20 AM| High-Power, High-Bandwidth, and High-Efficiency Supply Modulator for 5G System  
Paul Liang, MediaTek, Hsinchu, Taiwan |
| 12:10 PM| Lunch                                                                |
| 1:10 PM| Massive MIMO for Sub-6GHz Wireless Communications  
Ove Edfors, Lund University, Lund, Sweden |
| 2:00 PM| RF Transceivers for 5G Basestations  
Tony Montalvo, Analog Devices, Raleigh, NC |
| 2:50 PM| Break                                                                |
| 3:10 PM| Power Amplifier Linearity and Efficiency Challenges for Sub-6GHz 5G Systems  
Christian Fager, Chalmers University of Technology, Gothenburg, Sweden |
| 4:00 PM| Silicon Technologies for Sub-6GHz Front-End and Radio Integrations  
Alvin Joseph, GlobalFoundries, Burlington, VT |
| 4:50 PM| Conclusion                                                           |
F2: Memory-Centric Computing from IoT to Artificial Intelligence and Machine Learning

Organizer: Fatih Hamzaoglu, Intel, Hillsboro, OR

Committee: Meng-Fan Chang, National Tsing Hua University, Hsinchu, Taiwan
Ki-Tae Park, Samsung, Hwaseong, Korea
Yasuhiko Taito, Renesas, Kodaira, Tokyo, Japan
Alicia Klinefelter, Nvidia, Durham, NC
Naveen Verma, Princeton University, Princeton, NJ

This forum will present state-of-the-art memory-centric architectures, as well as future innovative solutions to enable energy-efficient, high-performance AI/ML applications. It will also describe the challenges and solutions from edge processors to cloud applications, such as algorithmic accuracy, cost, security and practicality, including technology readiness to areas where further technology development is needed. At the high-performance and machine-learning end, emerging and storage-class memories are going to change the memory hierarchy. Meanwhile, low-power high-bandwidth DRAMs and SRAMs continue to be innovated around, to remain the workhorses of the latest process nodes (HBM, GDDR6, 7nm-FinFET SRAM etc.). Furthermore, with the explosive growth of memory intensive workloads like machine learning, video capture/playback, language translation, etc. there is a tremendous interest in preforming some compute near memory, by placing logic inside the DRAM/NVM main-memory die (AKA near-memory compute), or even doing the compute within the SRAM/STTRAM/RRAM array embedded within the compute die (AKA in-memory compute). In either case, the motivation is to reduce the significant data movement between main/embedded memory and compute units, as well as to reduce latency by preforming many operations in parallel, inside the array. Many challenges to productize these ideas remain to be addressed, including area-cost trade-offs for adding logic in the memory die for near-memory compute or augmenting embedded arrays with mixed-signal circuits to enable in-memory compute. Noticeable degradation of S/N ratio, especially in the in-memory compute case, is lurking and may direct its use to specific applications.

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<td>8:20 AM</td>
<td>Introduction by Chair, Fatih Hamzaoglu, Intel, Hillsboro, OR</td>
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<td>8:30 AM</td>
<td>Hardware-Enabled AI, Bill Dally, Nvidia, Santa Clara, CA</td>
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<td>9:20 AM</td>
<td>Embedded Memory Solutions for AI, ML and IoT Masanori Hayashikoshi, Renesas, Kodaira, Tokyo, Japan</td>
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<td>10:10 AM</td>
<td>Break</td>
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<td>10:35 AM</td>
<td>High-Bandwidth Memory (HBM) DRAM for Energy-Efficient Near-Memory Computing, Kyomin Sohn, Samsung, Hwasung, Korea</td>
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<td>11:25 AM</td>
<td>Novel Memory/Storage Solutions for Memory-Centric Computing Mohamed Arafa, Intel, Chandler, AZ</td>
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<td>12:15 PM</td>
<td>Lunch</td>
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<tr>
<td>1:20 PM</td>
<td>The Deep In-memory Architecture for Energy Efficient Machine Learning Naresh Shanbhag, UIUC, Urbana, IL</td>
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<td>2:10 PM</td>
<td>Low Power SRAM for IoT and ML Applications YK Chong, ARM, Austin, TX</td>
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<td>3:00 PM</td>
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<tr>
<td>3:20 PM</td>
<td>Advanced Memory, Logic and 3D Technologies for In-Memory Computing and Machine Learning Stefan Cosemans, IMEC, Leuven, Belgium</td>
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<td>4:10 PM</td>
<td>Deep-Learning Hardware Acceleration: Opportunities in Memory Design Leland Chang, IBM, Yorktown Heights, NY</td>
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<td>5:00 PM</td>
<td>Closing Remarks by Chair</td>
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The Student Research Preview (SRP) will highlight selected student research projects in progress. The SRP consists of 20 ninety-second presentations followed by a Poster Session, by graduate students from around the world, which have been selected on the basis of a short submission concerning their on-going research. Selection is based on the technical quality and innovation of the work. This year, the SRP will be presented in three theme sections: Digital and Machine Learning Circuits and Systems; Data Converters and Clocking; Analog and Wireless Circuits.

The Student Research Preview will include the talk "Machine Learning: The Next Big Opportunity for Chip Designers" by Professor Marian Verhelst, KU Leuven. The SRP begins at 7:30 pm on Sunday, February 17th. SRP is open to all ISSCC registrants.

Co-Chair: Denis Daly  Omni Design Technologies, MA
Co-Chair: Makoto Ikeda  University of Tokyo, Japan
Secretary: Jerald Yoo  National University of Singapore, Singapore
Advisor: Jan Van der Spiegel  University of Pennsylvania, PA
Advisor: Anantha Chandrakasan  Massachusetts Institute of Technology, MA
Media/Publications: Laura Fujino  University of Toronto, Canada
A/V: Trudy Stetzler  Houston, TX

Committee Members

Jason Anderson  University of Toronto, Canada
Masoud Babaie  Delft University of Technology, Netherlands
Andrea Baschirotto  University of Milan-Bicocca, Italy
Ben Calhoun  University of Virginia, VA
Hayun Chung  Korea University, Korea
Denis Daly  Omni Design Technologies, MA
Shidhartha Das  ARM, United Kingdom
Andreas Demosthenous  University College London, United Kingdom
Makoto Ikeda  University of Tokyo, Japan
Seulki Lee  IMEC-NL, Netherlands
Yoonmyung Lee  SungKyunkwan University, Korea
Salvatore Levantino  Politecnico di Milano, Italy
Qiang Li  University of Electronic Science & Tech., China
Shih-Chii Liu  University of Zurich / ETH Zurich, Switzerland
Shahriar Mirabbasi  University of British Columbia, Canada
Tinoosh Mohsenin  University of Maryland, MD
Cormac O’Connell  TSMC, Canada
Mondira Pant  Intel, MA
Shanthi Pavan  Indian Institute of Technology, India
Jae-sun Seo  Arizona State University, AZ
Mingoo Seok  Columbia University, NY
Farhana Sheikh  Intel, OR
Bing Sheu  Chang Gung University, Taiwan
Atsushi Shirane  Tokyo Institute of Technology, Japan
GuoXing Wang  Shanghai Jiao Tong University, China
Jeffrey Weldon  University of Hawaii, HI
Chia-Hsiang Yang  National Taiwan University, Taiwan
Rabia Tugce Yazicigil  Boston University, MA
Jerald Yoo  National University of Singapore, Singapore
Samira Zaliasl  Ferric, New York, NY
Milin Zhang  Tsinghua University, China
EE2: How to Save Lives with Circuits

Chair: Kathy Wilcox, AMD, Boxborough, MA
Organizers: Edith Beigné, Facebook, Menlo Park, CA
Dina El-Damak, University of Southern California, Los Angeles, CA
Azita Emami, California Institute of Technology, Pasadena, CA
Ulkuhan Guler, Worcester Polytechnic Institute, Worcester, MA
Rikky Muller, University of California, Berkeley, Berkeley, CA
Mandy Pant, Intel, Hudson, MA
Negar Reiskarimian, Columbia University, New York, NY
Abira Sengupta, IEEE SSCS, Piscataway, NJ
Farhana Sheikh, Intel, Hillsboro, OR
Trudy Stetzler, Halliburton, Houston, TX
Vivienne Sze, Massachusetts Institute of Technology, Cambridge, MA
Ingrid Verbauwhede, KU Leuven, Leuven, Belgium
Alice Wang, PsiKick, Santa Clara, CA
Rabia Tugce Yazicigil, Boston University, Boston, MA

The workshop highlights circuits and their impact on healthcare-related industries. The goal of the panel is to provide perspectives from system architects, security experts and circuit designers on where we should be heading with the large amount of data that is being generated from more-advanced tests and increased monitoring of our current health status.

Distinguished Speakers

6:00 - 6:30 PM
Catalyzing Growth and Innovation
Sue Siegel, GE Chief Innovation Officer and CEO, GE Business Innovations

6:30 - 7:00 PM
Better Circuits for a Better World
Dr. Jennifer Lloyd, VP, Healthcare and Consumer, Analog Devices

Invited Talks

7:00 - 7:20 PM
Unravelling the Brain with High-Density CMOS Neural Probes
Dr. Carolina Mora Lopez, Team Leader, Circuits for Neural Interfaces at imec

7:20 - 7:40 PM
Neurotechnology: Where Engineering Meets Neuroscience
Dr. Hyunjoo J. Lee, Assistant Professor Electrical Engineering, KAIST

Panel

7:45 - 9:00 PM
What Can Circuit Designers Do to Bolster Security in AI-driven Healthcare
Moderator: Ingrid Verbauwhede, KU Leuven, Leuven, Belgium

Security and privacy problems with medical devices and IOT devices in general are in the news on an almost daily basis. One example from 2017 stated: “FDA issues recall of 465,000 pacemakers to patch security holes.” Once medical data is obtained reliably and securely, it is stored on remote servers and in remote databases where there are risks of leaks and data breaches of private medical records. However, it is difficult to put the genie back into the bottle! We have asked our distinguished panel to discuss how circuit designers can contribute to bolster our trust in medical devices and in electronic healthcare systems that manage private medical records. We also encourage the audience to propose attacks and countermeasures.

Distinguished Speaker

7:45 - 8:15 PM
Perspectives on Machine Learning and Cryptography by Turing Award Winner Shafi Goldwasser
Shafi Goldwasser, Professor Electrical Engineering and Computer Sciences, University of California at Berkeley, Berkeley, CA

Panelists

Alison Burdett, Sensium Healthcare, Abingdon, United Kingdom
Shafi Goldwasser, University of California at Berkeley, Berkeley, CA
Rikky Muller, University of California at Berkeley, Berkeley, CA
Sugako Otani, Renesas Electronics Corporation, Tokyo, Japan
Vivienne Sze, Massachusetts Institute of Technology, Cambridge, MA
Wenyuan Xu, Zhejiang University, Hangzhou, China
Plenary Session — Invited Papers

Chair: Jan van der Spiegel, University of Pennsylvania, Philadelphia, PA
ISSCC Conference Chair

Associate Chair: Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands
ISSCC International Technical Program Chair

FORMAL OPENING OF THE CONFERENCE 8:30 AM

1.1 Deep Learning Hardware: Past, Present, and Future 8:45 AM
Yann LeCun, Facebook AI Research & New York University, New York, NY

Deep learning has caused revolutions in computer understanding of images, audio, and text, enabling new applications such as information search and filtering, autonomous driving, radiology screening, real-time language translation, and virtual assistants. But almost all these successes largely use supervised learning, which requires human-annotated data, or reinforcement learning, which requires too many trials to be practical in most real-world situations. In contrast, animals and humans seem to learn vast amounts of background knowledge about the world through mere observation and occasional actions in a self-supervised manner. Making progress in self-supervised learning is the main challenge of AI for the next decade. Success may result in machines with some level of common sense. But they will be built around deep learning architectures that are considerably larger than current ones, requiring vastly more powerful hardware than what we have today.

1.2 Intelligence on Silicon: 9:20 AM
From Deep Neural Network Accelerators to Brain-Mimicking AI-SoCs
Hoi-Jun Yoo, KAIST, Daejeon, Korea

Deep learning is influencing not only the technology itself but also our everyday lives. Formerly, most AI functionalities and applications were centralized on datacenters. However, the primary platform for AI has recently shifted to mobile devices. With the increasing demand on mobile AI, conventional hardware solutions face their ordeal because of their low energy efficiency on such power hungry applications. For the past few years, dedicated DNN accelerators inference have been under the spotlight. However, with the rising emphasis on privacy and personalization, ability to learn on mobile platform is becoming the second hurdle for “on-device AI.” Going hand in hand, the brain mimicking is also a highlighted field in AI. Fundamentals of neuromorphic architecture start from the synapses and the neurons, which are realized with custom memories including non-volatile memories. The brain mimicking AI is not restricted to the naive neuron implementation, but it extends further to mimic the behavioral characteristics such as “connectome” or “visual attention.” In conclusion, mobile learning and brain mimicking will be the two horses driving the carriage called AI, thus opening up new requirements for the next generation deep learning SoCs.

ISSCC, SSCS, IEEE AWARD PRESENTATIONS 9:55 AM

BREAK 10:20 AM
1.3 Integration of Photonics and Electronics  
Meint K. Smit, Eindhoven University of Technology, Eindhoven, The Netherlands

The application market for Photonic Integrated Circuits (PICs) is rapidly growing. Photonic Integration is the dominant technology in high bandwidth communications and is set to become dominant in many fields of photonics, just like microelectronics in the field of electronics. Photonic integrated circuits offer compelling performance advances in terms of precision, bandwidth and energy efficiency. To enable uptake in new sectors, the availability of highly standardized (generic) photonic integration platform technologies is of key importance as this separates design from technology, reducing barriers for new entrants. The major platform technologies today are InP-based monolithic integration and Silicon Photonics. In this perspective paper we will describe the current status and future developments of InP-based generic integration platforms.

1.4 5G Wireless Communication: An Inflection Point  
Vida Ilderem, Intel, Hillsboro, OR

The 5G era is upon us, ushering in new opportunities for technology innovation across the computing and connectivity landscape. 5G presents an inflection point where wireless communication technology is driven by application and expected use cases, and where the network will set the stage for data-rich services and sophisticated cloud apps, delivered faster and with lower latency. This paper will highlight the disruptive architectures and technology innovations required to make 5G and beyond a reality.
PROCESSORS

Session Chair: Ingrid Verbauwhede, KU Leuven, Leuven, Belgium
Associate Chair: James Myers, ARM, Cambridge, United Kingdom

1:30 PM

2.1 Summit and Sierra: Designing AI/HPC Supercomputers
J. A. Kahle1, J. Moreno2, D. Dreps3
1IBM Research, Austin, TX; 2IBM Research, Yorktown Heights, NY; 3IBM Systems and Technology, Austin, TX

2:00 PM

2.2 A 978GOPS/W Flexible Streaming Processor for Real-Time Image Processing Applications in 22nm FDSOI
S. Smets1, T. Goedemé1, A. Mitta2, M. Verhelst2
1KU Leuven, Heverlee, Belgium; 2San Jose, CA

2.3 An Energy-Efficient Configurable Lattice Cryptography Processor for the Quantum-Secure Internet of Things
U. Banerjee1, A. Pathak2, A. P. Chandrakasan2
1Massachusetts Institute of Technology, Cambridge, MA; 2Indian Institute of Technology Delhi, New Delhi, India

Break 3:00 PM

3:15 PM

2.4 A Distributed Autonomous and Collaborative Multi-Robot System Featuring a Low-Power Robot SoC in 22nm CMOS for Integrated Battery-Powered Minibots
V. Honkote1, D. Kuriyan1, S. Muthukumar1, D. Ghosh1, S. Yada1, K. Jain2, B. Jackson2, I. Klotchkov2, M. R. Nimmagadda1, S. Dattawadkar2, P. Deshmukh1, A. Gupta1, J. Timbadiya1, R. Pali1, K. Narayanan1, S. Soni1, S. Chhabra1, P. Dham1, N. Sreenivasulu1, J. Kollikunnel1, S. Kadavakollu1, V. D. Sivaraj1, P. Aseron1, L. Azarenkov2, N. Robinson2, A. Radhakrishnan3, M. Moiseev2, G. Gandakumar1, A. Madhukumar1, R. Popov2, K. P. Sahu1, R. Pegovanda1, A. Del Rio Ruiz2, M. Bhartiya1, A. Srinivasan2, V. De3
1Intel, Bangalore, India; 2Intel, Hillsboro, OR; 3Intel, Guadalajara, Mexico; 4Intel, Toronto, Canada

3:45 PM

2.5 A 40×40 Four-Neighbor Time-Based In-Memory Computing Graph ASIC Chip Featuring Wavefront Expansion and 2D Gradient Control
L. R. Everson, S. S. Sapatnekar, C. H. Kim
University of Minnesota, Minneapolis, MN

4:15 PM

2.6 A 2×30k-Spin Multichip Scalable Annealing Processor Based on a Processing-In-Memory Approach for Solving Large-Scale Combinatorial Optimization Problems
T. Takegami1, M. Hayashi2, C. Yoshimura2, M. Yamaoka2
1Hitachi, Sapporo, Japan; 2Hitachi, Tokyo, Japan

4:45 PM

2.7 A 28nm 600MHz Automotive Flash Microcontroller with Virtualization-Assisted Processor for Next-Generation Automotive Architecture Complying with ISO26262 ASIL-D
Renesas Electronics, Kodaira, Japan

Conclusion 5:15 PM
Nyquist-Rate ADCs
Session Chair: Seng-Pan (Ben) U, University of Macau, Macau, China
Associate Chair: Ahmed Ali, Analog Devices, Greensboro, NC

1:30 PM
3.1 A 3.2GS/s 10 ENOB 61mW Ringamp ADC in 16nm with Background Monitoring of Distortion
B. Hershberg, D. Dermit, B. van Liempd, E. Martens, N. Markulic, J. Lagos, J. Craninckx
imec, Leuven, Belgium

2:00 PM
3.2 A 7.6mW 1GS/s 60dB SNDR Single-Channel SAR-Assisted Pipelined ADC with Temperature-Compensated Dynamic Gm-R-Based Amplifier
W. Jiang¹, Y. Zhu¹, M. Zhang¹, C-H. Chan¹, R. P. Martins¹²
¹University of Macau, Macau, China
²Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

2:30 PM
3.3 A 5GS/s 158.6mW 12b Passive-Sampling 8×-Interleaved Hybrid ADC with 9.4 ENOB and 160.5dB FoM in 28nm CMOS
A. Ramkaj¹, J. C. Pena Ramos¹, Y. Lyu¹, M. Strackx², M. J. Pelgrom¹, M. Steyaert¹, M. Verhelst¹, F. Tavernier²
¹KU Leuven, Heverlee, Belgium; ²Nokia Bell Labs, Antwerpen, Belgium

Break 3:00 PM

3:15 PM
3.4 A 0.01mm² 25μW 2MS/s 74dB-SNDR Continuous-Time Pipelined-SAR ADC with 120fF Input Capacitor
L. Shen¹, Y. Shen¹², X. Tang¹, C-K. Hsu¹, W. Shi¹, S. Li¹, W. Zhao¹, A. Mukherjee¹, N. Sun¹
¹University of Texas, Austin, TX; ²Xidian University, Xi’an, China

3:45 PM
3.5 A 0.6V 13b 20MS/s Two-Step TDC-Assisted SAR ADC with PVT Tracking and Speed-Enhanced Techniques
M. Zhang¹, C-H. Chan¹, Y. Zhu¹, R. P. Martins¹²
¹University of Macau, Macau, China
²Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

4:15 PM
3.6 A 6-to-600MS/s Fully Dynamic Ringamp Pipelined ADC with Asynchronous Event-Driven Clocking in 16nm
B. Hershberg, B. van Liempd, N. Markulic, J. Lagos, E. Martens, D. Dermit, J. Craninckx
imec, Leuven, Belgium

4:45 PM
3.7 A 10mW 16b 15MS/s Two-Step SAR ADC with 95dB DR Using Dual-Deadzone Ring-Amplifier
A. ElShater¹, C. Y. Lee¹, P. K. Venkatachala¹, J. Muhlestein¹, S. Leuenberger¹, K. Sobue², K. Hamashita², U-K. Moon²
¹Oregon State University, Corvallis, OR; ²Asahi Kasei Microdevices, Atsugi, Japan

Conclusion 5:15 PM
Power Amplifiers

Session Chair: Krzysztof Dufrêne, Intel, Linz, Austria
Associate Chair: Harish Krishnaswamy, Columbia University, New York, NY

1:30 PM

4.1 A Watt-Level Phase-Interleaved Multi-Subharmonic Switching Digital Power Amplifier Achieving 31.4% Average Drain Efficiency
A. Zhang, M-W. Chen, University of Southern California, Los Angeles, CA

2:00 PM

4.2 A Broadband Switched-Transformer Digital Power Amplifier for Deep Back-Off Efficiency Enhancement
L. Xiong, T. Li, Y. Yin, H. Min, N. Yan, H. Xu, Fudan University, Shanghai, China

2:15 PM

4.3 A Multiphase Interpolating Digital Power Amplifier for TX Beamforming in 65nm CMOS
Z. Bai, W. Yuan, A. Azam, J. S. Walling, University of Utah, Salt Lake City, UT

2:30 PM

4.4 A Highly Linear High-Power 802.11ac/ax WLAN SiGe HBT Power Amplifier Using a Compact 2nd-Harmonic-Shorting Four-Way Transformer and Integrated Thermal Sensors
I. Ju¹, M. McPartlin², C-W. P. Huang³, C. D. Cheon⁴, M. Doherty⁵, J. D. Cressler⁵
¹Georgia Institute of Technology, Atlanta, GA; ²Skyworks Solutions, Andover, MA

2:45 PM

4.5 A 13.5dBm Fully Integrated 200-to-255GHz Power Amplifier with a 4-Way Power Combiner in SiGe:C BiCMOS
M. H. Eissa¹, D. Kissinger¹,²
¹IHP, Frankfurt (Oder), Germany; ²Technische Universität Berlin, Berlin, Germany

Break 3:00 PM

3:15 PM

4.6 A mm-Wave 3-Way Linear Doherty Radiator with Multi-Antenna Coupling and On-Antenna Current-Scaling Series Combiner for Deep Power Back-Off Efficiency Enhancement
H. T. Nguyen, S. Li, H. Wang, Georgia Institute of Technology, Atlanta, GA

3:45 PM

4.7 A Compact DC-to-108GHz Stacked-SOI Distributed PA/Driver Using Multi-Drive Inter-Stack Coupling, Achieving 1.525THz GBW, 20.8dBm Peak P1dB, and Over 100Gb/s in 64-QAM and PAM-4 Modulation
O. El-Aassar, G. M. Rebeiz, University of California, San Diego, La Jolla, CA

4:15 PM

4.8 A Highly Linear Super-Resolution Mixed-Signal Doherty Power Amplifier for High-Efficiency mm-Wave 5G Multi-Gb/s Communications
F. Wang, T-W. Li, H. Wang, Georgia Institute of Technology, Atlanta, GA

4:45 PM

4.9 A 60GHz CMOS Power Amplifier with Cascaded Asymmetric Distributed-Active-Transformer Achieving Watt-Level Peak Output Power with 20.8% PAE and Supporting 2Gsym/s 64-QAM Modulation
H. T. Nguyen, D. Jung, H. Wang, Georgia Institute of Technology, Atlanta, GA

Conclusion 5:15 PM
SESSION 5  
Monday February 18th, 1:30 PM

Image Sensors

Session Chair: Kazuko Nishimura, Panasonic Corporation, Moriguchi, Japan  
Associate Chair: Jun Deguchi, Toshiba Memory Corporation, Kawasaki, Japan

1:30 PM

5.1 A Stacked Global-Shutter CMOS Imager with SC-Type Hybrid-GS Pixel and Self-Knee Point Calibration Single-Frame HDR and On-Chip Binarization Algorithm for Smart Vision Applications

C. Xu1, Y. Mo1, G. Ren2, W. Ma2, X. Wang2, W. Shi2, J. Hou2, K. Shao2, H. Wang2, P. Xiao2, Z. Shao2, X. Xie1, X. Wang1, C. Yi1
1SmartSens Technology, San Jose, CA; 2SmartSens Technology, Shanghai, China

5.2 Energy-Efficient Low-Noise CMOS Image Sensor with Capacitor Array-Assisted Charge-Injection SAR ADC for Motion-Triggered Low-Power IoT Applications

K. D. Choo, L. Xu, Y. Kim, J-H. Seol, X. Wu, D. Sylvester, D. Blaauw
University of Michigan, Ann Arbor, MI

2:00 PM

5.3 A Data-Compressive 1.5b/2.75b Log-Gradient QVGA Image Sensor with Multi-Scale Readout for Always-On Object Detection

C. Young1, A. Omid-Zohoor1,2, P. Lajevardi3
1Stanford University, Stanford, CA; 2*now with K-Motion Interactive, San Francisco, CA
3Robert Bosch, Sunnyvale, CA

2:30 PM

Break 3:00 PM

3:15 PM

5.4 A 76mW 500fps VGA CMOS Image Sensor with Time-Stretched Single-Slope ADCs Achieving 1.95e Random Noise

I. Park1, C. Park2, J. Cheon2, Y. Chae1
1Yonsei University, Seoul, Korea
2Kumoh National Institute of Technology, Gyeongbuk, Korea

5.5 Dual-Tap Pipelined-Code-Memory Coded-Exposure-Pixel CMOS Image Sensor for Multi-Exposure Single-Frame Computational Imaging

N. Sarhangnejad1, N. Katic2, Z. Xia1, M. Wei1, N. Gusev1, G. Dutta1, R. Gulve1, H. Haim1, M. Moreno Garcia2, D. Stoppa4, K. N. Kutulakos4, R. Genov2
1University of Toronto, Toronto, Canada; 2*now with Synopsys, Toronto, Canada
3Fondazione Bruno Kessler, Trento, Italy; 4*ams AG, Ruschlikon, Switzerland

3:30 PM

5.6 A 400×400-Pixel 6μm-Pitch Vertical Avalanche Photodiodes CMOS Image Sensor Based on 150ps-Fast Capacitive Relaxation Quenching in Geiger Mode for Synthesis of Arbitrary Gain Images

Panasonic, Nagaokakyo, Japan

3:45 PM

5.7 A 256×256 40nm/90nm CMOS 3D-Stacked 120dB-Dynamic-Range Reconfigurable Time-Resolved SPAD Imager

R. K. Henderson1, N. Johnston1, S. W. Hutchings1, I. Gyongy1, T. Al Abbas1, N. Dutton1, M. Tyler1, S. Chan3, J. Leach3
1University of Edinburgh, Edinburgh, United Kingdom
2STMicroelectronics, Edinburgh, United Kingdom
3Heriot-Watt University, Edinburgh, United Kingdom

4:15 PM

5.8 A 32×32-Pixel 0.9THz Imager with Pixel-Parallel 12b VCO-Based ADC in 0.18μm CMOS

S. Yokoyama1, M. Ikebe1, Y. Kanazawa1, T. Ikegami1, P. Ambalathankandy1, S. Hiramatsu1, E. Sano1, Y. Takida2, H. Minamide2
1Hokkaido University, Sapporo, Japan; 2RIKEN, Sendai, Japan

Conclusion 5:15 PM
**Ultra-High-Speed Wireline**

Session Chair: **Tony Chan Carusone**, University of Toronto, Toronto, Canada  
Associate Chair: **Takayuki Shibasaki**, Fujitsu Laboratories, Kawasaki, Japan

1:30 PM

6.1 A 100Gb/s 1.1pJ/b PAM-4 RX with Dual-Mode 1-Tap PAM-4 / 3-Tap NRZ Speculative DFE in 14nm CMOS FinFET  
A. Cevrero, I. Ozkaya, P. A. Francese, M. Brandli, C. Menolfi, T. Morf, M. Kossel, L. Kull, D. Luu, M. Dazzi, T. Toifl, IBM Research, Ruschlikon, Switzerland

2:00 PM

6.2 A 60Gb/s PAM-4 ADC-DSP Transceiver in 7nm CMOS with SNR-Based Adaptive Power Scaling Achieving 6.9pJ/b at 32dB Loss  

2:30 PM

6.3 A Sub-250mW 1-to-56Gb/s Continuous-Range PAM-4 42.5dB IL ADC/DAC-Based Transceiver in 7nm FinFET  

Break 3:00 PM

3:15 PM

6.4 A 180mW 56Gb/s DSP-Based Transceiver for High-Density IOs in Data Center Switches in 7nm FinFET Technology  

3:45 PM

6.5 A 400Gb/s Transceiver for PAM-4 Optical Direct-Detect Application in 16nm FinFET  

4:15 PM

6.6 A 128Gb/s 1.3pJ/b PAM-4 Transmitter with Reconfigurable 3-Tap FFE in 14nm CMOS  
Z. Toprak-Deniz, J. E. Proesel, J. F. Bulzacchelli, H. A. Ainspan, T. O. Dickson, M. P. Beakes, M. Meghelli, IBM T. J. Watson Research Center, Yorktown Heights, NY

4:45 PM

6.7 A 112Gb/s PAM-4 Voltage-Mode Transmitter with 4-Tap Two-Step FFE and Automatic Phase Alignment Techniques in 40nm CMOS  

5:00 PM

6.8 A 36Gb/s Adaptive Baud-Rate CDR with CTLE and 1-Tap DFE in 28nm CMOS  
D. Yoo, M. Bagherbeik, W. Rahman, A. Sheikholeslami, H. Tamura, T. Shibasaki

Conclusion 5:15 PM
Demonstration Session 1, Monday February 18th, 5:00-7:00 PM

This year, the Demonstration Session extending in selected regular papers, both Academic and Industrial, will take place on Monday February 18th, and Tuesday February 19th, from 5 pm until 7 pm in the Golden Gate Hall. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2019, as noted by the symbol DS1.

2.3 An Energy-Efficient Configurable Lattice Cryptography Processor for the Quantum-Secure Internet of Things

2.4 A Distributed Autonomous and Collaborative Multi-Robot System Featuring a Low-Power Robot SoC in 22nm CMOS for Integrated Battery-Powered Minibots

2.6 A 2×30k-Spin Multichip Scalable Annealing Processor Based on a Processing-In-Memory Approach for Solving Large-Scale Combinatorial Optimization Problems

2.5 A 0.6V 13b 20MS/s Two-Step TDC-Assisted SAR ADC with PVT Tracking and Speed-Enhanced Techniques

2.7 A Compact DC-to-108GHz Stacked-SOI Distributed PA/Driver Using Multi-Drive Inter-Stack Coupling, Achieving 1.525THz GBW, 20.8dBm Peak P1dB, and Over 100Gb/s in 64-QAM and PAM-4 Modulation

2.8 A Highly Linear Super-Resolution Mixed-Signal Doherty Power Amplifier for High-Efficiency mm-Wave 5G Multi-Gb/s Communications

2.1 A Stacked Global-Shutter CMOS Imager with SC-Type Hybrid-GS Pixel and Self-Knee Point Calibration Single-Frame HDR and On-Chip Binarization Algorithm for Smart Vision Applications

2.2 Energy-Efficient Low-Noise CMOS Image Sensor with Capacitor Array-Assisted Charge-Injection SAR ADC for Motion-Triggered Low-Power IoT Applications

2.3 A Data-Compressive 1.5b/2.75b Log-Gradient QVGA Image Sensor with Multi-Scale Readout for Always-On Object Detection

2.4 Dual-Tap Pipelined-Code-Memory Coded-Exposure-Pixel CMOS Image Sensor for Multi-Exposure Single-Frame Computational Imaging

2.5 A 400×400-Pixel 6μm-Pitch Vertical Avalanche Photodiodes CMOS Image Sensor Based on 150ps-Fast Capacitive Relaxation Quenching in Geiger Mode for Synthesis of Arbitrary Gain Images

2.6 A 256×256 40nm/90nm CMOS 3D-Stacked 120dB-Dynamic-Range Reconfigurable Time-Resolved SPAD Imager

2.7 A 256×256 40nm/90nm CMOS 3D-Stacked 120dB-Dynamic-Range Reconfigurable Time-Resolved SPAD Imager

2.8 A 256×256 40nm/90nm CMOS 3D-Stacked 120dB-Dynamic-Range Reconfigurable Time-Resolved SPAD Imager

2.9 A 256×256 40nm/90nm CMOS 3D-Stacked 120dB-Dynamic-Range Reconfigurable Time-Resolved SPAD Imager

2.10 A 256×256 40nm/90nm CMOS 3D-Stacked 120dB-Dynamic-Range Reconfigurable Time-Resolved SPAD Imager

3.1 A Sub-250mW 1-to-56Gb/s Continuous-Range PAM-4 42.5dB IL ADC/DAC-Based Transceiver in 7nm FinFET

3.2 A 180mW 56Gb/s DSP-Based Transceiver for High-Density IOs in Data Center Switches in 7nm FinFET Technology

3.3 A 112Gb/s PAM-4 Voltage-Mode Transmitter with 4-Tap Two-Step FFE and Automatic Phase Alignment Techniques in 40nm CMOS

3.4 A 20.5TOPS and 217.3GOPS/mm² Multicore SoC with DNN Accelerator and Image Signal Processor Complying with ISO26262 for Automotive Applications

3.5 An 879GOPS 243mW 80fps VGA Fully Visual CNN-SLAM Processor for Wide-Range Autonomous Exploration

3.6 A 2.1TFLOPS/W Mobile Deep RL Accelerator with Transposable PE Array and Experience Compression

3.7 A 65nm 236.5nJ/Classification Neuromorphic Processor with 7.5% Energy Overhead On-Chip Learning Using Direct Spike-Only Feedback

3.8 LNPU: A 25.3TFLOPS/W Sparse Deep-Neural-Network Learning Processor with Fine-Grained Mixed Precision of FP8-FP16

3.9 A 93.8% Peak Efficiency, 5V-Input, 10A Max ILOAD Flying Capacitor Multilevel Converter in 22nm CMOS Featuring Wide Output Voltage Range and Flying Capacitor Precharging

3.10 A 10.9W 93.4%-Efficient (27W 97%-Efficient) Flying-Inductor Hybrid DC-DC Converter Suitable for 1-Cell (2-Cell) Battery Charging Applications

3.11 A Fully Integrated Voltage Regulator in 14nm CMOS with Package-Embedded Air-Core Inductor Featuring Self-Trimmed, Digitally Controlled Variable On-Time Discontinuous Conduction Mode Operation
Chair: Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands
Organizers: Alison Burdett, Sensium Healthcare, Abingdon, United Kingdom
Kush Gulati, Omni Design Technologies, Milpitas, CA
Un-Ku Moon, Oregon State University Corvallis, OR
Committee: Ahmed Ali, Analog Devices, Greensboro, NC
Min Chen, Analog Devices, Milpitas, CA
Muhammad Khellah, Intel, Hillsboro, OR
Yan Li, Western Digital, Milpitas, CA
Yao-Hong Liu, imec, Eindhoven, The Netherlands
Michael Perrott, TDK-Invensense, Boston, MA
Bruce Rae, ST Microelectronics, Edinburgh, United Kingdom
Jiayoon Ru, Broadcom, Irvine, CA
Takayuki Shibasaki, Fujitsu Laboratories, Kawasaki, Japan
Youngmin Shin, Samsung, Hwaseong, Korea

The event will begin with a Showcase Keynote “Accelerated Platforms: The Future of Computing” by Bill Dally, Chief Scientist and Senior Vice President of Research, NVIDIA, Santa Clara, CA and Professor (Research) of EE and CS, Stanford University, Stanford, CA.

Following the keynote, the Industry Showcase will feature short presentations as well as interactive demonstrations from each of the Industry Showcase participants, and represent an exciting introduction to the next generation of applications and products enabled by advances in solid-state integrated circuits.

The list below highlights the list of participants in the Industry Showcase.

Altia Systems, Cupertino, CA
180° Real-time Immersive, Intelligent Vision Systems

ams AG, Premstätten, Austria
Direct Time-of-Flight Module in CMOS 55nm HV for Mobile Applications

Ayar Labs, Emeryville, CA
TeraPHY: A high-density electronic-photonic chiplet for co-packaged optical I/O

Healthian, Daejeon, Korea
Impedance-based Sensor Chip for Non-invasive Blood Pressure Monitoring

IBM T. J. Watson Research Center, Yorktown Heights, NY
Fast channel sounding and beam optimization for 5G using software defined phased array radios

Mediatek, HsinChu, Taiwan
Future Driving with Better Safety Inside-Out

NUFRONT, Beijing, China
The world’s first deployed URLLC wireless communication system and SoCs

NVIDIA, Santa Clara, CA
Deep Learning Inference on NVIDIA GPUs and Accelerators

Ouster, San Francisco, CA
Native camera imaging on LiDAR and deep learning enablement

PsiKick, Santa Clara, CA
PsiKick’s Batteryless Sensor Network Platform for the Industrial IoT

Samsung Electronics, Hwaseong, Korea
A Fully Integrated 10nm Multi-Mode 5G Modem Chipset Compatible with 3GPP NR Standards

SiFive, San Mateo, CA
Unleashed Acceleration: AI on RISC-V
8:30 AM
7.1 An 11.5TOPS/W 1024-MAC Butterfly Structure Dual-Core Sparsity-Aware Neural Processing Unit in 8nm Flagship Mobile SoC
J. Song 1, Y. Cho 1, J-S. Park 1, J-W. Jang 2, S. Lee 2, J-H. Song 2, J-G. Lee 2, I. Kang 2
1Samsung Electronics, Hwaseong, Korea
2Samsung Advanced Institute of Technology, Suwon, Korea

9:00 AM
7.2 A 20.5TOPS and 217.3GOPS/mm² Multicore SoC with DNN Accelerator and Image Signal Processor Complying with ISO26262 for Automotive Applications
Toshiba Electronic Devices & Storage, Kawasaki, Japan

9:30 AM
7.3 An 879GOPS 243mW 80fps VGA Fully Visual CNN-SLAM Processor for Wide-Range Autonomous Exploration
Z. Li, Y. Chen, L. Gong, L. Liu, D. Sylvester, D. Blaauw, H-S. Kim
University of Michigan, Ann Arbor, MI

10:00 AM
Break

10:15 AM
7.4 A 2.1TFLOPS/W Mobile Deep RL Accelerator with Transposable PE Array and Experience Compression
C. Kim, S. Kang, D. Shin, S. Choi, Y. Kim, H-J. Yoo
KAIST, Daejeon, Korea

10:45 AM
7.5 A 65nm 0.39-to-140.3TOPS/W 1-to-12b Unified Neural-Network Processor Using Block-Circulant-Enabled Transpose-Domain Acceleration with 8.1x Higher TOPS/mm² and 6T HBST-TRAM-Based 2D Data-Reuse Architecture
J. Yue 1, R. Liu 1, W. Sun 1, Z. Yuan 1, Z. Wang 1, Y-N. Tu 1, Y-J. Chen 2, A. Ren 3, Y. Wang 3, M-F. Chang 3, X. Li 3, H. Yang 1, Y. Liu 1
1Tsinghua University, Beijing, China
2National Tsing Hua University, Hsinchu, Taiwan
3Northeastern University, Boston, MA

11:00 AM
7.6 A 65nm 236.5nJ/Classification Neuromorphic Processor with 7.5% Energy Overhead On-Chip Learning Using Direct Spike-Only Feedback
J. Park, J. Lee, D. Jeon
Seoul National University, Seoul, Korea

11:30 AM
7.7 LNPU: A 25.3TFLOPS/W Sparse Deep-Neural-Network Learning Processor with Fine-Grained Mixed Precision of FP8-FP16
J. Lee, J. Lee, D. Han, J. Lee, G. Park, H-J. Yoo
KAIST, Daejeon, Korea

Conclusion 12:15 PM
DC-DC Converters
Session Chair: Gerard Villar Pique, NXP Semiconductor, Eindhoven, The Netherlands
Associate Chair: Jason Stauth, Dartmouth College, Hanover, NH

8:30 AM
8.1 A 93.8% Peak Efficiency, 5V-Input, 10A Max $I_{LOAD}$ Flying Capacitor Multilevel Converter in 22nm CMOS Featuring Wide Output Voltage Range and Flying Capacitor Precharging
C. Schaef¹, S. Weng¹, B. Cho², W. Lambert², K. Radhakrishnan², K. Ravichandran¹, J. Tschanz², V. De¹
¹Intel, Hillsboro, OR
²Intel, Chandler, AZ

9:00 AM
8.2 A Continuous-Input-Current Passive-Stacked Third-Order Buck Converter Achieving 0.7W/mm² Power Density and 94% Peak Efficiency
A. Abdulslam, P. P. Mercier, University of California, San Diego, La Jolla, CA

9:30 AM
8.3 A 10.9W 93.4%-Efficient (27W 97%-Efficient) Flying-Inductor Hybrid DC-DC Converter Suitable for 1-Cell (2-Cell) Battery Charging Applications
C. Hardy, H-P. Le
University of Colorado, Boulder, CO

Break 10:00 AM

10:15 AM
8.4 Fully Integrated Buck Converter with 78% Efficiency at 365mW Output Power Enabled by Switched-Inductor-Capacitor Topology and Inductor Current Reduction Technique
N. Tang¹, B. Nguyen¹, Y. Tang², W. Hong¹, Z. Zhou¹, D. Heo¹
¹Washington State University, Pullman, WA
²HiSilicon, Shenzhen, China

10:45 AM
8.5 A Fully Integrated Voltage Regulator in 14nm CMOS with Package-Embedded Air-Core Inductor Featuring Self-Trimmed, Digitally Controlled Variable On-Time Discontinuous Conduction Mode Operation
C. Schaef¹, N. Desai², H. Krishnamurthy¹, S. Weng¹, H. Do², W. Lambert², K. Radhakrishnan², K. Ravichandran¹, J. Tschanz², V. De¹
¹Intel, Hillsboro, OR
²Intel, Chandler, AZ

11:15 AM
8.6 A Fully Integrated 85%-Peak-Efficiency Hybrid Multi-Ratio Resonant DC-DC Converter with 3.0-to-4.5V Input and 500μA-to-120mA Load Range
P. Renz¹, M. Kaufmann¹, M. Lueders³, B. Wicht¹
¹Leibniz University Hannover, Hannover, Germany
²Texas Instruments, Freising, Germany

11:45 AM
8.7 A 2MHz 4-to-60V in Buck-Boost Converter for Automotive Use Achieving 95% Efficiency and CISPR 25 Class 5 Standard
J. Xue, M. K. Song, X. Ke, M. Chen, L. Shtargot
Analog Devices, Milpitas, CA

Conclusion 12:15 PM
High-Frequency Transceivers for Radar and Communications

Session Chair: Nagendra Krishnapura, Indian Institute of Technology Madras, Chennai, India
Associate Chair: Yuu Watanabe, Waseda University, Atsugi, Japan

8:30 AM

9.1 Toward Automotive Surround-View Radars
1MediaTek, Hsinchu, Taiwan; 2MediaTek, San Jose, CA; 3MediaTek, Hefei, China

9:00 AM

9.2 A 192-Virtual-Receiver 77/79GHz GMSK Code-Domain MIMO Radar System-on-Chip

9:30 AM

9.3 A 680µW Burst-Chirp UWB Radar Transceiver for Vital Signs and Occupancy Sensing up to 15m Distance

Break 10:00 AM

10:15 AM

9.4 A 145GHz FMCW-Radar Transceiver in 28nm CMOS
A. Visweswaran, K. Vessen, S. Sinha, I. Ocket, M. Glasse, C. Dessert, A. Bourdoux, P. Wambacq, imec, Leuven, Belgium

10:30 AM

9.5 An 80Gb/s 300GHz-Band Single-Chip CMOS Transceiver
1Hiroshima University, Higashihiroshima, Japan; 2National Institute of Information and Communications Technology, Koganei, Japan; 3Panasonic, Yokohama, Japan

10:45 AM

9.6 A 42.2Gb/s 4.3pj/b 60GHz Digital Transmitter with 12b/Symbol Polarization MIMO
C. Thakkar, S. Shopov, A. Chakrabarti, S. Yamada, D. Choudhury, J. Jaussi, B. Casper
Intel, Hillsboro, OR

11:15 AM

9.7 A Scalable 71-to-76GHz 64-Element Phased-Array Transceiver Module with 2×2 Direct-Conversion IC in 22nm FinFET CMOS Technology
1Intel, Hillsboro, OR; 2Hillsboro, OR; 3Intel, Chandler, AZ

11:45 AM

9.8 A 28GHz 20.3%-Transmitter-Efficiency 1.5°-Phase-Error Beamforming Front-End IC with Embedded Switches and Dual-Vector Variable-Gain Phase Shifters
J. Park *, S. Lee *, D. Lee, S. Hong
1KAIST, Daejeon, Korea; 2Hanbat National University, Daejeon, Korea; *Equally-Credited Authors (ECAs)

Conclusion 12:15 PM
8:30 AM

10.1 An Energy Measurement Front-End with Integrated In-Situ Background Full System Accuracy Monitoring Including the Current and Voltage Sensors
S. Danesh¹, W. Holland¹, J. Spalding¹, M. Guidry², J. Hurwitz²
¹Analog Devices, Edinburgh, United Kingdom
²Analog Devices, Wilmington, MA

9:00 AM

10.2 A 22ng/√Hz 17mW MEMS Accelerometer with Digital Noise-Reduction Techniques
Hitachi, Tokyo, Japan

9:30 AM

10.3 A 0.12mm² Wien-Bridge Temperature Sensor with 0.1°C (3σ) Inaccuracy from -40°C to 180°C
S. Pan, Ç. Gürleyük, M. F. Pimenta, K. A. A. Makinwa
Delft University of Technology, Delft, The Netherlands

9:45 AM

10.4 A Wheatstone-Bridge Temperature Sensor with a Resolution FoM of 20fJ·K²
S. Pan, K. A. A. Makinwa
Delft University of Technology, Delft, The Netherlands

Break 10:00 AM
10:15 AM

11.1 A 5.37mW/Channel Pitch-Matched Ultrasound ASIC with Dynamic-Bit-Shared SAR ADC and 13.2V Charge-Recycling TX in Standard CMOS for Intracardiac Echocardiography
J. Lee¹, K-R. Lee¹, B. E. Eovino², J. H. Park³, L. Lin², H-J. Yoo⁴, J. Yoo⁵,⁶
¹KAIST, Daejeon, Korea
²University of California, Berkeley, CA
³National University of Singapore, Singapore
⁴Singapore Institute for Neurotechnology, Singapore

10:45 AM

11.2 A CMOS Biosensor Array with 1024 3-Electrode Voltammetry Pixels and 93dB Dynamic Range
A. Manickam¹, K-D. You², N. Wood³, L. Pei⁴, Y. Liu⁴, R. Singh⁵, N. Gaminiv, D. Shahrjerdi⁶, R. G. Kuimelis¹, A. Hassibi¹
¹InSilixa, Sunnyvale, CA
²New York University, New York, NY

11:15 AM

11.3 A Capacitive Biosensor for Cancer Diagnosis Using a Functionalized Microneedle and a 13.7b-Resolution Capacitance-to-Digital Converter from 1 to 100nF
Yonsei University, Seoul, Korea

11:45 AM

11.4 A Fast-Readout Mismatch-Insensitive Magnetoresistive Biosensor Front-End Achieving Sub-ppm Sensitivity
X. Zhou, M. Sveiven, D. A. Hall
University of California, San Diego, La Jolla, CA

12:00 PM

11.5 A 512-Pixel 3kHz-Frame-Rate Dual-Shank Lensless Filterless Single-Photon-Avalanche-Diode CMOS Neural Imaging Probe
C. Lee¹,², A. J. Taal¹, J. Choi¹, K. Kim¹, K. Tien¹, L. Moreaux⁳, M. L. Roukes⁴, K. L. Shepard¹
¹Columbia University, New York, NY
²KIST, Seoul, Korea
³California Institute of Technology, Pasadena

Conclusion 12:15 PM
8:30 AM

12.1 An FPGA-Accelerated Fully Nonvolatile Microcontroller Unit for Sensor-Node Applications in 40nm CMOS/MTJ-Hybrid Technology Achieving 47.14 μW Operation at 200MHz

M. Natsui¹, D. Suzuki¹, A. Tamakoshi¹, T. Watanabe¹-², H. Honjo¹-², H. Koike¹-², T. Nasuno¹-², Y. Ma¹, T. Tanigawa¹-², Y. Noguchi¹-², M. Yasuhira¹-², H. Sato¹, S. Ikeda¹-², H. Ohno¹, T. Endoh¹-², T. Hanyu¹
¹Tohoku University, Miyagi, Japan
²JST/ACCEL, Tokyo, Japan

9:00 AM

12.2 Micro Short-Circuit Detector Including S/H Circuit for 1hr Retention and 52dB Comparator Composed of C-Axis Aligned Crystalline IGZO FETs for Li-Ion Battery Protection IC

H. Inoue¹, T. Aoki¹, F. Akasawa¹, T. Hamada¹, T. Takeuchi¹, K. Nei¹, T. Seki¹, Y. Yakubo¹, K. Takahashi¹, S. Fukai¹, T. Ishizu¹, M. Kozuma¹, R. Tajima¹, T. Matsuzaki¹, T. Ikeda¹, M. Ikeda², S. Yamazaki²
¹Semiconductor Energy Laboratory, Kanagawa, Japan
²University of Tokyo, Tokyo, Japan

9:30 AM

12.3 Memory Solutions for Flexible Thin-Film Logic: up to 8kb, >105.9kb/s LPROM and SRAM with Integrated Timing Generation Meeting the ISO NFC Standard

F. De Roose¹-², J. Genoe¹-², A. J. Kronemeijer³, K. Myny², W. Dehaene¹-²
¹KU Leuven, Heverlee, Belgium
²imec, Heverlee, Belgium
³Holst Centre/TNO, Eindhoven, The Netherlands

Break 10:00 AM
Non-Volatile Memories

Session Chair: Yan Li, Western Digital, Milpitas, CA
Associate Chair: Jongmin Park, SK Hynix, Icheon-si, Gyeonggi-do, Korea

10:15 AM

13.1 A 1.33Tb 4-bit/Cell 3D-Flash Memory on a 96-Word-Line-Layer Technology
N. Shibata1, K. Kanda1, T. Shimizu1, J. Nakai2, O. Nagao1, N. Kobayashi1, M. Miakashi1, Y. Nagadomi1, T. Nakano1, T. Kawabe1, T. Shibuya1, M. Sakoi1, K. Yanagidaira1, T. Hashimoto1, H. Date1, M. Sato1, T. Nakagawa1, H. Takamoto1, J. Mushi1, T. Minamoto1, M. Uda1, D. Nakamura1, K. Sakurai1, T. Yamashita1, J. Zhou1, R. Tachibana1, T. Tagakiwa1, T. Sugimoto1, M. Ogawa1, Y. Ochi1, K. Kawaguchi1, M. Kojima1, T. Ogawa1, T. Hashiguchi1, R. Fukuda1, M. Masuda1, K. Kawakami1, T. Someya1, Y. Kajitani1, Y. Matsumoto1, N. Morozumi1, J. Sato1, N. Raghunathann1, Y. L. Koh1, S. Chen1, J. Lee2, H. Nasu1, H. Sugawara2, K. Hosono1, T. Hisada1, T. Kaneko1, H. Nakamura1
1Toshiba Memory, Yokohama, Japan; 2Western Digital, Milpitas, CA

10:45 AM

13.2 A 3.6Mb 10.1Mb/mm² Embedded Non-Volatile ReRAM Macro in 22nm FinFET Technology with Adaptive Forming/Set/Reset Schemes Yielding Down to 0.5V with Sensing Time of 5ns at 0.7V
Intel, Hillsboro, OR

11:15 AM

13.3 A 7Mb STT-MRAM in 22FFL FinFET Technology with 4ns Read Sensing Time at 0.9V Using Write-Verify-Write Scheme and Offset-Cancellation Sensing Technique
Intel, Hillsboro, OR

11:30 AM

13.4 A 512Gb 3-bit/Cell 3D 6th-Generation V-NAND Flash Memory with 82MB/s Write Throughput and 1.2Gb/s Interface
Samsung Electronics, Hwasung, Korea

11:45 AM

13.5 A 512Gb 3-bit/Cell 3D Flash Memory on 128-Wordline-Layer with 132MB/s Write Performance Featuring Circuit-Under-Array Technology
C. Siau1, K-H. Kim1, S. Lee1, K. Isobe2, N. Shibata3, K. Verma1, T. Ariki1, J. Li1, J. Yuh1, A. Amarnath1, Q. Nguyen1, O. Kwon1, S. Jeong1, H. Li1, H-L. Hsu1, T-Y. Tseng1, S. Choi1, S. Darne1, P. Anantula1, A. Yap1, H. Chibvongodze1, H. Miwa1, M. Yamashita1, M. Watanabe1, K. Hayashi1, Y. Kato1, T. Miwa1, J. Y. Kang1, M. Okumura1, N. Ooku1, M. Balaga1, V. Ramachandra1, A. Matsuda1, S. Kulkani1, R. Rachineni1, P. K. Manjunath1, M. Takehara1, A. Pai1, S. Rajendra1, T. Hisada1, R. Fukuda1, N. Tekiwa1, K. Kawaguchi1, M. Yamaoka1, H. Koma1, T. Minamoto2, M. Unno1, S. Ozawa2, H. Nakamura2, T. Hishida2, Y. Kajitan1, L. Lin1
1Western Digital, Milpitas, CA; 2Toshiba Memory, Yokohama, Japan

Conclusion 12:15 PM
Machine Learning & Digital LDO Circuits
Session Chair: Vivek De, Intel, Beaverton, OR
Associate Chair: Ping-Ying Wang, CMOS-Crystal Technology, Zhubei City, Hsinchu County, Taiwan

1:30 PM

14.1  A 65nm 1.1-to-9.1TOPS/W Hybrid-Digital-Mixed-Signal Computing Platform for Accelerating Model-Based and Model-Free Swarm Robotics
N. Cao, M. Chang, A. Raychowdhury
Georgia Institute of Technology, Atlanta, GA

2:00 PM

14.2  A Compute SRAM with Bit-Serial Integer/Floating-Point Operations for Programmable In-Memory Vector Acceleration
J. Wang, X. Wang, C. Eckert, A. Subramaniyan, R. Das, D. Blaauw, D. Sylvester
University of Michigan, Ann Arbor, MI

2:30 PM

14.3  A 43pJ/Cycle Non-Volatile Microcontroller with 4.7µs Shutdown/Wake-up Integrating 2.3-bit/Cell Resistive RAM and Resilience Techniques
T. F. Wu¹, B. Q. Le¹, R. Radway¹, A. Bartolo¹, W. Hwang¹, S. Jeong¹, H. Li¹, P. Tandon¹, E. Vianello², P. Vivet², E. Nowak², M. K. Wootters¹, H-S. P. Wong¹, M. M. Sabry Aly³, E. Beigne³, S. Mitra¹
¹Stanford University, Stanford, CA
²CEA-LETI-MINATEC, Grenoble, France
³Nanyang Technological University, Singapore

Break 3:00 PM

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14.4  All-Digital Time-Domain CNN Engine Using Bidirectional Memory Delay Lines for Energy-Efficient Edge Computing
A. Sayal, S. Fathima, S. T. Nibhanupudi, J. P. Kulkarni
University of Texas, Austin, TX

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14.5  A 0.6-to-1.1V Computationally Regulated Digital LDO with 2.79-Cycle Mean Settling Time and Autonomous Runtime Gain Tracking in 65nm CMOS
X. Sun, A. Boora, W. Zhang, V. R. Pamula, V. Sathe
University of Washington, Seattle, WA

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14.6  A 745pA Hybrid Asynchronous Binary-Searching and Synchronous Linear-Searching Digital LDO with 3.8×10⁵ Dynamic Load Range, 99.99% Current Efficiency, and 2mV Output Voltage Ripple
S. Li, B. H. Calhoun
University of Virginia, Charlottesville, VA

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14.7  A Modular Hybrid LDO with Fast Load-Transient Response and Programmable PSRR in 14nm CMOS Featuring Dynamic Clamp Tuning and Time-Constant Compensation
Intel, Hillsboro, OR

Conclusion 5:15 PM
Power for 5G, Wireless Power, and GaN Converters
Session Chair: Min Chen, Analog Devices, Milpitas, CA
Associate Chair: Johan Janssens, ON Semiconductor, Mechelen, Belgium

1:30 PM

15.1 An 88%-Efficiency Supply Modulator Achieving 1.08μs/V Fast Transition and 100MHz Envelope-Tracking Bandwidth for 5G New Radio RF Power Amplifier
J-S. Paek, D. Kim, J-S. Bang, J. Baek, J. Choi, T. Nomiyama, J. Han, Y. Choo, Y. Youn, E. Park, S. Lee, J-H. Kim, J. Lee, T. B. Cho, I. Kang
Samsung Electronics, Hwaseong, Korea

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15.2 A 90ns/V Fast-Transition Symbol-Power-Tracking Buck Converter for 5G mm-Wave Phased-Array Transceiver
J-S. Paek, T. Nomiyama, J. Han, J-H. Kim, Y. Lee, D. Kim, E. Park, S. Lee, J. Lee, T. B. Cho, I. Kang, Samsung Electronics, Hwaseong, Korea

2:30 PM

15.3 A 100W and 91% GaN-Based Class-E Wireless-Power-Transfer Transmitter with Differential-Impedance-Matching Control for Charging Multiple Devices
C-Y. Xie1, S-H. Yang1, S-F. Lu1, F-Y. Lin1, Y-A. Lin1, Y-Z. Ou-Yang1, K-H. Chen1, K-C. Liu1, Y-H. Lin2
1National Chiao Tung University, Hsinchu, Taiwan
2Realtek Semiconductor, Hsinchu, Taiwan

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15.4 A 52% Peak-Efficiency >1W Isolated Power Transfer System Using Fully Integrated Magnetic-Core Transformer
Z. Yue1, M. Shaoyu2, Z. Tianting2, Q. Wenhui2, Z. Yuanyuan2, G. Yingjie1, C. Baoxing3
1Analog Devices, Beijing, China; 2Analog Devices, Shanghai, China
3Analog Devices, Wilmington, MA

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15.5 An 800mW Fully Integrated Galvanic Isolated Power Transfer System Meeting CISPR 22 Class-B Emission Levels with 6dB Margin
W. Qin1, X. Yang3, S. Ma1, F. Liu2, Y. Zhao2, T. Zhao2, B. Chen2
1Analog Devices, Shanghai, China; 2Analog Devices, Beijing, China
3Analog Devices, Wilmington, MA

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15.6 A 10MHz ë-Collapse Failure Self-Prognostic GaN Power Converter with Tj-Independent In-Situ Condition Monitoring and Proactive Temperature Frequency Scaling
Y. Chen, D. B. Ma, University of Texas at Dallas, Richardson, TX

4:45 PM

15.7 An 8.3MHz GaN Power Converter Using Markov Continuous RSSM for 35dBµV Conducted EMI Attenuation and One-Cycle TON Rebalancing for 27.6dB VJ Jittering Suppression
Y. Chen, D. B. Ma, University of Texas at Dallas, Richardson, TX

5:00 PM

15.8 A 4.5V/ns Active Slew-Rate-Controlling Gate Driver with Robust Discrete-Time Feedback Technique for 600V Superjunction MOSFETs
S. Kawai, T. Ueno, K. Onizuka, Toshiba, Kawasaki, Japan

Conclusion 5:15 PM
SESSION 16  
Tuesday February 19th, 1:30 PM

Frequency Synthesizers

Session Chair: Xiang Gao, Zhejiang University, Hangzhou, China
Associate Chair: Jaehyouk Choi, Ulsan National Institute of Science Technology, Ulsan, Korea

1:30 PM

16.1  A 265µW Fractional-N Digital PLL with Seamless Automatic Switching Subsampling/Sampling Feedback Path and Duty-Cycled Frequency-Locked Loop in 65nm CMOS
Tokyo Institute of Technology, Tokyo, Japan

16.2  A 76fs rms Jitter and —40dBc Integrated-Phase-Noise 28-to-31GHz Frequency Synthesizer Based on Digital Sub-Sampling PLL Using Optimally Spaced Voltage Comparators and Background Loop-Gain Optimization
Ulsan National Institute of Science and Technology, Ulsan, Korea; *Equally-Credited Authors (ECAs)

1:15 PM

16.3  A -246dB Jitter-FoM 2.4GHz Calibration-Free Ring-Oscillator PLL Achieving 9% Jitter Variation Over PVT
X. Yang1, C-H. Chan1, Y. Zhu1, R. P. Martins1,2
1University of Macau, Macau, China; 2Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

16.4  A 0.5-to-2.5GHz Multi-Output Fractional Frequency Synthesizer with 90fs Jitter and ~106dBc Spurious Tones Based on Digital Spur Cancellation
S-Y. Hung, S. Pamarti
University of California, Los Angeles, CA

2:00 PM

16.5  A Fractional-N Synthesizer with 110fs rms Jitter and a Reference Quadrupler for Wideband 802.11ax
F. Song1, Y. Zhao1, B. Wu1, L. Tang1, L. Lin1, B. Razavi2
1Ubilinx Technology, San Jose, CA; 2University of California, Los Angeles, CA

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16.6  A Calibration-Free Triple-Loop Bang-Bang PLL Achieving 131fs rms Jitter and -70dBc Fractional Spurs
D. Yang1, A. Abidi1, H. Darabi2, H. Xu1, D. Murphy2, H. Wu2, Z. Wang2
1University of California, Los Angeles, CA; 2Broadcom, Irvine, CA
2Columbia University, New York, NY

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16.7  A 30GHz Digital Sub-Sampling Fractional-N PLL with 198fs rms Jitter in 65nm LP CMOS
L. Grimaldi, L. Bertulessi, S. Karman, D. Cherniak, A. Garghetti, C. Samori, A. L. Lacaita, S. Levantino
Politecnico di Milano, Milan, Italy

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16.8  A 25.4-to-29.5GHz 10.2mW Isolated Sub-Sampling PLL Achieving -252.9dB Jitter-Power FoM and -63dBc Reference Spur
Z. Yang1, Y. Chen1, S. Yang1, P-I. Mak1, R. P. Martins1,2
1University of Macau, Macau, China; 2Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

4:00 PM

16.9  4.48GHz 0.18μm SiGe BiCMOS Exact-Frequency Fractional-N Frequency Synthesizer with Spurious-Tone Suppression Yielding a -80dBc In-Band Fractional Spur
M. P. Kennedy1,2, Y. Donnelly1,3, J. Breslin1, S. Tulisi1, S. Patil1, C. Curtin1, S. Brookes1, B. Shelly1, P. Griffin1, M. Keaveney4
1University College Dublin, Dublin, Ireland; 2Microelectronic Circuits Centre Ireland, Dublin, Ireland
3Microelectronic Circuits Centre Ireland, Cork, Ireland; 4Analog Devices, Limerick, Ireland

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Conclusion 5:15 PM
17.1 AI x Robotics: Technology Challenges and Opportunities in Sensors, Actuators, and Integrated Circuits

M. Fujita
Sony, Tokyo, Japan

2:00 PM

17.2 A 142nW Voice and Acoustic Activity Detection Chip for mm-Scale Sensor Nodes Using Time-Interleaved Mixer-Based Frequency Scanning

University of Michigan, Ann Arbor, MI; *Equally-Credited Authors (ECAs)

2:30 PM

17.3 Hybrid System for Efficient LAE-CMOS Interfacing in Large-Scale Tactile-Sensing Skins via TFT-Based Compressed Sensing

Princeton University, Princeton, NJ; *Equally-Credited Authors (ECAs)

Break 3:00 PM

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17.4 16MHz FRAM Micro-Controller with a Low-Cost Sub-1μA Embedded Piezo-Electric Strain Sensor for ULP Motion Detection

S. Khanna 1, M. Zwerg 1, B. Elies 1, J. Luebbe 1, N. Krishnasawamy 1, H. Najar 2, S. Bellary 2, W-Y. Shih 1, S. Summerfelt 1, S. Bartling 1
1Texas Instruments, Dallas, TX
2Texas Instruments, Santa Clara, CA

3:30 PM

17.5 A 0.8mm³ Ultrasonic Implantable Wireless Neural Recording System with Linear AM Backscattering

University of California, Berkeley, CA

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17.6 A Sub-40µW 5Mb/s Magnetic Human Body Communication Transceiver Demonstrating Trans-Body Delivery of High-Fidelity Audio to a Wearable In-Ear Headphone

J. Park, P. P. Mercier
University of California, San Diego, La Jolla, CA

4:15 PM

17.7 A 7.0fps Optical and Electrical Dual Tomographic Imaging SoC for Skin-Disease Diagnosis System

KAIST, Daejeon, Korea

4:45 PM

17.8 A 2.6µW Monolithic CMOS Photoplethysmographic Sensor Operating with 2pW LED Power

A. Caizzone, A. Boukhayma, C. Enz
EPFL, Neuchâtel, Switzerland

Conclusion 5:15 PM
Analog Techniques

Session Chair: David Blaauw, University of Michigan, Ann Arbor, MI
Associate Chair: Byungsub Kim, POSTECH, Pohang, Gyeongbuk, Korea

1:30 PM

18.1 A -105dBc THD+N (-114dBc HD2) at 2.8Vpp Swing and 120dB DR Audio Decoder with Sample-and-Hold Noise Filtering and Poly Resistor Linearization Schemes
S-H. Wen, K-D. Chen, C-H. Hsiao, Y-C. Chen, MediaTek, Hsinchu, Taiwan

2:00 PM

18.2 A 16fJ/Conversion-Step Time-Domain Two-Step Capacitance-to-Digital Converter
X. Tang, S. Li, L. Shen, W. Zhao, X. Yang, R. Williams, J. Liu, Z. Tan, N. Hall, N. Sun
1University of Texas, Austin, TX
2University of Electronic Science and Technology of China, Chengdu, China
3Analog Devices, Boston, MA

2:30 PM

18.3 An Auto-Zero Stabilized Voltage Buffer with a Quiet Chopping Scheme and Constant Input Current
T. Rooijers, J. H. Huijsing, K. A. A. Makinwa
Delft University of Technology, Delft, The Netherlands

Break 3:00 PM

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18.4 A 0.55nW/0.5V 32kHz Crystal Oscillator Based on a DC-Only Sustaining Amplifier for IoT
H. Esmaeilzadeh, S. Pamarti, University of California, Los Angeles, CA

3:45 PM

18.5 A 54MHz Crystal Oscillator with 30x Start-Up Time Reduction Using 2-Step Injection in 65nm CMOS
1University of Illinois, Urbana-Champaign, IL; 2Texas Instruments, Dallas, TX

4:15 PM

18.6 A 32MHz Crystal Oscillator with Fast Startup Using Synchronized Signal Injection
B. Verhoef, J. Prummel, W. Kruiskamp, R. Post
1Dialog Semiconductor, Hengelo, The Netherlands
2Dialog Semiconductor, 's-Hertogenbosch, The Netherlands

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18.7 A 0.7V, 2.35% 3σ-Accuracy Bandgap Reference in 12nm CMOS
TSMC, Hsinchu, Taiwan

4:45 PM

18.8 A 192pW Hybrid Bandgap-Vth Reference with Process Dependence Compensated by a Dimension-Induced Side-Effect
Y. Ji, J. Lee, B. Kim, H-J. Park, J-Y. Sim
Pohang University of Science and Technology, Pohang, Korea

Conclusion 5:15 PM
9.3 A 680µW Burst-Chirp UWB Radar Transceiver for Vital Signs and Occupancy Sensing up to 15m Distance

9.4 A 145GHz FMCW-Radar Transceiver in 28nm CMOS

9.5 An 80Gb/s 300GHz-Band Single-Chip CMOS Transceiver

9.7 A Scalable 71-to-76GHz 64-Element Phased-Array Transceiver Module with 2×2 Direct-Conversion IC in 22nm FinFET CMOS Technology

10.1 An Energy Measurement Front-End with Integrated In-Situ Background Full System Accuracy Monitoring Including the Current and Voltage Sensors

10.2 A 22ng/√Hz 17mW MEMS Accelerometer with Digital Noise-Reduction Techniques

11.5 A 512-Pixel 3kHz-Frame-Rate Dual-Shank Lensless Filterless Single-Photon-Avalanche-Diode CMOS Neural Imaging Probe

12.2 Micro Short-Circuit Detector Including S/H Circuit for 1hr Retention and 52dB Comparator Composed of C-Axis Aligned Crystalline IGZO FETs for Li-Ion Battery Protection IC

14.1 A 65nm 1.1-to-9.1TOPS/W Hybrid-Digital-Mixed-Signal Computing Platform for Accelerating Model-Based and Model-Free Swarm Robotics

14.3 A 43pJ/Cycle Non-Volatile Microcontroller with 4.7µs Shutdown/Wake-up Integrating 2.3-bit/Cell Resistive RAM and Resilience Techniques

16.5 A Fractional-N Synthesizer with 110fs Jitter and a Reference Quadrupler for Wideband 802.11ax

17.1 AI x Robotics: Technology Challenges and Opportunities in Sensors, Actuators, and Integrated Circuits

17.4 16MHz FRAM Micro-Controller with a Low-Cost Sub-1µA Embedded Piezo-Electric Strain Sensor for ULP Motion Detection

17.8 A 2.6µW Monolithic CMOS Photoplethysmographic Sensor Operating with 2µW LED Power

18.4 A 0.55nW/0.5V 32kHz Crystal Oscillator Based on a DC-Only Sustaining Amplifier for IoT

21.1 A 28GHz CMOS Phased-Array Beamformer Utilizing Neutralized Bi-Directional Technique Supporting Dual-Polarized MIMO for 5G NR

22.1 A 769µW Battery-Powered Single-Chip SoC with BLE for Multi-Modal Vital Sign Health Patches

22.4 A 27.8µW Biopotential Amplifier Tolerant to 30Vpp Common-Mode Interference for Two-Electrode ECG Recording in 0.18µm CMOS

23.4 A 512GB 1.1V Managed DRAM Solution with 16GB ODP and Media Controller

25.3 A 128b AES Engine with Higher Resistance to Power and Electromagnetic Side-Channel Attacks Enabled by a Security-Aware Integrated All-Digital Low-Dropout Regulator

27.4 Multi-Beam Shared-Inductor Reconfigurable Voltage/SECE-Mode Piezoelectric Energy Harvesting of Multi-Axial Human Motion

28.1 A 0.42nW 434MHz -79.1dBm Wake-Up Receiver with a Time-Domain Integrator

29.2 A Scalable Quantum Magnetometer in 65nm CMOS with Vector-Field Detection Capability

29.4 Ultra-Low-Power Atomic Clock for Satellite Constellation with 2.2×10⁻¹² Long-Term Allan Deviation Using Cesium Coherent Population Trapping
# TIMETABLE OF ISSCC 2019 SESSIONS

## ISSCC 2019 • SUNDAY FEBRUARY 17TH

### Tutorials

<table>
<thead>
<tr>
<th>Time</th>
<th>Session</th>
<th>Title</th>
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</thead>
<tbody>
<tr>
<td>8:30 AM</td>
<td>T1</td>
<td>Fundamentals of Integrated Radars</td>
</tr>
<tr>
<td>10:30 AM</td>
<td>T4</td>
<td>Fundamentals of Efficient IoT Microcontrollers</td>
</tr>
<tr>
<td>1:30 PM</td>
<td>T7</td>
<td>Hardware Security – from Basics to ASICs</td>
</tr>
<tr>
<td>3:30 PM</td>
<td>T9</td>
<td>Calibration Techniques for Wireless Transceivers</td>
</tr>
<tr>
<td></td>
<td>T10</td>
<td>Low-Noise Sensor Interfaces</td>
</tr>
</tbody>
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### Forums

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<tr>
<th>Time</th>
<th>Forum</th>
<th>Title</th>
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</thead>
<tbody>
<tr>
<td>8:00 AM</td>
<td>F1</td>
<td>Sub-6GHz 5G Radio Circuits and Systems: From Concepts to Silicon</td>
</tr>
<tr>
<td></td>
<td>F2</td>
<td>Memory-Centric Computing from IoT to Artificial Intelligence and Machine Learning</td>
</tr>
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</table>

### Tutorials (Continued)

<table>
<thead>
<tr>
<th>Time</th>
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</thead>
<tbody>
<tr>
<td>8:30 AM</td>
<td>F3</td>
<td>The Complete Advanced Driver-Assistance System (ADAS) Sensing Network</td>
</tr>
<tr>
<td>10:30 AM</td>
<td>F4</td>
<td>Intelligence at the Edge: How Can We Make Machine Learning More Energy Efficient?</td>
</tr>
<tr>
<td>1:30 PM</td>
<td>F6</td>
<td>The Right Tool for the Job: Application-Optimized Data Converters</td>
</tr>
</tbody>
</table>

### Evenings Events

- EE1: Student Research Preview: Short Presentations with Poster Session
- EE2: How to Save Lives With Circuits
- EE3: Making a Career Choice
- EE4: Industry Showcase

## ISSCC 2019 • MONDAY FEBRUARY 18TH • Paper Sessions

### Session 1: Plenary Session

<table>
<thead>
<tr>
<th>Time</th>
<th>Session</th>
<th>Title</th>
</tr>
</thead>
<tbody>
<tr>
<td>8:30 AM</td>
<td>Session 2: Processors</td>
<td>Nyquist-Rate ADCs</td>
</tr>
<tr>
<td>1:30 PM</td>
<td>Session 4: Power Amplifiers</td>
<td>Image Sensors</td>
</tr>
</tbody>
</table>

### Evening Events

12noon to 7:00 PM – Book Displays • 5:00 PM to 7:00 PM – Demonstration Session • 5:15 PM – Author Interviews • Social Hour

### Session 3: Machine Learning

<table>
<thead>
<tr>
<th>Time</th>
<th>Session</th>
<th>Title</th>
</tr>
</thead>
<tbody>
<tr>
<td>8:30 AM</td>
<td>Session 8: DC-DC Converters</td>
<td>High-Frequency Transceivers for Radar and Communications</td>
</tr>
<tr>
<td>1:30 PM</td>
<td>Session 15: Power for 5G, Wireless Power, and GaN Converters</td>
<td>Frequency Synthesizers</td>
</tr>
</tbody>
</table>

### Evening Events

10:00 AM to 7:00 PM – Book Displays • 5:00 PM to 7:00 PM – Demonstration Session • 5:15 PM – Author Interviews • Social Hour

### Session 4: Analog Techniques

<table>
<thead>
<tr>
<th>Time</th>
<th>Session</th>
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<tbody>
<tr>
<td>8:30 AM</td>
<td>Session 19: Adaptive Digital &amp; Clocking Techniques</td>
<td>Noise-Shaped &amp; VCO-Based ADCs</td>
</tr>
<tr>
<td>1:30 PM</td>
<td>Session 25: Circuits Enabling Security</td>
<td>Frequency Generation &amp; Interference Mitigation</td>
</tr>
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</table>

### Evening Events

10:00 AM to 3:00 PM – Book Displays • 5:15 PM – Author Interviews

## ISSCC 2019 • WEDNESDAY FEBRUARY 20TH • Paper Sessions

### Session 5: Emerging Technologies

<table>
<thead>
<tr>
<th>Time</th>
<th>Session</th>
<th>Title</th>
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<tbody>
<tr>
<td>8:30 AM</td>
<td>Session 20: Noise-Shaped &amp; VCO-Based ADCs</td>
<td>4G/5G Transceivers</td>
</tr>
<tr>
<td>1:30 PM</td>
<td>Session 26: Frequency Generation &amp; Interference Mitigation</td>
<td>Techniques for Low-Power &amp; High-Performance Wireless</td>
</tr>
</tbody>
</table>

### Evening Events

10:00 AM to 3:00 PM – Book Displays • 5:15 PM – Author Interviews

## ISSCC 2019 • THURSDAY FEBRUARY 21ST

### Short Course

<table>
<thead>
<tr>
<th>Time</th>
<th>Title</th>
</tr>
</thead>
<tbody>
<tr>
<td>8:00 AM</td>
<td>Integrated Phased Arrays: Theory, Practice, and Implementation for 5G and Beyond</td>
</tr>
</tbody>
</table>

### Evening Events

10:00 AM to 11:00 PM – Book Displays • 5:15 PM – Author Interviews

## Events Below in Bold Box are Included with your Conference Registration

- EE3: Making a Career Choice
- EE4: Industry Showcase
EE5: “Moving to The Dark Side”

Many practicing engineers view management and business as ‘The Dark Side’, and executive decisions often baffle them. Can engineers do a good job on ‘The Dark Side’ in management and business? Is it possible to return to engineering from ‘The Dark Side’?

The relation between business and management on one side and engineering on the other side has always been complex. On one hand, innovative engineers often don’t understand the limitations imposed on them by more financially driven business managers. On the other hand, business needs solid engineering, within their budgetary boundaries, in order to be successful. Is it possible to transform from a good engineer to a good business manager? Can business managers return to engineering and be successful engineers after having spent time on ‘The Dark Side’? Can engineers and business managers peacefully coexist, and are they able to understand each other? Is that a situation we should work towards or, is a world where each side sees the other as a necessary evil perfectly balanced and sustainable?

In an entertaining and educational discussion between the panelists, the audience will get a closer look into the hearts and minds of Captains of Industry, sharing their views on the subject. How do they view the world after moving to ‘The Dark Side’ and have they truly moved to ‘The Dark Side’?

Join this panel discussion with active audience interaction, take a seat in the tribunal and make your vote count!

Moderator: Matt Straayer, Maxim, North Chelmsford, MA

Panelists

Anthony Collins, Xilinx, Dublin, Ireland
Kavé Kianush, Catena, Delft, The Netherlands
Curtis Ling, MaxLinear, Carlsbad, CA
Jen Lloyd, Analog Devices, San Jose, CA
Tyson Tuttle, Silicon Labs, Austin, TX
Patrick Yue, Hong Kong University of Science and Technology (HKUST), Hong Kong

EE6: “How Can Hardware Designers Reclaim the Spotlight?”

Gone seem the heady days when hardware innovation drove entrepreneurship in communications, computing, and other domains. The bar for circuit innovation and design has been inexorably climbing higher, even as circuit components are becoming increasingly commoditized and seemingly losing relevance in the larger scheme of things.

Is this trend here to stay? Should we do something about it? What should we do? Are long hardware design cycles to blame? Can we learn something from software design practices? Or, are there new opportunities where hardware innovation can still play a central role? If so, how far out is the horizon? How do we prepare for these opportunities?

This evening panel assembles a galaxy of international experts from academia, government, and both the hardware and software industries to discuss these issues. The experts will diagnose the situation, offer insightful prognoses, and engage in a lively discussion with each other, and with the audience. Come join us to see if you agree with our experts and for an opportunity to enlighten us with your opinion.

Moderator: Mike Shuo-Wei Chen, University of Southern California, Los Angeles, CA

Panelists

Luca Benini, ETH Zurich, Zurich, Switzerland, and Universita di Bologna, Bologna, Italy
Bill Dally, NVIDIA, Santa Clara, CA
Varada Gopalakrishnan, Amazon Lab126, Sunnyvale, CA
Colin Lyden, Analog Devices, Limerick, Ireland
Liam Madden, Xilinx, San Jose, CA
Andreas Olofsson, DARPA, Arlington, VA
Shaojun Wei, Tsinghua University, Beijing, China
Adaptive Digital & Clocking Techniques
Session Chair: John Maneatis, True Circuits, Los Alamos, CA
Associate Chair: Alicia Klinefelter, Nvidia, Durham, NC

8:30 AM
19.1 Computationally Enabled Total Energy Minimization Under Performance Requirements for a Voltage-Regulated 0.38-to-0.58V Microprocessor in 65nm CMOS
F. U. Rahman, R. Pamula, A. Boora, X. Sun, V. Sathe
University of Washington, Seattle, WA

9:00 AM
J. Lee¹, Y. Zhang¹, Q. Dong¹, W. Lim¹, M. Saligane¹, Y. Kim¹, S. Jeong¹, J. Lim¹, M. Yasuda², S. Miyoshi³, M. Kawaminami³, D. Blaauw¹, D. Sylvester¹
¹University of Michigan, Ann Arbor, MI
²Mie Fujitsu Semiconductor Limited, Kuwana, Japan
³Fujitsu Electronics America, Inc., Sunnyvale, CA

9:30 AM
19.3 A 7nm All-Digital Unified Voltage and Frequency Regulator Based on a High-Bandwidth 2-Phase Buck Converter with Package Inductors
F. I. Atallah¹, K. A. Bowman¹, H. H. Nguyen¹, J. Jeong¹, D. Yingling¹, Y. Sun¹, B. Appel¹, A. Polomik¹, M. Harinathi¹, J. Morelli¹, T. Moore², N. Reeves², A. Cassier², A. Raychoudhury¹
¹Qualcomm, Raleigh, NC; ²Qualcomm, San Diego, CA
³Georgia Institute of Technology, Atlanta, GA

Break 10:00 AM

10:15 AM
19.4 An Adaptive Clock Management Scheme Exploiting Instruction-Based Dynamic Timing Slack for a General-Purpose Graphics Processor Unit with Deep Pipeline and Out-of-Order Execution
T. Jia, R. Joseph, J. Gu, Northwestern University, Evanston, IL

10:45 AM
19.5 Digital Leakage Compensation for a Low-Power and Low-Jitter 0.5-to-5GHz PLL in 10nm FinFET CMOS Technology

11:15 AM
19.6 A 40-to-80MHz Sub-4µW/MHz ULV Cortex-M0 MCU SoC in 28nm FDSOI with Dual-Loop Adaptive Back-Bias Generator for 20µs Wake-Up From Deep Fully Retentive Sleep Mode
D. Bol¹, M. Schramme¹, L. Moreau¹, T. Haine¹, P. Xu¹, C. Frenkel¹, R. Dekimpe¹, F. Stas², D. Flandre²
¹UCLouvain, Louvain-la-Neuve, Belgium
²e-peas semiconductors, Louvain-la-Neuve, Belgium

11:45 AM
19.7 A Scalable Pipelined Time-Domain DTW Engine for Time-Series Classification Using Multibit Time Flip-Flops with 140Giga-Cell-Updates/s Throughput
Z. Chen, J. Gu, Northwestern University, Evanston, IL

Conclusion 12:15 PM
8:30 AM

20.1 A 5GS/s 7.2 ENOB Time-Interleaved VCO-Based ADC Achieving 30.5fJ/conv-step
M. Baert, W. Dehaene
KU Leuven, Heverlee, Belgium

9:00 AM

20.2 A 40MHz-BW 320MS/s Passive Noise-Shaping SAR ADC with Passive Signal-Residue Summation in 14nm FinFET
MediaTek, Hsinchu, Taiwan; *Equally-Credited Authors (ECAs)

9:30 AM

20.3 A 50MHz-Bandwidth 70.4dB-SNDR Calibration-Free Time-Interleaved 4th-Order Noise-Shaping SAR ADC
L. Jie, B. Zhang, M. P. Flynn
University of Michigan, Ann Arbor, MI

Break 10:00 AM

10:15 AM

20.4 An 8×-OSR 25MHz-BW 79.4dB/74dB DR/SNDR CT ΔΣ Modulator Using 7b Linearized Segmented DACs with Digital Noise-Coupling-Compensation Filter in 7nm FinFET CMOS
T-Y. Lo, C-H. Weng, H-Y. Hsieh, T-Y. Wang, Y-S. Shu, P-C. Chiu
MediaTek, Hsinchu, Taiwan

10:45 AM

20.5 A 76.6dB-SNDR 50MHz-BW 29.2mW Noise-Coupling-Assisted CT Sturdy MASH ΔΣ Modulator with 1.5b/4b Quantizers in 28nm CMOS
L. Qi⁴, A. Jain⁵, D. Jiang⁴, S-W. Sin⁴, R. P. Martins¹,³, M. Ortmanns²
¹University of Macau, Macau, China
³University of Ulm, Ulm, Germany
²Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

11:15 AM

20.6 An 80MHz-BW 31.9fJ/conv-step Filtering ΔΣ ADC with a Built-In DAC-Segmentation/ELD-Compensation 6b 960MS/s SAR-Quantizer in 28nm LP for 802.11ax Applications
C-Y. Wang, J-H. Tsai, S-Y. Su, J-C. Tsai, J-R. Chen, C-H. Lou
MediaTek, Hsinchu, Taiwan

11:45 AM

20.7 A 72.6dB-SNDR 100MHz-BW 16.36mW CTDSM with Preliminary Sampling and Quantization Scheme in Backend Subranging QTZ
W. Wang⁴, C-H. Chan⁴, Y. Zhu⁴, R. P. Martins¹,²
¹University of Macau, Macau, China
²Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

Conclusion 12:15 PM
4G/5G Transceivers

Session Chair: Yiwu Tang, Qualcomm Technologies, San Diego, CA
Associate Chair: Kyoo Hyun Lim, FCI, Seongnam, Korea

8:30 AM

21.1 A 28GHz CMOS Phased-Array Beamformer Utilizing Neutralized Bi-Directional Technique Supporting Dual-Polarized MIMO for 5G NR
J. Pang1, Z. Li1, R. Kubozen1, X. Luo1, R. Wu1, Y. Wang1, D. You1, A. A. Fadila1, R. Saengchan1, T. Nakamura1, J. Alvin1, D. Matsumoto1, A. T. Narayanan1, B. Liu1, J. Qiu1, H. Liu1, Z. Sun1, H. Huang1, K. K. Tokgoz1, K. Moto2, N. Oshima2, S. Hor2, K. Kunihiro2, T. Kaneko2, A. Shirane2, K. Okada2
1Tokyo Institute of Technology, Tokyo, Japan; 2NEC, Kawasaki, Japan

9:00 AM

21.2 A 27-to-41GHz MIMO Receiver with N-Input-N-Output Using Scalable Cascadable Autonomous Array-Based High-Order Spatial Filters for Instinctual Full-FoV Multi-Blocker/Signal Management
M-Y. Huang, H. Wang, Georgia Institute of Technology, Atlanta, GA

9:30 AM

21.3 A Reconfigurable Bidirectional 28/37/39GHz Front-End Supporting MIMO-TDD, Carrier Aggregation TDD and FDD/Full-Duplex with Self-Interference Cancellation in Digital and Fully Connected Hybrid Beamformers
S. Mondal, R. Singh, J. Paramesh, Carnegie Mellon University, Pittsburgh, PA

Break 10:00 AM

10:15 AM

21.4 An LTE-A Multimode Multiband RF Transceiver with 4RX/2TX Inter-Band Carrier Aggregation, 2-Carrier 4×4 MIMO with 256QAM and HPUE Capability in 28nm CMOS
C-C. Tang1, Y-B. Lee1, C-H. E. Sun1, C-C. Lin1, J-S. Syu1, M-H. Wu1, Y. Chen2, T-C. Chueh1, C. Bryant3, M. Collados3, M. Hassan3, J. Ramos3, Y-L. Hsieh1, H-H. Chen1, X. Guo1, H. Chen1, C. Cao1, D. Li1, J. Strange3, C. Wang4, G-K. Dehng1
1MediaTek, Hsinchu, Taiwan; 2MediaTek, San Diego, CA
3MediaTek, Kent, United Kingdom, 4MediaTek, Austin, TX

10:45 AM

21.5 A 5G Sub-6GHz Zero-IF and mm-Wave IF Transceiver with MIMO and Carrier Aggregation
B. Jann1, G. Chance2, A. Guha Roy1, A. Balakrishnan1, N. Karandikar1, T. Brown1, X. Li2, B. Davis3, J. L. Ceballos2, N. Tanz2, K. Hausmann2, H. Yoon2, Y-L. Huang2, A. Freiman4, B. Geren2, P. Pawliuk2, W. Ballantyne2
1Intel, Hillsboro, OR; 2Intel, Chandler, AZ; 3Intel, Villach, Austria
4Intel, Santa Clara, CA

11:15 AM

21.6 A Sub-6GHz 5G New Radio RF Transceiver Supporting EN-DC with 3.15Gb/s DL and 1.27Gb/s UL in 14nm FinFET CMOS
J. Lee, S. Han, J. Lee, B. Kang, J. Bae, J. Jang, S. Oh, S. Ahn, S. Kang, Q-D. Bui, K. Son, H. Lim, D. Jeong, R. Ni, Y. Zuo, I. Jong, C-W. Yao, S. Heo, T. B. Cho, I. Kang
Samsung Electronics, Hwaseong, Korea

11:45 AM

21.7 A Mixed-Signal Circuit Technique for Cancellation of Multiple Modulated Spurs in 4G/5G Carrier-Aggregation Transceivers
S. Sadjina1, K. Dufrière1, R. S. Kanumalli1, M. Huemer2, H. Prettl2
1Intel DMCE, Linz, Austria; 2Johannes Kepler University, Linz, Austria

Conclusion 12:15 PM
SESSION 22
Wednesday February 20th, 8:30 AM

Physiological Monitoring

Session Chair: Esther Rodriguez-Villegas, Imperial College, London, United Kingdom
Associate Chair: Rikky Muller, University of California, Berkeley, Berkeley, CA

8:30 AM

22.1 A 769µW Battery-Powered Single-Chip SoC with BLE for Multi-Modal Vital Sign Health Patches
M. Konijnenburg1, R. van Wegberg1, S. Song2, H. Ha1, W. Sijbers2, J. Xu1, S. Stanzione1, C. van Liempd1, D. Biswas2, A. Breeschooten1, P. Vis1, C. Van Hoof2,3, N. Van Helleputte4
1imec - Netherlands, Eindhoven, The Netherlands; 2imec, Leuven, Belgium; 3KU Leuven, Heverlee, Belgium

9:00 AM

22.2 A Rugged Wearable Modular ExG Platform Employing a Distributed Scalable Multi-Channel FM-ADC Achieving 101dB Input Dynamic Range and Motion-Artifact Resilience
J. Warchall1, P. Theilmann2, Y. Ouyang2, H. Garudadri1, P. P. Mercier1
1University of California, San Diego, La Jolla, CA; 2MaXentric Technologies, La Jolla, CA

9:30 AM

22.3 A 0.5V 9.26µW 15.28mΩ/√Hz Bio-Impedance Sensor IC with 0.55° Overall Phase Error
K. Kim, J-H. Kim, S. Gweon, J. Lee, M. Kim, Y. Lee, S. Kim, H-J. Yoo
KAIST, Daejeon, Korea

9:45 AM

22.4 A 27.8 μW Biopotential Amplifier Tolerant to 30Vpp Common-Mode Interference for Two-Electrode ECG Recording in 0.18µm CMOS
N. Koo, S. Cho
KAIST, Daejeon, Korea

Break 10:00 AM

10:15 AM

22.5 A Bio-Impedance Readout IC with Digital-Assisted Baseline Cancellation for 2-Electrode Measurement
H. Ha1, W. Sijbers2, R. van Wegberg1, J. Xu1, M. Konijnenburg1, P. Vis1, A. Breeschooten1, S. Song2, C. Van Hoof2,3, N. Van Helleputte4
1imec - Netherlands, Eindhoven, The Netherlands; 2imec, Leuven, Belgium; 3KU Leuven, Heverlee, Belgium

10:45 AM

22.6 A 13-Channel 1.53-mW 11.28-mm2 Electrical Impedance Tomography SoC Based on Frequency Division Multiplexing with 10× Throughput Reduction
B. Liu1,2, G. Wang1, Y. Li1, H. Li1, Y. Gao1, L. Zeng1, Y. Ma1, Y. Lian1, C. H. Heng2
1Shanghai Jiao Tong University, Shanghai, China; 2National University of Singapore, Singapore

11:15 AM

22.7 A Programmable Wireless EEG Monitoring SoC with Open/Closed-Loop Optogenetic and Electrical Stimulation for Epilepsy Control
National Cheng Kung University, Tainan, Taiwan

11:45 AM

22.8 Adaptively Clock-Boosted Auto-Ranging Responsive Neurostimulator for Emerging Neuromodulation Applications
1University of Toronto, Toronto, Canada; 2Krembil Neuroscience Center, Toronto, Canada; 3now at Envirosen, Toronto, Canada; 4now at Sitrus Technology, Irvine, CA; 5now at Princeton University, Princeton, NJ

*Equally-Credited Authors (ECAs)

Conclusion 12:15 PM
8:30 AM
23.1 A 7.5Gb/s/pin LPDDR5 SDRAM with WCK Clocking and Non-Target ODT for High Speed and with DVFS, Internal Data Copy, and Deep-Sleep Mode for Low Power
Samsung Electronics, Hwaseong, Korea

9:00 AM
23.2 A 1.1V 1ynn 6.4Gb/s/pin 16Gb DDR5 SDRAM with a Phase-Rotator-Based DLL, High-Speed SerDes and RX/TX Equalization Scheme
SK hynix, Icheon, Korea

9:30 AM
23.3 A 3-bit/2UI 27Gb/s PAM-3 Single-Ended Transceiver Using One-Tap DFE for Next-Generation Memory Interface
H. Park\(^1\), J. Song\(^2\), Y. Lee\(^1\), J. Sim\(^1\), J. Choi\(^1\), C. Kim\(^1\)
\(^1\)Korea University, Seoul, Korea
\(^2\)Incheon National University, Incheon, Korea

9:45 AM
23.4 A 512GB 1.1V Managed DRAM Solution with 16GB ODP and Media Controller
SK hynix, Icheon, Korea

Break 10:00 AM
SRAM & Computation-in-Memory
Session Chair: Shinichiro Shiratake, Toshiba Memory, Yokohama, Japan
Associate Chair: Kyu-hyoun Kim, IBM T.J. Watson, Yorktown Heights, NY

10:15 AM
24.1 A 1Mb Multibit ReRAM Computing-In-Memory Macro with 14.6ns Parallel MAC Computing Time for CNN-Based AI Edge Processors
National Tsing Hua University, Hsinchu, Taiwan

10:45 AM
24.2 A 7nm 2.1GHz Dual-Port SRAM with WL-RC Optimization and Dummy-Read-Recovery Circuitry to Mitigate Read-Disturb-Write Issue
TSMC, Hsinchu, Taiwan

11:15 AM
24.3 A Voltage and Temperature Tracking SRAM Assist Supporting 740mV Dual-Rail Offset for Low-Power and High-Performance Applications in 7nm EUV FinFET Technology
Samsung Electronics, Hwaseong, Korea

11:30 AM
24.4 Sandwich-RAM: An Energy-Efficient In-Memory BWN Architecture with Pulse-Width Modulation
J. Yang1, Y. Kong1, Z. Wang1, Y. Liu1, B. Wang1, S. Yin1, L. Shi1
1Southeast University, Nanjing, China
2Boxing Electronics, Nanjing, China
3Tsinghua University, Beijing, China

11:45 AM
24.5 A Twin-8T SRAM Computation-In-Memory Macro for Multiple-Bit CNN-Based Machine Learning
X. Si2, J-J. Chen1, Y-N. Tu1, W-H. Huang1, J-H. Wang1, W-C. Wei1, S-Y. Wu1, X. Sun2, R. Liu3, S. Yu4, R-S. Liu4, C-C. Hsieh4, K-T. Tang4, Q. Lfäther4, M-F. Chang
1National Tsing Hua University, Hsinchu, Taiwan
2University of Electronic Science and Technology of China, Chengdu, China
3Arizona State University, Tempe, AZ
4Georgia Institute of Technology, Atlanta, GA

Conclusion 12:15 PM
Circuits Enabling Security

Session Chair: Hirofumi Shinohara, Waseda University, Kitakyushu, Japan
Associate Chair: Dennis Sylvester, University of Michigan, Ann Arbor, MI

1:30 PM
25.1 A 562F² Physically Unclonable Function with a Zero-Overhead Stabilization Scheme
D. Li, K. Yang
Rice University, Houston, TX

2:00 PM
25.2 A Reconfigurable RRAM Physically Unclonable Function Utilizing Post-Process Randomness Source with <6×10⁻⁶ Native Bit Error Rate
Y. Pang¹, B. Gao¹, D. Wu¹, S. Yi¹, Q. Liu¹, W-H. Chen², T-W. Chang³, W-E. Lin², X. Sun², S. Yu², H. Qian¹, M-F. Chang², H. Wu¹
¹Tsinghua University, Beijing, China
²National Tsing Hua University, Hsinchu, Taiwan
³Georgia Institute of Technology, Atlanta, GA

2:30 PM
25.3 A 128b AES Engine with Higher Resistance to Power and Electromagnetic Side-Channel Attacks Enabled by a Security-Aware Integrated All-Digital Low-Dropout Regulator
A. Singh¹, M. Kar², S. Mathew², A. Rajan², V. De², S. Mukhopadhyay³
¹Georgia Institute of Technology, Atlanta, GA
²Intel, Hillsboro, OR

Break 3:00 PM
SESSION 26                  Wednesday February 20th, 3:15 PM

Frequency Generation & Interference Mitigation
Session Chair: Ramesh Harjani, University of Minnesota, Minneapolis, MN
Associate Chair: Andrea Mazzanti, Università degli Studi di Pavia, Pavia, Italy

3:15 PM
26.1 A Self-Calibrated 16GHz Subsampling-PLL-Based 30µs Fast Chirp FMCW
Modulator with 1.5GHz Bandwidth and 100kHz rms Error
Q. Shi¹, K. Bunsen², N. Markulic¹, J. Craninckx¹
¹imec, Heverlee, Belgium
²Sony Semiconductor Solutions, Atsugi, Japan

3:45 PM
26.2 A 0.08mm² 25.5-to-29.9GHz Multi-Resonant-RLCM-Tank VCO Using a
Single-Turn Multi-Tap Inductor and CM-Only Capacitors Achieving
191.6dBc/Hz FoM and 130kHz 1/f³ PN Corner
H. Guo¹, Y. Chen¹, P-I. Mak¹, R. P. Martins¹,²
¹University of Macau, Macau, China
²Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

4:15 PM
26.3 A 25-to-38GHz, 195dB FoM LC QVCO in 65nm LP CMOS Using a 4-Port
Dual-Mode Resonator for 5G Radios
A. Bhat, N. Krishnapura
Indian Institute of Technology Madras, Chennai, India

4:30 PM
26.4 A 2.4GHz 65nm CMOS Mixer-First Receiver Using 4-Stage Cascaded
Inverter-Based Envelope-Biased LNAs Achieving 66dB In-Band
Interference Tolerance and -83dBm Sensitivity
D. Ye¹, R. Xu¹, C-J. R. Shi¹,²
¹Fudan University, Shanghai, China
²University of Washington, Seattle, WA

5:00 PM
26.5 A 0.1-to-0.2V Transformer-Based Switched-Mode Folded DCO in 22nm
FDSOI with Active Step-Down Impedance Achieving 197dBc/Hz Peak FoM
and 40MHz/V Frequency Pushing
O. El-Aassar, G. M. Rebeiz
University of California, San Diego, La Jolla, CA

Conclusion 5:15 PM
Energy Harvesting & DC/DC Control Techniques

Session Chair: Yuan Gao, Institute of Microelectronics, Singapore
Associate Chair: Chan-Hong Chern, TSMC, Hsinchu, Taiwan

1:30 PM

27.1 An 84% Peak Efficiency Bipolar-Input Boost/Flyback Hybrid Converter with MPPT and On-Chip Cold Starter for Thermoelectric Energy Harvesting
P. Cao¹, Y. Qian¹, P. Xue¹, D. Lv², J. He³, Z. Hong¹
¹Fudan University, Shanghai, China; ²Analog Devices, Shanghai, China

2:00 PM

27.2 An Adiabatic Sense and Set Rectifier for Improved Maximum-Power-Point Tracking in Piezoelectric Harvesting with 541% Energy Extraction Gain
University of Michigan, Ann Arbor, MI

2:30 PM

27.3 A Piezoelectric Energy-Harvesting Interface Using Split-Phase Flipping-Capacitor Rectifier and Capacitor Reuse Multiple-VCR SC DC-DC Achieving 9.3x Energy-Extraction Improvement
Z. Chen¹,², Y. Jiang¹, M-K. Law¹, P-I. Mak¹, X. Zeng³, R. P. Martins¹,³
¹University of Macau, Macau, China; ²Fudan University, Shanghai, China
³Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

2:45 PM

27.4 Multi-Beam Shared-Inductor Reconfigurable Voltage/SECE-Mode Piezoelectric Energy Harvesting of Multi-Axial Human Motion
M. Meng¹, A. Ibrahim¹, T. Xue², H. G. Yeo³, D. Wang¹, S. Roundy²,
S. Trolier-McKinstry¹, M. Kiani³
¹Pennsylvania State University, University Park, PA
²University of Utah, Salt Lake City, UT
³Daegu- Gyeongbuk Institute of Science and Technology, DaeguKorea

3:15 PM

27.5 A 91%-Efficiency Envelope-Tracking Modulator Using Hysteresis-Controlled Three-Level Switching Regulator and Slew-Rate-Enhanced Linear Amplifier for LTE-80MHz Applications
P. Mahmoudidaryan, D. Mandal, B. Bakkaloglu, S. Kiaei
Arizona State University, Tempe, AZ

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27.6 Background Capacitor-Current-Sensor Calibration of DC-DC Buck Converter with DVS for Accurately Accelerating Load-Transient Response
T-H. Kuo, Y-W. Huang, P-Y. Wang, National Cheng Kung University, Tainan, Taiwan

4:15 PM

27.7 A Synthesizable Digital AOT 4-Phase Buck Voltage Regulator for Digital Systems with 0.0054mm² Controller and 80ns Recovery Time
M. Choi¹,², C-H. Kye¹, J. Oh¹, M-S. Choo¹, D-K. Jeong¹
¹Seoul National University, Seoul, Korea; ²Samsung Electronics, Hwaseong, Korea

4:45 PM

27.8 Dynamic-Charging Current-Scaling Technique with Dual Accurate Current Control and Temperature Loops with Charging-CURRENT Accuracy up to 99.6% for 1.6x Faster Lithium-Ion Battery Charging
W-T. Lin¹, Z-Y. Lin¹, C-H. Liu¹, C-M. Huang¹, L-C. Chu¹, K-H. Chen¹, Y-H. Lin²,
S-R. Lin², T-Y. Tsai², H-H. Tsai², Y-Z. Juang¹
¹National Chiao Tung University, Hsinchu, Taiwan; ²Realtek Semiconductor, Hsinchu, Taiwan

Conclusion 5:15 PM
Techniques for Low-Power & High-Performance Wireless

Session Chair: Danielle Griffith, Texas Instruments, Dallas, TX
Associate Chair: Alan Wong, EnSilica, Abingdon, United Kingdom

1:30 PM

28.1 A 0.42nW 434MHz -79.1dBm Wake-Up Receiver with a Time-Domain Integrator
V. Mangal, P. R. Kinget, Columbia University, New York, NY

2:00 PM

28.2 A 220μW -85dBm Sensitivity BLE-Compliant Wake-up Receiver Achieving -60dB SIR via Single-Die Multi-Channel FBAR-Based Filtering and a 4-Dimensional Wake-Up Signature
P-H. P. Wang, P. P. Mercier, University of California, San Diego, La Jolla, CA

2:30 PM

28.3 A 606µW mm-Scale Bluetooth Low-Energy Transmitter Using Co-Designed 3.5×3.5mm² Loop Antenna and Transformer-Boost Power Oscillator
University of Michigan, Ann Arbor, MI

2:45 PM

28.4 A High-Q Resonant Inductive Link Transmit Modulator/Driver for Enhanced Power and FSK/PSK Data Transfer Using Adaptive-Predictive Phase-Continuous Switching Fractional-Capacitance Tuning
H. Kennedy, R. Bodnar, T. Lee, W. Redman-White
University of Southampton, Southampton, United Kingdom

Break 3:00 PM

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28.5 Non-Magnetic 60GHz SOI CMOS Circulator Based on Loss/Dispersion-Engineered Switched Bandpass Filters
A. Nagulu, H. Krishnaswamy, Columbia University, New York, NY

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28.6 Full-Duplex 2×2 MIMO Circulator-Receiver with High TX Power Handling Exploiting MIMO RF and Shared-Delay Baseband Self-Interference Cancellation
M. Baraani Dastjerdī, S. Jain, N. Reiskarimian, A. Natarajan, H. Krishnaswamy
1Columbia University, New York, NY; 2Oregon State University, Corvallis, OR

4:15 PM

28.7 A Wideband Blocker-Tolerant Receiver with High-Q RF-Input Selectivity and <-80dBm LO Leakage
H. Wang, Z. Wang, P. Heydari, University of California, Irvine, CA

4:45 PM

28.8 A 21dBm-OP 1dB 20.3%-Efficiency -131.8dBm/Hz-Noise X-band Cartesian-Error-Feedback Transmitter with Fully Integrated Power Amplifier in 65nm CMOS
J. Li, Z. Xu, Q. J. Gu
1University of California, Davis, CA; 2Zhejiang University, Hangzhou, China

Conclusion 5:15 PM
Quantum & Photonics Technologies
Session Chair: Edoardo Charbon, EPFL, Neuchatel, Switzerland
Associate Chair: Pui-In Mak, University of Macau, Macau, China
1:30 PM
29.1 A 28nm Bulk-CMOS 4-to-8GHz <2mW Cryogenic Pulse Modulator for Scalable Quantum Computing
1University of Massachusetts, Amherst, MA; 2Google, Goleta, CA
3University of California, Santa Barbara, CA; 4Google, Los Angeles, CA

2:00 PM
29.2 A Scalable Quantum Magnetometer in 65nm CMOS with Vector-Field Detection Capability
M. I. Ibrahim, C. Fay, D. R. Englund, R. Han
Massachusetts Institute of Technology, Cambridge, MA

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29.3 A 48GHz 5.6mW Gate-Level-Pipelined Multiplier Using Single-Flux Logic
I. Nagaoka1, M. Tanaka1, K. Inoue2, A. Fujimaki1
1Nagoya University, Nagoya, Japan; 2Kyushu University, Fukuoka, Japan

Break 3:00 PM

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29.4 Ultra-Low-Power Atomic Clock for Satellite Constellation with 2.2×10-12 Long-Term Allan Deviation Using Cesium Coherent Population Trapping
H. Zhang1, H. Herdian1, A. T. Narayanan1, A. Shirane1, M. Suzuki2, K. Harasaka2, K. Adachi2, S. Yanagimachi3, K. Okada1
1Tokyo Institute of Technology, Tokyo, Japan; 2Ricoh, Miyagi, Japan
3National Institute of Advanced Industrial Science and Technology, Ibaraki, Japan

3:45 PM
29.5 A Single-Chip Optical Phased Array in a 3D-Integrated Silicon Photonics/65nm CMOS Technology
1University of California, Berkeley, CA; 2Massachusetts Institute of Technology, Cambridge, MA
3Colleges of Nanoscale Science and Engineering, Albany, NY

4:15 PM
29.6 A Digital-Type GaN Driver with Current-Pulse-Balancer Technique Achieving Sub-Nanosecond Current Pulse Width for High-Resolution and Dynamic Effective Range LiDAR System
Y-S. Ma1, Z-Y. Lin1, Y-T. Lin1, C-Y. Lee1, T-P. Huang1, K-H. Chen2, Y-H. Lin2, S-R. Lin2, T-Y. Tsai2
1National Chiao Tung University, Hsinchu, Taiwan; 2Realtek Semiconductor, Hsinchu, Taiwan

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29.7 A 500Mb/s -46.1dBm CMOS SPAD Receiver for Laser Diode Visible-Light Communications
J. Kosman1,2, O. Almer1, T. Al Abbas1, N. Dutton2, R. Walker2, S. Videv2, K. Moore2, H. Haas2, R. Henderson2
1University of Edinburgh, Edinburgh, United Kingdom; 2STMicroelectronics, Edinburgh, United Kingdom; 3Photon Force, Edinburgh, United Kingdom

5:00 PM
29.8 SHARC: Self-Healing Analog with RRAM and CNFETs
A. G. Amer, R. Ha, G. Hills, A. P. Chandrakasan, M. M. Shulaker
Massachusetts Institute of Technology, Cambridge, MA

Conclusion 5:15 PM
Advanced Wireline Techniques

Session Chair: Yohan Frans, Xilinx, San Jose, CA
Associate Chair: Friedel Gerfers, Technische Universität Berlin, Berlin, Germany

1:30 PM

30.1 Single-Pair Automotive PHY Solutions from 10Mb/s to 10Gb/s and Beyond
G. W. den Besten, NXP Semiconductors, Eindhoven, The Netherlands

2:00 PM

30.2 A 161mW 56Gb/s ADC-Based Discrete Multitone Wireline Receiver Data-Path in 14nm FinFET
G. Kim1,2, L. Kuif3, D. Luu4, M. Braendiff2, C. Menolfif2, P-A. Francese6, H. Yuke6, C. Apri1,2, T. Morf1, M. Kosseif1, A. Cevo6, I. Ozkaya5, A. Burg7, T. Tolff1, Y. Leblebicil
1EPFL, Lausanne, Switzerland; 2IBM Zurich Research Laboratory, Rüschlikon, Switzerland
3*now with KAIST, Daejeon, Korea; 4ETH Zürich, Zurich, Switzerland
5IBM T. J. Watson Research Center, Yorktown Heights, NY

2:30 PM

30.3 A 25.6Gb/s Uplink-Downlink Interface Employing PAM-4-Based 4-Channel Multiplexing and Cascaded CDR Circuits in Ring Topology for High-Bandwidth and Large-Capacity Storage Systems
Toshiba Memory, Kawasaki, Japan

Break 3:00 PM

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30.4 A 32Gb/s 2.9pJ/b Transceiver for Sequence-Coded PAM-4 Signalling with 4-to-6dB SNR Gain in 28nm FDSOI CMOS
Aurangzeb1, C. Dick1, M. Mohammed1, M. Hossain1
1University of Alberta, Edmonton, Canada; 2Intel, Santa Clara, CA

3:45 PM

30.5 A 1.41pJ/b 56Gb/s PAM-4 Wireline Receiver Employing Enhanced Pattern Utilization CDR and Genetic Adaptation Algorithms in 7nm CMOS
S. Shahramian1, B. Dehlaghi1, J. Liang7, R. Bespalko1, D. Dunwell1, J. Bailey1, B. Wang1, A. Sharif-Bakhtiar1, M. O’Farrell1, K. Tang1, A. Chan Carusone2, D. Cassan1, D. Tonietto3
1Huawei Technologies, Toronto, Canada; 2University of Toronto, Toronto, Canada
3Elenion Technologies, New York, NY

4:15 PM

30.6 A 6V Swing 3.6% THD >40GHz Driver with 4.5x Bandwidth Extension for a 272Gb/s Dual-Polarization 16-QAM Silicon Photonic Transmitter
1University of British Columbia, Vancouver, Canada; 2Elenion Technologies, New York, NY

4:30 PM

30.7 An 8b Injection-Locked Phase Rotator with Dynamic Multiphase Injection for 28/56/112Gb/s Serdes Application
Y-C. Huang, B-J. Chen, MediaTek, Hsinchu, Taiwan

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30.8 A 0.65V 12-to-16GHz Sub-Sampling PLL with 56.4fsrms Integrated Jitter and -256.4dB FoM
Z. Zhang, G. Zhu, C. P. Yue, Hong Kong University of Science and Technology, Hong Kong, China

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30.9 A 140fsrms-Jitter and -72dBc-Reference-Spur Ring-VCO-Based Injection-Locked Clock Multiplier Using a Background Triple-Point Frequency/Phase/Slope Calibrator
S. Yoo, S. Choi, Y. Lee, T. Seong, Y. Lim, J. Choi
Ulsan National Institute of Science and Technology, Ulsan, Korea

Conclusion 5:15 PM
Short Course: Integrated Phased Arrays: Theory, Practice, and Implementation for 5G and Beyond

Time: Topic:
8:00 AM Breakfast
8:20 AM Introduction by Chair, Daniel Friedman
IBM Thomas J. Watson Research Center, Yorktown Heights, NY
8:30 AM Introduction to Phased-Array Technology from mm-Wave to Optics
Hossein Hashemi, University of Southern California, Los Angeles, CA
10:00 AM Break
10:30 AM Scalable mm-Wave Phased Arrays for Imaging and 5G Communications
Bodhisatwa Sadhu, IBM T. J. Watson Research Center, Yorktown Heights, NY
12:15 PM Lunch
1:20 PM Challenges and Architectures for Large-Scale Next-Generation Phased Arrays and 5G Systems
Shahriar Shahramian, Nokia, Murray Hill, NJ
2:50 PM Break
3:20 PM Emerging Topics in Phased Arrays and the Path to THz
Ehsan Afshari, University of Michigan, Ann Arbor, MI
4:50 PM Conclusion

Introduction
Phased array technology is a staple in specialized radar and long reach communications applications. With the rise of mmWave circuits and associated dense packaging, integrated, scalable phased arrays are key technology elements in a new wave of emerging broad-based commercial applications in the communication and imaging spaces. In this short course, we first introduce the concept of electronically steered arrays, describe how to analyze such designs, discuss analog, digital, and hybrid beamforming phased array tradeoffs, and introduce both mmWave and optical examples. We next discuss some of the key circuits enabling these designs, scalability of such designs, and emerging opportunities for systems leveraging these designs. We continue with a discussion of paths to realizing very large scale arrays, including physical design, packaging, verification, and test. Finally, we conclude with a discussion of emerging topics in phased arrays and the opportunities for even higher radio frequency phased array solutions.
SC1: Introduction to Phased-Array Technology from mm-Wave to Optics
Hossein Hashemi, University of Southern California, Los Angeles, CA

This talk will cover the basic principles, architectures, applications, and associated building blocks of phased arrays from radio frequencies up to optical frequencies.

Hossein Hashemi is a Professor of Electrical Engineering at the University of Southern California. His research interests include analog, mixed-signal, radio-frequency and photonic integrated circuits. He received the B.S. and M.S. degrees in Electronics Engineering from the Sharif University of Technology, Tehran, Iran, in 1997 and 1999, respectively, and the M.S. and Ph.D. degrees in Electrical Engineering from the California Institute of Technology, Pasadena, in 2001 and 2003, respectively. Hossein is an Associate Editor for the IEEE Journal of Solid state Circuits. He was a co-recipient of the 2004 IEEE Journal of Solid-State Circuits Best Paper Award and the 2007 IEEE ISSCC Lewis Winner Award for Outstanding Paper.

SC2: Scalable mm-Wave Phased Arrays for Imaging and 5G Communications
Bodhisatwa Sadhu, IBM T. J. Watson Research Center, Yorktown Heights, NY

Large numbers of millimeter-wave antenna elements (typically from 10s to 100s) can be supported using multiple integrated circuits (ICs) that are further integrated at the package level to create a phased-array module. This talk motivates the need for millimeter-wave phased-array scaling to realize such large apertures and outlines key challenges toward their implementation. Various aspects of phased array scaling, including beamforming architectures and functional partitioning, signal distribution among multiple ICs, module-level implementation of antennas and packaging, and digital control will be discussed. Two recently introduced scaled 64-element dual-polarized phased array designs will be reviewed as implementation examples: 1) A phased-array transceiver module operating at 28GHz supporting 5G applications, and 2) TX and RX phased arrays operating at 94GHz, suitable for backhaul and imaging applications. Design techniques implementing requirements relevant to these applications will be discussed, and measurement results validating the designs will be presented. Finally, an emerging approach to managing the rich control space associated with highly integrated phased-array designs will be discussed.

Bodhisatwa Sadhu is currently a Research Staff Member at IBM T. J. Watson Research Center. He received the Ph.D. degree in Electrical Engineering from University of Minnesota, Minneapolis, in 2012, working on cognitive radio circuits. Since 2012, Dr. Sadhu has been working on RF and mm-wave transceivers at IBM T. J. Watson Research, where he has led the design and demonstration of a self-healing frequency synthesizer, a low-power 60GHz transceiver IC, and a mm-wave 5G phased array base-station IC. In the last five years, he has authored and co-authored 10+ journal papers, 20+ conference papers, and a book on cognitive radio circuits, and holds 20 issued US patents with 20+ pending. He is currently an Adjunct Assistant Professor at Columbia University, serves as a TPC member of the IEEE RFIC Symposium and IEEE BCICTS, and a guest editor of IEEE JSSC. Dr. Sadhu is the recipient of the 2017 ISSCC Lewis Winner Award for Outstanding Paper, the 2017 Pat Goldberg Memorial Award for the best paper in computer science, electrical engineering, and mathematics published by IBM Research, two IBM A-level Accomplishment awards, six IBM Patent Plateau Awards, the University of Minnesota Graduate School Fellowship in 2007, the 3M Science and Technology Fellowship in 2009, the University of Minnesota Doctoral Dissertation Fellowship in 2011, and stood 2nd in India in the Indian School Certificate (ISC) examination in 2003. He was recognized as an IBM Master Inventor in 2017.
SC3: Challenges and Architectures for Large-Scale Next-Generation Phased Arrays and 5G Systems

Shahriar Shahramian, Nokia, Murray Hill, NJ

The wireless communications industry is at the verge of an exciting transformation: a shift from broadcast-mode to directed-beam communication in the form of large-scale mm-wave phased arrays. In order to enable mass deployment of phased array systems, every layer of our future networks must undergo a transformation. This workshop discusses the challenges associated with the design and architecture of mm-wave phased-array systems up to and beyond the W-band. The impact of technology, circuit topology and chipset architecture on the overall system is examined alongside state-of-the-art reported communication platforms. Furthermore, packaging, calibration and cost reductions techniques are explored.

Shahriar Shahramian received his Ph.D. degree from University of Toronto in 2010, where he focused on the design of mm-wave data converters and transceivers. Dr. Shahramian has been with the Bell Laboratories division of Alcatel-Lucent (now Nokia), Murray Hill, NJ, since 2009 and is currently the Director of the mm-Wave ASIC Research Department. He is also a member of the technical program committee of the IEEE Compound Semiconductor Integrated Circuits Symposium (CSICS) and the IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS). He is also a guest Editor of the IEEE Journal of Solid-State Circuits (JSSC). His research focus includes the design of mm-wave wireless and wireline integrated circuits. He is the lead designer of several state-of-the-art ASICs for optical coherent and wireless backhaul products at Bell Laboratories.

Dr. Shahramian has been the recipient of Ontario Graduate Scholarship, University of Toronto Fellowship and the Best Paper Award at the CSICS Symposium in 2005, 2015, and the RFIC Symposium in 2015. He also holds an Adjunct Associate Professor position at Columbia University, has received several teaching awards, and is the founder and host of The Signal Path educational video series.

SC4: Emerging Topics in Phased Arrays and the Path to THz

Ehsan Afshari, University of Michigan, Ann Arbor, MI

The design and implementation of phased arrays at mmWave and THz frequencies has several challenges, including loss of passives, phase mismatch, limited efficiency of active devices, and the antenna implementation. In this short course, we demonstrate that as we get closer to the cut-off frequency of transistors, new approaches that combine the device physics, circuit techniques, and EM theory are needed. We will discuss several scalable phased arrays for communication and radar applications.

Ehsan Afshari received his Ph.D. in Electrical Engineering from Caltech in 2006, and joined the ECE Department of Cornell University. Ten years later, he joined the EECS department of the University of Michigan, Ann Arbor. His team is engaged in the theoretical foundations, design and experimental validation of analog, RF, mm-wave, and THz integrated devices, circuits and systems for a variety of applications, including communications, imaging and sensing. His work is funded by federal agencies, such the NSF, DARPA, ONR, and the ARL, as well as companies like Intel, TI, Raytheon, and Qualcomm. He has been the recipient of several awards and honors, including a 2008 DARPA Young Faculty Award, a 2010 NSF CAREER Award, a first place at the Stanford-Berkeley-Caltech Innovation Challenge in 2005, and several best paper awards at the leading conferences in his field. He has also served as a Distinguished Lecturer for the IEEE Solid-State Circuits Society. He was selected as one of the 50 most distinguished alumni of Sharif University. His doctoral students have also received several prestigious awards and fellowships, including: 2018, 2017, 2012, 2011, and 2010 Solid-State Circuit Society Predoctoral Achievement Award; 2011, 2013, and 2017 IEEE MTT-S Microwave Engineering Graduate Fellowships; the Cornell Best Ph.D. Thesis Award in 2011 and 2014; as well as many best paper awards. The Ph.D. graduates of his group are leaders in the field, including faculty members at MIT, UC Davis and the University of Minnesota, and companies such as IBM, Bell Labs, Qualcomm and Broadcom.
As the automotive industry continues its intensive commercial and R&D drive towards ever more sophisticated advanced driver-assistance systems, the focus on sensor quality, reliability and security has never been greater. Such systems comprise a multi-sensor network and decision engine capable of processing high volumes of data, in real-time to take safety critical, vehicle actions. In this forum, we will review the ADAS system and the requirements of OEMs and system integrators before presentations on state-of-the-art automotive sensors covering CIS, inertial sensors, LiDAR, RADAR and ultrasonics.

**Forum Agenda**

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<td>8:00 AM</td>
<td>Breakfast</td>
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| 8:20 AM | Introduction  
Bruce Rae, STMicroelectronics, Edinburgh, United Kingdom                               |
| 8:30 AM | Overview of ADAS Systems  
Patrick Denny, Valeo, Galway, Ireland                                                       |
| 9:20 AM | ADAS - AV Central Processing Hub  
Richard Bramley, Nvidia, Santa Clara, CA                                                   |
| 10:10 AM| Break                                                                                     |
| 10:30 AM| Intelligent Sensors for Autonomous Driving  
Sergey Velichko, ON Semiconductor, Meridian, ID                                               |
| 11:20 AM| Achieving High-Performance and Robustness: Technologies for Automotive MEMS Gyroscopes  
Deyou Fang, STMicroelectronics, Coppell, TX                                                |
| 12:10 PM| Lunch                                                                                     |
| 1:10 PM | LiDAR Sensor Systems  
Ming Wu, UC Berkeley, Berkeley, CA                                                        |
| 2:00 PM | The Evolving Landscape in Automotive Radars: Waveform, System Implementation, and IC Technologies  
Cicero Vaucher, NXP Semiconductor, Eindhoven, The Netherlands |
| 2:50 PM | Break                                                                                     |
| 3:10 PM | Ultrasonic Sensors and Their Role in ADAS  
Ajit Sharma, Texas Instruments, Dallas, TX                                                   |
| 4:00 PM | Battery Management IC Design Complying with Functional Safety  
Pieter De Muyter, ICsence, Leuven, Belgium                                                   |
| 4:50 PM | Conclusion                                                                                |
Deep learning algorithms mainly used today in Machine Learning applications are very costly in terms of energy consumption, due to their large amount of required computations and large model sizes. Many issues like connectivity to the cloud, latency, privacy, and public safety could be resolved by establishing intelligent computing at the edge. This forum brings together architecture, circuit, and integrated design solutions to minimize the energy consumption of edge learning systems. Various approaches from different perspectives will be covered: neuro-inspired architectures, in memory computation, embedded sensing, and spiking neural networks.

### Forum Agenda

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<td>8:00 AM</td>
<td>Breakfast</td>
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<td>8:20 AM</td>
<td>Introduction</td>
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<td><strong>Masato Motomura</strong>, Hokkaido University, Sapporo, Japan</td>
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<tr>
<td>8:30 AM</td>
<td>Enabling Embedded Intelligence: Application, Architecture and Design Solutions</td>
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<td><strong>Bert Moons</strong>, Synopsys, Leuven, Belgium</td>
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<td>9:20 AM</td>
<td>Mixed-Signal Circuits for Inference at the Edge</td>
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<td><strong>Daniel Bankman</strong>, Stanford University, Stanford, CA</td>
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<td>10:10 AM</td>
<td>Break</td>
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<tr>
<td>10:30 AM</td>
<td>Processing Data Where It Makes Sense in Modern Computing Systems:</td>
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<td>Enabling In-Memory Computation</td>
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<td><strong>Onur Mutlu</strong>, ETH Zurich, Zurich, Switzerland</td>
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<tr>
<td>11:20 AM</td>
<td>Bandwidth-Efficient Deep Learning with Algorithm and Hardware Co-Design</td>
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<td><strong>Song Han</strong>, Massachusetts Institute of Technology, Cambridge, MA</td>
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<td>12:10 PM</td>
<td>Lunch</td>
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<td>1:10 PM</td>
<td>On-Chip Epilepsy Detection: Where Machine Learning Enables Patient-Specific Pervasive Healthcare</td>
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<td><strong>Jerald Yoo</strong>, National University of Singapore, Singapore</td>
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<td>2:00 PM</td>
<td>Applying Principles of Neural Computation for Efficient Learning in Silicon</td>
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<td><strong>Mike Davies</strong>, Intel Labs, Hillsboro, OR</td>
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<td>2:50 PM</td>
<td>Break</td>
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<td>3:10 PM</td>
<td>Energy-Efficient Deep Learning for Intelligent Embedded Systems</td>
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<td><strong>Nitin Chawla</strong>, ST Microelectronics, Greater Noida, India</td>
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<td>4:00 PM</td>
<td>Energy-Efficient Intelligent Vision Sensor for Next Generation Mobile and Autonomous Applications</td>
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<td><strong>Eric Ryu</strong>, Samsung Electronics, Hwasung, Korea</td>
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<td>4:50 PM</td>
<td>Conclusion</td>
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</tbody>
</table>
This forum brings together experts from the forefront of all areas in the design of high-speed wireline SerDes. The talks will take you through a detailed review of current and next generation serial link designs and the associated challenges in each area, as well as where the industry and roadmap maybe heading beyond 112Gb/s.

The forum is a circuit- and algorithm-oriented review of high-performance transceivers, focussing on all aspects of SerDes design including analog front-end circuits, high-speed ADC design for receivers, high-speed DAC design for transmitters, clock-and-data recovery techniques, wide-range PLLs and clocking, and adaptive equalization. Talks include the Forward Error Correction techniques that are essential for the future and those that are currently employed, as well as the error statistics and how solutions can be tailored around them. Short-reach links and their challenges are included, as well as longer-reach backplane links, together with the modeling techniques used with IBIS AMI for the verification of how well they will operate in practise. Finally, some non-standard techniques are also discussed to solving the bandwidth limitation problem.

**Forum Agenda**

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<th>Time</th>
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<td>Breakfast</td>
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<td>8:15 AM</td>
<td>Introduction, Andrew Joy, Cavium, Northampton, United Kingdom</td>
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<td>9:05 AM</td>
<td>ADCs for High-Speed Communication - Architectures and Circuit Implementations Filip Tavernier, KU Leuven, Leuven, Belgium</td>
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<tr>
<td>9:50 AM</td>
<td>Break</td>
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<tr>
<td>10:00 AM</td>
<td>Design Techniques for a 112Gb/s PAM-4 Transmitter Jihwan Kim, Intel, Hillsboro, OR</td>
</tr>
<tr>
<td>10:45 AM</td>
<td>Equalization Techniques/Trends for 56+Gb/s and the Efficacy of Forward Error Correction, Cathy Liu, Broadcom, San Jose, CA</td>
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<tr>
<td>11:30 AM</td>
<td>High-Speed Clock and Data Recovery Circuit: Architecture, Modeling, Specifications, and Consideration Jri Lee, National Taiwan University, Taiwan</td>
</tr>
<tr>
<td>12:15 PM</td>
<td>Lunch</td>
</tr>
<tr>
<td>1:30 PM</td>
<td>Challenges and Solutions for High-Bandwidth Density, Energy-Efficient, Short-Reach Signaling that Enables Massively Scalable Parallelism John Wilson, Nvidia, Durham, NC</td>
</tr>
<tr>
<td>2:15 PM</td>
<td>Clock Generation and Distribution for 56Gb/s, 112Gb/s and Beyond Serial Links, Didem Turker, Xilinx, San Jose, CA</td>
</tr>
<tr>
<td>3:00 PM</td>
<td>Break</td>
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<tr>
<td>3:15 PM</td>
<td>Link Modelling and the Challenges and Limitations for IBIS AMI for 56+Gb/s in Matching Circuit Performance Mike Steinberger, Signal Integrity Software, Chippewa Falls, WI</td>
</tr>
<tr>
<td>4:00 PM</td>
<td>Non-Differential Techniques: Multi-Wire Multi-Level I/O Armin Tajalli, University of Utah, Salt Lake City, Utah</td>
</tr>
<tr>
<td>4:45 PM</td>
<td>Conclusion</td>
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Conditioning the data converter function to the properties of evolving CMOS technologies through architectural, algorithmic and circuit innovation enabled the last decades making radical steps in accuracy, speed and power efficiency. In analogy to this, optimizing the data converter for the unique requirements of emerging applications such as 5G mobile, biomedical and IoT, imaging, automotive radars and wireline communications offers the designer new degrees of freedom to improve performance and power efficiency of the data converter.

This forum addresses the unique challenges of application-specific data converters and presents the best tradeoffs and optimum architectures for each application.

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</tbody>
</table>
| 8:20 AM  | Introduction  
**Kostas Doris**, NXP Semiconductors, Eindhoven, The Netherlands                      |
| 8:30 AM  | Application-Optimized Data Converters: An Introduction  
**Boris Murmann**, Stanford University, Palo Alto, CA                                    |
| 9:20 AM  | ADCs for Biomedical and IoT Applications  
**Chih-Cheng Hsieh**, National Tsing Hua University, Hsinchu, Taiwan                    |
| 10:10 AM | Break                                                                                       |
| 10:30 AM | Filtering Delta-Sigma ADCs for Mobile Receivers  
**Maurits Ortmanns**, University of Ulm, Ulm, Germany                                    |
| 11:20 AM | Data Converter Design Considerations for Mobile Transceivers: Benchmark and Trends from 4G LTE to 5G NR  
**Tien-Yu Lo**, Tien-Yu Lo, MediaTek, Hsinchu, Taiwan                                        |
| 12:10 PM | Lunch                                                                                       |
| 1:10 PM  | Analog-to-Digital Conversion for Imaging, from 2-D to Lidar  
**Ron Kapusta**, Analog Devices, Wilmington, MA                                           |
| 2:00 PM  | Analog-to-Digital Converters for Automotive Radar  
**Erwin Janssen**, NXP Semiconductors, Eindhoven, The Netherlands                         |
| 2:50 PM  | Break                                                                                       |
| 3:10 PM  | Multi-GS/s Data Converters for High-Speed Wireline and Optical Links  
**Jun Cao**, Broadcom, Irvine, CA                                                          |
| 4:00 PM  | Panel Discussion - All speakers  
Moderator: **David Robertson**, Analog Devices, Wilmington, MA                             |
| 4:50 PM  | Closing Remarks                                                                           |
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Jason H. Anderson, University of Toronto, Toronto, Canada
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Saturday, February 16  4:00 pm to 7:00 pm
Sunday, February 17  7:00 am to 8:30 pm
Monday, February 18  6:30 am to 3:00 pm
Tuesday, February 19  8:00 am to 3:00 pm
Wednesday, February 20  8:00 am to 3:00 pm
Thursday, February 21  7:00 am to 2:00 pm

Students must present their Student ID at the Registration Desk to receive the student rates. Those registering at the IEEE Member rate must provide their IEEE Membership number.

Deadlines: The deadline for registering at the Early Registration rates is 11:59 pm Pacific Time Tuesday January 8, 2019. After January 8th, and on or before 11:59 pm Pacific Time Sunday January 27, 2019, registrations will be processed at the Late Registration rates. After January 27th, you must register at the on-site rates. You are urged to register early to obtain the lowest rates and ensure your participation in all aspects of ISSCC.

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Demonstration Sessions: Hardware demonstrations will support selected papers on Monday and Tuesday evenings.

Author Interviews: Author Interviews will be held Monday, Tuesday and Wednesday evenings. Authors from each day’s papers will be available to discuss their work.

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- Papers Visuals: The visuals from all papers presented will be available by download.
- Demonstration Session Guidebook: A descriptive guide to the Demonstration Session will be available by download.
- Note: Instructions will be provided for access to all downloads. Downloads will be available both during the Conference and for a limited time afterwards.
OPTIONAL EVENTS

Educational Events: Many educational events are available at ISSCC for an additional fee. There are ten 90-minute Tutorials and two all-day Forums on Sunday. There are four additional all-day Forums on Thursday as well as an all-day Short Course. All events include a course handout in color. The Forums and Short Course include breakfast, lunch and break refreshments. The Tutorials include break refreshments. See the schedule for details of the topics and times. A “Thursday All-Access Pass” is available that provides access to all Thursday educational events and a copy of each course handout. Pick just the speakers you want to hear!

OPTIONAL PUBLICATIONS

ISSCC 2019 Publications: The following ISSCC 2019 publications can be purchased in advance or on site:

- 2019 ISSCC Download USB: All of the downloads included in conference registration (mailed in March).
- 2019 Tutorials USB: All of the 90 minute Tutorials (mailed in June).
- 2019 Short Course USB: “Hardware Approaches to Machine Learning and Inference” (mailed in June).

The Short Course and Tutorial USBs contain audio and written English transcripts synchronized with the presentation visuals. In addition, the USBs contain a pdf file of the presentations and pdf files of key reference material.

Earlier ISSCC Publications: Selected publications from earlier conferences can be purchased. There are several ways to purchase this material:

- Items listed on the registration form can be purchased with registration and picked up at the conference.
- Visit the ISSCC Publications Desk. This desk is located in the registration area and has the same hours as conference registration. With payment by cash, check or credit card, you can purchase materials at this desk. See the posted list at the Conference for titles and prices.
- Visit the ISSCC website at www.isscc.org and click on the link “About/Shop ISSCC/Shop Now” where you can order online or download an order form to mail, email or fax. For a small shipping fee, this material will be sent to you immediately and you will not have to wait until you attend the Conference to get it.

HOW TO MAKE HOTEL RESERVATIONS

Online: ISSCC participants are urged to make their hotel reservations at the San Francisco Marriott Marquis online. Go to the conference website and click on the Hotel Reservation link. Conference room rates are $279 for a single/double, $304 for a triple and $329 for a quad (per night plus tax). In addition, ISSCC attendees booked in the ISSCC group receive in-room Internet access for free. All online reservations require the use of a credit card. Online reservations are confirmed immediately. You should print the page containing your confirmation number and reservation details and bring it with you when you travel to ISSCC.

Telephone: Call 877-622-3056 (US) or 415-896-1600 and ask for “Reservations.” When making your reservation, identify the group as ISSCC 2019 to get the group rate.

Hotel Deadline: Reservations must be received at the San Francisco Marriott Marquis no later than 5 pm Pacific Time January 28, 2019 to obtain the special ISSCC rates. A limited number of rooms are available at these rates. Once this limit is reached or after January 28th the group rates may no longer be available and reservations will be filled at the best available rate. Changes: Before the hotel deadline, your reservation can be changed by calling the telephone numbers above. After the hotel deadline, call the Marriott Marquis at 415-896-1600 (ask for “Reservations”). Have your hotel confirmation number ready.

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REFERENCE INFORMATION

TAKING PICTURES, VIDEOS OR AUDIO RECORDINGS DURING ANY OF THE SESSIONS IS NOT PERMITTED

Conference Website: www.isscc.org
ISSCC Email: ISSCC@ieee.org
Registration questions: ISSCCInfo@yesevents.com
Hotel Information: San Francisco Marriott Marquis
780 Mission Street
San Francisco, CA 94103
Phone: 415-896-1600
Press Information: Kenneth C. Smith
University of Toronto
Email: lcufjino@aol.com
Phone: 416-418-3034
Registration: YesEvents
1700 Reisterstown Road #236
Baltimore, MD 21208
Email: issccinfo@yesevents.com
Phone: 410-559-2200 or 800-937-8728
Fax: 410-559-2217

Hotel Transportation: Visit the ISSCC website “Registration/Transportation from Airport” page for helpful travel information and links. You can get a map and driving directions from the hotel website at:

Next ISSCC Dates and Location:
ISSCC 2020 will be held on February 16-20, 2020 at the San Francisco Marriott Marquis Hotel.

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