

ADVANCE PROGRAM



2022 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

FEBRUARY
19, 20, 21, 22, 23, 24, 25, 26

ALL VIRTUAL

CONFERENCE THEME:

**Intelligent Silicon
for a Sustainable World**

DRAFT 2 - 17 - 2022

12 TUTORIALS

ANALOG CIRCUITS FOR BCD; HIGH FREQUENCY DC-DC CONVERTERS; NOISE-SHAPING SAR ADCs; SELF-SENSING PROCESSING SYSTEMS;
PROCESS MONITORS FOR SIGNOFF-ORIENTED CIRCUITS; POWER TRANSFER/MANAGEMENT FOR MEDICAL APPS;
HBM DRAM/3D STACKED; MIXED-MODE RF TRANSCEIVERS; ENERGY HARVESTING WIRELESS SENSOR NODES; MM-WAVE PHASED-ARRAYS;
EQUALIZATION TECHNIQUES; DIGITAL VS. ANALOG AI ACCELERATORS

6 FORUMS

CX: OVERCOMING DATA BOTTLENECK; CHIP DESIGN FOR SECURE IoTS; PATH TO 6G;
PAYING THE WAY TO 200Gb/s; IMPROVE AI EFFICIENCY; COMPUTER SYSTEMS UNDER ATTACK

SHORT-COURSE

HIGH SPEED/HIGH PERFORMANCE DATA CONVERTERS

ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and application to maintain technical currency, and to network with leading experts.

ISSCC 2022 ON-DEMAND CONTENT / RELEASE

ISSCC ON-DEMAND CONTENT	RELEASE DATE
TUTORIALS	FRIDAY, FEBRUARY 11, 5PM PST
FORUMS, SHORT COURSE	FRIDAY, FEBRUARY 11, 5PM PST
TECHNICAL PAPERS	FRIDAY, FEBRUARY 18, 5PM PST
PLENARY TALKS	MONDAY, FEBRUARY 21, 7AM PST

Recorded content available until March 31, 2022

CONFERENCE TECHNICAL HIGHLIGHTS

This year, ISSCC 2022 will be available only virtually.

See next page for Conference schedule details.

Need Additional Information? Go to: www.isscc.org

ISSCC 2022 Timetable

ISSCC 2022 • SUNDAY FEBRUARY 20TH

Tutorials

7:00 AM T6: Wireless Power Transfer and Management for Medical Applications	7:20 AM T5: Fundamentals of Process Monitors for Signoff-Oriented Circuit Design	7:40 AM T4: Fundamentals of Self-Sensing Processing Systems
8:00 AM T3: Noise-Shaping SAR ADCs	8:20 AM T2: Fundamentals of High Frequency DC-DC Converters	8:40 AM T1: Analog Circuit Design in Bipolar-CMOS-DMOS (BCD) Technologies
7:00 AM T12: Advances in Digital vs. Analog AI Accelerators	7:20 AM T11: Basics of Equalization Techniques: Channels, Equalization, and Circuits	7:40 AM T10: Fundamentals of mm-Wave Phased-Arrays
8:00 AM T9: Design Methodologies for Energy Harvesting Wireless Sensor Nodes	8:20 AM T8: Fundamentals of Mixed-mode RF Transceivers	8:40 AM T7: HBM DRAM and 3D Stacked Memory

Special Events

8:30 AM	8:30 AM – SE1: Student Research Preview: Short Presentations with Poster Session	7:00 AM – SE2: Next Generation Circuit Designer 2022 Workshop
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ISSCC 2022 • MONDAY FEBRUARY 21ST

6:45 AM – FORMAL OPENING OF THE CONFERENCE

Plenary I

7:00 AM – 1.1: Catalysts of the Impossible: Silicon, Software, and Smarts for the Era of SysMoore	7:45 AM – 1.2: Intelligent Sensing: Enabling the Next “Automation Age”
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Paper Sessions

8:30 AM	Session 2: Processors	Session 3: Analog Techniques & Sensor Interfaces	Session 4: mm-Wave and Sub-THz ICs for Communication and Sensing	Session 5: Imagers, Range Sensors and Displays	Session 6: Ultra-High-Speed Wireline	Session 7: NAND Flash Memory
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ISSCC 2022 • TUESDAY FEBRUARY 22ND

Plenary II

7:00 AM – 1.3: The Art of Scaling: Distributed and Connected to Sustain the Golden Age of Computation
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Awards

7:20 AM – ISSCC, SCS, IEEE Award Presentations

Plenary II

7:45 AM – 1.4: The Future of the High-Performance Semiconductor Industry and Design
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Paper Sessions

8:30 AM	Session 8: Advanced RF Building Blocks	9:00 AM Session 9: High-Quality GHz-to-THz Frequency Generation and Radiation	Session 10: Nyquist and Incremental ADCs	Session 11: Compute-in-Memory and SRAM	Session 12: Monolithic System for Robot and Bio Applications	Session 13: Digital Techniques for Clocking, Variation Tolerance and Power Management	Session 14: Gan, High-Voltage and Wireless Power
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ISSCC 2022 • WEDNESDAY FEBRUARY 23RD

Highlighted Industry Chips & Demonstration Sessions

7:00 AM	7:00 AM – Session 21: Highlighted Chip Releases: Digital/ML	7:00 AM – Demonstration Session 1
7:45 AM	7:45 AM – Session 26: Highlighted Chip Releases: Systems and Quantum Computing	7:45 AM – Demonstration Session 2

Paper Sessions

8:30 AM	Session 15: ML Processors	Session 16: Emerging Domain-Specific Digital Circuits and Systems	Session 17: Advanced Wireline Links and Techniques	Session 18: DC-DC Converters	Session 19: Power Amplifiers and Building Blocks	Session 20: Body and Brain Interfaces
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ISSCC 2022 • THURSDAY FEBRUARY 24TH

Paper Sessions

7:00 AM	Session 22: Cryo-Circuits and Ultra-Low-Power Intelligent IoT	Session 23: Frequency Synthesizers	Session 24: Low-Power and UWB Radios for Communication and Ranging	Session 25: Noise-Shaping ADCs	Session 27: mm-Wave & Sub-6GHz and Receivers and Transceivers for 5G Radios	Session 28: DRAM and Interface
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Special Events

7:00 AM	7:00 AM – SE3: Semiconductor Supply Chain	7:00 AM – SE4: The Bright and Dark Side of Artificial Intelligence (AI)
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Paper Sessions

8:30 AM	Session 29: ML Chips for Emerging Applications	Session 30: Power Management Techniques	Session 31: Audio Amplifiers	Session 32: Ultrasound and Beamforming Applications	Session 33: Domain Specific Processors	Session 34: Hardware Security
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ISSCC 2022 • FRIDAY FEBRUARY 25TH

Forums

7:00 AM	F1: Compute-in-X (CiX): Overcoming the Data Bottleneck in AI Processing	F2: Chip Design for Low-Power, Robust, and Secure IoT Devices	F3: The Path to 6G: Architectures, Circuits, Technologies for Sub-THz Communications, Sensing and Imaging
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Special Events

8:30 AM	8:30 AM – SE5: Shifting Tides of Innovation – Where is Cutting-Edge Research Happening Today?	8:30 AM – SE6: Next Trillion Dollar Market
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ISSCC 2022 • SATURDAY FEBRUARY 26TH

Forums & Short Course

7:00 AM	F4: Paving the Way to 200Gb/s Transceivers	F5: How to Improve AI Efficiency Further: New Devices, Architectures and Algorithms	F6: Computer Systems Under Attack – Paying the Performance Price for Protection	Short Course: High Speed/High Performance Data Converters: Metrics, Architectures, and Emerging Topics
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SRP and WiC Mentoring Sessions

7:00 AM – SRP and WiC Mentoring Sessions

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TUTORIALS

There are a total of 12 tutorials this year on 12 different topics. Each tutorial, selected through a competitive process within each subcommittee of the ISSCC, presents the basic concepts and working principles of a single topic. These tutorials are intended for non-experts, graduate students and practicing engineers who wish to explore and understand a new topic.

Naveen Verma

ISSCC Tutorials Chair

The presentations and the videos of all 12 tutorials (90 minutes each)
will be available online, on-demand, as of:
Friday, Feb. 11, 2022, 5:00pm, PST

**Live Q&A sessions for the tutorials will be available on:
Sunday Feb. 20, 2022, 7:00am - 9:00am PST**

20 minute live session = 5 minute summary + 10 minute Q&A + 5 minute break

The Q&A sessions will be recorded and made available after their live sessions.

Live Q&A - February 20, 7:00am PST

T6: Wireless Power Transfer and Management for Medical Applications

Mehdi Kiani, *The Pennsylvania State University, University Park, PA*

Wireless technologies play an important role in advanced biomedical systems. Implantable medical devices (IMDs) are a rapidly growing category of bio-systems, where the use of wireless technology is a necessity. This tutorial will present several system- and circuit-level techniques towards the development of novel wireless power-transfer systems with different modalities. Also, novel integrated power-management circuits with voltage and current mode operation will be reviewed.

Mehdi Kiani received his M.S. and Ph.D. degrees in Electrical and Computer Engineering from the Georgia Institute of Technology in 2012 and 2013, respectively. He joined the faculty of the School of Electrical Engineering and Computer Science at the Pennsylvania State University in August 2014 where he is currently an Associate Professor. His research interests are in the multidisciplinary areas of analog, mixed-signal, and power-management integrated circuits, wireless implantable medical devices, neural interfaces, and assistive technologies. He was a recipient of the 2020 NSF CAREER Award. He is currently an Associate Editor of the IEEE Transactions on Biomedical Circuits and Systems and IEEE Transactions on Biomedical Engineering.

Live Q&A - February 20, 7:20am PST

T5: Fundamentals of Process Monitors for Signoff-Oriented Circuit Design

Eric Jia-Wei Fang, *Mediatek, Hsinchu City, Taiwan*

In advanced technology nodes, the process technology requires more than a year to reach maturity. To avoid costly iterations between design and foundry, thus impeding time-to-market, the final validation of circuit timing and power, known as chip signoff, should leverage on-chip process monitors to speed-up process learning. This tutorial introduces the relationship between process and signoff in terms of speed/leakage, voltage, temperature and aging. Then, the tutorial covers the different types of digital circuits, with a focus on the corresponding challenges, to monitor this relationship. Since signoff requires a statistical methodology, silicon big-data collection and analysis are described to provide feedback to the foundry and designers.

Eric J.-W. Fang received the B.S. degree in electrical engineering from National Cheng Kung University, Taiwan in 2003, and the M.S. and Ph.D. degrees in electronics engineering from National Taiwan University, Taiwan in 2005 and 2009, respectively. He was a Visiting Scholar with the University of Illinois at Urbana-Champaign, Champaign, USA between 2008 and 2009. He is currently a senior department manager with MediaTek, Inc. and has served as an International Technical Program Committee member for IEEE ISSCC since 2021. His current research interests include digital sensor design with machine-learning technology, digital timing and IR signoff, and chip-package-board co-design. He has published more than 15 technical papers and holds 10 granted US patents.

Live Q&A - February 20, 7:40am PST

T4: Fundamentals of Self-Sensing Processing Systems

Shidhartha Das, *Arm, Cambridge, United Kingdom*

High-performance systems are challenged by the stringent computational, reliability and availability requirements of emerging cloud-native applications. Unfortunately, efficiency gains through scaling alone have slowed, even as susceptibility to variation-induced system failures have increased, thus necessitating further innovations in energy efficient and reliable processor and system design. This tutorial addresses the following key aspects: how do sources of variations impact design margins and system reliability?; how do self-monitoring systems use sensors to measure ambient environment?; how is environment adaptation actuated in high-volume production systems using a combination of power-delivery and clocking techniques?; what design and analysis techniques can mitigate transient soft errors and hard errors due to transistor aging and interconnect failures?

Shidhartha Das received the M.Sc. and Ph.D. degrees from the University of Michigan, Ann Arbor, MI, USA, in 2003 and 2009, respectively. He is currently a Distinguished Engineer with Arm Ltd., Cambridge, UK where he conducts research in high-performance CPU design, focusing on circuit/micro-architectural techniques for power delivery and variation mitigation. In the past, he has contributed to multiple areas of technology development, including mixed-signal architectures for machine-learning acceleration and emerging non-volatile memories, for which he received the Arm Inventor of the Year award in 2016. He has 58 granted US patents and several more that are pending. He has received multiple best paper awards and his research has been featured in IEEE Spectrum. He serves as the Guest Editor for the IEEE Journal of Solid-State Circuits and Associate Editor for the IEEE Solid-State Circuits Letters.

Live Q&A - February 20, 8:00am PST

T3: Noise-Shaping SAR ADCs

Yun-Shiang Shu, *MediaTek, Hsinchu City, Taiwan*

The noise-shaping (NS) successive-approximation register (SAR) has become a dominant emerging ADC architecture in a short time. Combining the benefits of SAR and noise shaping, NS-SAR ADCs take full advantage of advanced CMOS processes and continue to break records for energy and area efficiency. Along with increasing data rate, NS-SAR ADCs are getting attractive in various applications. This tutorial begins by explaining the basics of the NS SAR. It explores different noise-shaping techniques and introduces approaches for higher-order noise-shaping and high signal-bandwidth designs.

Yun-Shiang Shu (S'05–M'10–SM'19) received the B.S. and M.S. degrees in Electrical Engineering from National Taiwan University, Taiwan, in 1997 and 1999, respectively, and the Ph.D. degree in electrical and computer engineering from University of California at San Diego, CA in 2008. He is currently a Deputy Technical Director at MediaTek Inc., Hsinchu, Taiwan, where he leads the development of biosensors for wearable devices. His published works in ISSCC, VLSI, and JSSC range from flash, pipeline, SAR, to delta-sigma ADCs for communication and sensor interface applications, with a focus on signal processing techniques to compensate for analog circuit imperfections. Dr. Shu was a TPC member of the IEEE Symposium on VLSI Circuits and currently serves as an ITPC member and Far-East Regional Chair for IEEE ISSCC 2022.

Live Q&A - February 20, 8:20am PST

T2: Fundamentals of High-Frequency DC-DC Converters

Kousuke Miyaji, *Shinshu University, Nagano, Japan*

Advances in CMOS processes and the spread of GaN FETs are pushing the switching frequency of DC-DC converters beyond 10MHz. Such increase in the switching frequency of the converters results in reducing the size of passive components and increasing the system power density. Starting from the fundamentals of DC-DC buck converters, this tutorial will cover topics including loss analysis and control schemes at high frequencies typically above a few MHz. State-of-the-art design techniques to reduce the switching loss and to drive GaN FETs are also introduced. Finally, topics including recent progress in high-frequency magnetic components and their integration will be covered.

Kousuke Miyaji received the B.S., M.S., and Ph.D. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan, in 2003, 2005, and 2008, respectively. He is currently an Associate Professor in the Department of Electrical and Computer Engineering at Shinshu University. His current research interests include high-frequency DC-DC converters, efficient power-management systems, wireless power transfer systems, and 3D-integration of power magnetic components. Dr. Miyaji has been serving as a TPC member of the International Solid-State Circuits Conference (ISSCC) since 2021.

Live Q&A - February 20, 8:40am PST

T1: Analog Circuit Design in Bipolar-CMOS-DMOS (BCD) Technologies

Marco Berkhout, *Goodix Technology, Nijmegen, The Netherlands*

Bipolar-CMOS-DMOS (BCD) technologies enable applications of high industrial interest, whereby high-voltage and high-power circuits are combined with high-density digital logic on a single die, as in (audio) power amplifiers and switch-mode power supplies (SMPS). This tutorial addresses challenges of BCD design that are not usually encountered when designing in standard CMOS, e.g. crossing (multiple) voltage domains, parasitic bipolar activity with inductive loads, large operating supply voltage ranges and electrostatic discharge (ESD). The tutorial looks into the structure of BCD technologies and devices, as well as typical circuits, such as power switches, gate drivers, level shifters and bootstraps.

Marco Berkhout received the M.Sc. and the Ph.D. degrees in EE from the University of Twente, The Netherlands, in 1992 and 1996. From 1996 to 2019, he was with Philips/NXP Semiconductors, Nijmegen, The Netherlands. He is currently a fellow with Goodix Technologies, Nijmegen. His main interests are class-D amplifiers and integrated power electronics. Dr. Berkhout was a TPC member of the European Solid-State Circuits Conference (ESSCIRC) from 2008 to 2018 and the International Solid-State Circuits Conference (ISSCC) from 2013 to 2016, and since 2021. He received the ESSCIRC 2002 Best Paper Award and was a plenary invited speaker at the ESSCIRC 2008.

Live Q&A - February 20, 7:00am PST

T12: Advances in Digital vs. Analog AI Accelerators

Jae-sun Seo, *Arizona State University, Tempe, AZ*

For state-of-the-art AI accelerators, there have been large advances in both all-digital and analog/mixed-signal circuit-based designs. This tutorial presents a practical overview and comparison of recent digital and analog AI accelerators. It will first introduce recent AI algorithms for computer vision and speech applications, which have been targeted for many AI hardware designs. Next, it will present a survey of (i) all-digital AI accelerators, including designs with new dataflow, low precision, and sparsity, and (ii) analog/mixed-signal AI accelerators featuring switch-capacitor circuits and in-memory computing with analog-to-digital converters. The tutorial discusses the key trade-offs of both design approaches including circuit/architecture design, algorithm-mapping flexibility, hardware accuracy and energy efficiency.

Jae-sun Seo received the Ph.D. degree from the University of Michigan in 2010. From 2010 to 2013, he was with IBM T. J. Watson Research Center. In 2014, he joined ASU in the School of Electrical, Computer and Energy Engineering, where he is now an Associate Professor. He was a visiting faculty at Intel Circuits Research Lab in 2015. His research interests include efficient hardware design of machine learning and neuromorphic algorithms. He has authored/co-authored >130 papers and holds >10 issued U.S. patents. He is a recipient of an IBM Outstanding Technical Achievement Award (2012), an NSF CAREER Award (2017), and an Intel Outstanding Researcher Award (2021). He currently serves as an International Technical Program Committee member for ISSCC and an Associate Editor for IEEE Open Journal of the Solid-State Circuits Society (OJ-SSCS).

Live Q&A - February 20, 7:20am PST

T11: Basics of Equalization Techniques: Channels, Equalization, and Circuits

Byungsub Kim, *Pohang University of Science and Technology, Pohang, Korea*

This tutorial presents basic equalization techniques for high-speed serial interfaces. A simple channel transfer function model will be discussed to explain various channel behaviors. Basic transmitter and receiver equalization techniques such as feed-forward equalization (FFE), continuous-time linear equalization (CTLE), and decision-feedback equalization (DFE) will be covered. Modulation techniques such as non-return-to-zero (NRZ), duo-binary, and pulse-amplitude modulation 4 (PAM-4) will be discussed. Various implementations and design challenges of equalization circuits will be discussed and compared. Various methods of equalization adaptation algorithms will be covered.

Byungsub Kim received the B.S. degree in electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, South Korea, in 2000, and the M.S. and Ph.D. degrees in electrical engineering and computer science from the Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, in 2004 and 2010, respectively. He was an Analog Design Engineer with Intel Corporation, Hillsboro, OR, USA, from 2010 to 2011. In 2012, he joined the Faculty of Department of Electrical Engineering, POSTECH, where he is currently an Associate Professor. Dr. Kim received several honorable awards. He was a recipient of the IEEE Journal of Solid-State Circuits Best Paper Award in 2009. He was a co-recipient of the Beatrice Winner Award for Editorial Excellence at the 2009 IEEE Internal Solid-State Circuits Conference. He has been serving as a Technical Program Committee Member of IEEE International Solid-State Circuits Conference since 2018.

Live Q&A - February 20, 7:40am PST

T10: Fundamentals of mm-Wave Phased-Arrays

Bodhisatwa Sadhu, *IBM T. J. Watson Research Center, Yorktown Heights, NY*

Millimeter(mm)-Wave phased arrays are becoming a differentiating technology in modern wireless communication and imaging systems. This tutorial will cover key aspects of silicon-based mm-wave phased-array IC design and package integration. It will begin with an overview of the theory and intuition behind phased arrays; it will then discuss different silicon-based phased-array architectures and key phased-array building blocks, including phase shifters, variable-gain amplifiers, combiners, and splitters. Finally, this tutorial will discuss the integration of phased-array ICs with antennas in phased-array antenna modules.

Bodhisatwa Sadhu received the B.E. degree in electrical and electronics engineering from Birla Institute of Technology and Science (BITS) – Pilani, India in 2007, and the Ph.D. degree in Electrical Engineering from the University of Minnesota, Minneapolis, in 2012. He is currently a Research Scientist at IBM T. J. Watson Research Center, NY, and an Adjunct Assistant Professor at Columbia University, NY. At IBM, he led the design of the world's first reported silicon-based 5G phased array IC. He has authored/co-authored 50+ papers, a book, and several book chapters, and holds 50+ issued U.S. patents. He is the recipient of multiple awards including the 2017 ISSCC Lewis Winner Award for Outstanding Paper and the 2017 JSSC Best Paper Award. He is an MTT-S Distinguished Microwave Lecturer, and serves on the steering committee of IEEE RFIC Symposium, and the ITPC of IEEE ISSCC.

Live Q&A - February 20, 8:00am PST

T9: Design Methodologies for Energy Harvesting Wireless Sensor Nodes

Sriram Vangal, *Intel, Hillsboro, OR*

Wireless sensor nodes (WSNs) for IoT systems need to enable always-on always-sensing (AOAS) and advanced edge-computing capabilities under stringent energy constraints, often supported primarily by harvested energy. After an introduction into WSNs and their implementation challenges, this tutorial provides an overview of key blocks, designs, and system-level optimizations to enable energy-efficient WSN silicon. Multi-layered co-optimization approaches that crosscut architecture, devices, near-threshold voltage (NTV) logic and SRAM circuits, NTV cell libraries, low-power tool flows/methodologies, and aggressive power management techniques are required for realizing energy-efficient (μW) WSNs. The tutorial will also cover emerging trends in embedded energy-harvesting circuits, necessary to work in harmony with smart and fine-grain power management of different components of the WSN for realizing secure, AOAS-capable energy-neutral WSN systems.

Sriram Vangal received the B.E. degree from Bangalore University, India, in 1993, the M.S. degree from the University of Nebraska, Lincoln, USA in 1995, and the Ph.D. degree from Linköping University, Sweden in 2007 – all in Electrical Engineering. He joined Intel Corporation in 1995 and has played a lead role in multi-core CPU development and ultra-low power silicon research. Sriram is a Principal Engineer with Intel Labs researching sustainable net-zero energy computing. Sriram has received two Intel Achievement Awards for his work, is an IEEE senior member and has published over 35 conference and journal papers, has authored three book chapters, and has over 30 issued patents.

Live Q&A - February 20, 8:20am PST T8: Fundamentals of Mixed-Mode RF Transceivers Jeff Walling, *Virginia Tech, Blacksburg, VA*

RF systems that directly interface between digital bits and RF front-ends are rapidly gaining interest as the number of transceivers in mobile systems is increasing. This tutorial will review the concepts of direct digital-to-RF conversion and focus on the analysis and design of digital transceiver building blocks, such as switched capacitor RF-DACs, current-mode RF-DACs, and directly quantized receiver circuits. The tutorial will focus on the practical implementation of these circuit blocks using theoretical predictions.

Jeff Walling received his PhD degree from the University of Washington in 2008 and has been actively engaged in research and product design in the wireless industry for 20 years. While a student and intern at Intel Research, he was an early pioneer in digital friendly and mixed-mode transceiver systems and has continued to lead innovation in the field, particularly with the introduction of the switched-capacitor power amplifier. He has published >70 journal and conference papers and has twice won outstanding department teaching awards at Rutgers University and the University of Utah. He was in the corporate R&D group at Qualcomm and the AI solutions sector at Skyworks. Since the Fall of 2021, he is an Associate Professor in the ECE department at Virginia Tech. His research is focused on efficient radio architectures from RF-to-THz for next generation communication networks.

Live Q&A - February 20, 8:40am PST T7: HBM DRAM and 3D Stacked Memory Dong Uk Lee, *SK hynix, Icheon-si, Korea*

The proliferation of machine-learning workloads has accelerated the demand for higher memory bandwidth in modern systems. HBM DRAM was developed to break through the system-performance limit caused by memory bandwidth. With advanced packaging technology, HBM has been the only scalable DRAM bandwidth solution of the past 10 years, starting from 128GB/s and now extending beyond 800GB/s. This tutorial will cover HBM, HBM2, and HBM3 architectures; it will also cover historical trends and state-of-the-art for DRAM. Electrical interfaces and PDN for 2.5D system-in-package (SiP) structures will be reviewed, along with heterogeneous memory structures, including TSV interfaces. This tutorial will also cover the various design methods such as known-good-stack verification, self-repair, MBIST and RAS features, to deal with the new package structures. Finally, advanced 3D memory architectures including future trends of HBM, will be introduced.

Dong Uk Lee is Principal Engineer of SK hynix. He was the Lead Engineer of the industry's first HBM DRAM development and standardization from 2011 to 2013. He received the B.S. and M.S. degrees in electronics from Hanyang University, Seoul, Korea, in 1996 and 2001. He joined Hynix in 2001, and has developed 16 commodity DRAMs, including graphics DRAM, computing DRAM, HBM, HBM2E and HBM3. He holds 70 US patents. He is the author of 8 ISSCC and 2 JSSC, from 2006 to 2020. He presented an invited paper at CICC 2015, and he was a forum presenter at ISSCC 2016. Mr. Lee received the Medal of Honor for outstanding contribution to the semiconductor industry from the Government of Korea in 2021. Since 2017, he has been serving as a member of the ISSCC Technical Program Committee.

SE1: Student Research Preview (SRP)

The Student Research Preview (SRP) will highlight selected student research projects in progress. The SRP consists of 90 second presentations followed by a Poster Session, by graduate students from around the world, which have been selected on the basis of a short submission concerning their on-going research. Selection is based on the technical quality and innovation of the work. This year, the SRP will be presented in two theme sections: Digital and Machine-Learning; Analog and Radio.

The Student Research Preview will include a Distinguished Lecture by Prof. Kofi Makinwa, Delft University of Technology. SRP is open to all ISSCC registrants.

SRP Session (8:30 AM – 10:30 AM)

8:30 AM:	Introductory Remarks
8:35 AM:	Awards Silk Road Award SSCS Pre-Doctoral Fellowship Award ISSCC Student Travel Grant
8:45 AM:	Distinguished Speaker Talk (pre-recorded) “ <i>First Time Right!</i> ” by Prof. Kofi Makinwa, Delft University of Technology
9:00 AM - 9:30 AM:	90 Second Presentations (pre-recorded)
9:30 AM - 10:30 AM:	Posters (Gathertown)

SRP Organizing Committee

Co-Chair:	Jerald Yoo	National University of Singapore, Singapore
Co-Chair:	Mondira Pant	Intel, MA
Advisor:	Anantha Chandrakasan	MIT
Advisor:	Kevin Zhang	TSMC
Advisor:	Jan Van der Spiegel	University of Pennsylvania
Media/Publications:	Laura Fujino	University of Toronto
A/V:	Trudy Stetzler	Halliburton, Houston, TX

Committee Members

Masoud Babaie , Delft University of Technology, Netherlands	Phillip Nadeau , Analog Devices, MA
Utsav Banerjee , Indian Institute of Science, India	Mondira Pant , Intel, MA
Hsin-Shu Chen , National Taiwan University, Taiwan	Negar Reiskarimian , MIT, MA
Po-Hung Chen , National Chiao Tung University, Taiwan	Jae-sun Seo , Arizona State University, AZ
Zeynep Deniz , IBM, NY	Atsushi Shirane , Tokyo Institute of Technology, Japan
Hao Gao , Eindhoven University of Technology, Netherlands	Mahsa Shoaran , EPFL, Switzerland
Minkyu Je , KAIST, Korea	Yildiz Sinangil , Apple, CA
Matthias Kuhl , Hamburg University of Technology, Germany	Mahmut Sinangil , TSMC, CA
Seulki Lee , IMEC-NL, Netherlands	Filip Tavernier , KU Leuven, Belgium
Yoonmyung Lee , SungKyunKwan University, Korea	Chia-Hsiang Yang , National Taiwan University, Taiwan
Shih-Chii Liu , University of Zurich/ETH Zurich, Switzerland	Lita Yang , Microsoft, CA
Carolina Mora Lopez , imec, Belgium	Rabia Tugce Yazicigil , Boston University, MA
Noriyuki Miura , Osaka University, Japan	Jerald Yoo , National University of Singapore, Singapore
	Milin Zhang , Tsinghua University, China

SE2:

Morning Session: Next Generation Circuit Designer 2022 Workshop

Chair: Yildiz Sinangil, *Apple, Cupertino, CA*
Co-Chair: Sophia Shao, *UC Berkeley, Berkeley, CA*
Co-Chair: Alice Wang, *Everactive, Plano, TX*

Workshop Committee:

Abira Alvater, *IEEE-SSCS, Piscataway, NJ*
Aya G. Amer, *MIT, Cambridge, MA*
Zeynep Deniz, *IBM Research, Yorktown Heights, NY*
Najme Ebrahimi, *University of Florida, Gainesville, FL*
Dina Reda El-Damak, *University of Science and Technology at Zewail City, Egypt*
Yasemin Engur, *EPFL, Switzerland*
Q. Jane Gu, *University of California Davis, CA*
Ulkuhan Guler, *Worcester Polytechnic Institute, Worcester, MA*
Yaoyao Jia, *University of Austin, Austin, TX*
Awani Khodkumbhe, *University of California, Berkeley, CA*
Rabia Tugce Yazicigil, *Boston University, Boston, MA*
Alicia Klinefelter, *NVIDIA, Durham, NC*
Deeksha Lal, *Anokiwave, Billerica, MA*
Jiamin Li, *National University of Singapore, Singapore*
Farhana Sheikh, *Intel, Hillsboro, OR*
Trudy Stetzler, *Halliburton, Houston, TX*
Vivienne Sze, *MIT, Cambridge, MA*
Kathy Wilcox, *AMD, Boxborough, MA*

Advisory Board:

Anantha Chandrakasan, *MIT, Cambridge, MA*

The IEEE SCS Women in Circuits together with ISSCC will be co-sponsoring the first “Next Generation Circuit Designer 2022” for young professionals and students. This is a virtual educational workshop for a diverse set of graduate and undergraduate students, and young professionals who have graduated with B.S. within the last two years, who are interested in learning how to excel at academic and industry careers in computer science and computer and electrical engineering.

The panel on “Our Path to Circuit Design”, with panelists from diverse regions, backgrounds and career levels, will touch upon topics such as:

- networking and mentoring,
- choosing or changing a career path, a research topic, or an advisor,
- time management, work-life balance, and mental and physical well-being,
- managing day-to-day life in both graduate school and industry,
- dealing with challenges and conflict, and more.

In addition to the panel, we will be selecting forty next generation circuit designers in academia and industry to attend a keynote from a distinguished speaker, an informal fireside chat with a high-profile leader in the field, and participate in an elevator pitch. The selected designers will also get the opportunity for networking and mentoring through virtual events leading up to the workshop. The morning virtual event will be followed by an optional evening in-person event, which will include further networking opportunities.

SE2:

IEEE SSCS WiC Next Generation Circuit Designer 2022

- 7:00AM – 7:10AM:** **Workshop Opening and Introduction**
Yildiz Sinangil, *Apple, Cupertino, CA*
Alice Wang, *Everactive, Plano, TX*
Sophia Shao, *University of Berkeley, Berkeley, CA*
- 7:10AM – 7:20AM:** **Video - "Advice to Next Generation Circuit Designers",**
presented by Kathy Wilcox, *AMD, Boxborough, MA*
- 7:20AM – 8:00AM:** **Fireside Discussion with**
Megan Smith, *United States Chief Technology Officer (CTO)*
of the United States
- Introduction and Facilitator:**
Rabia Tugce Yazicigil, *Boston University, Boston, MA*
- 8:05AM – 9:00AM:** **Next Generation Circuit Designers Elevator Pitch**
- Introduction and Facilitator:**
Deeksha Lal, *Anokiwave, Billerica, MA*
Najme Ebrahimi, *University of Florida, Gainesville, FL*
- The selected next generation circuit designers will have the chance to give an elevator pitch to the attendees.
- 9:05AM – 9:45AM:** **Special Talk by Tsu-Jae King Liu**,
Dean of the College of Engineering at the University of California, Berkeley, CA
- Introduction and Facilitator:**
Alicia Klinefelter, *NVIDIA, Durham, NC*
- 9:50AM – 10:50AM:** **Our Path To Circuit Design Panel**
- Panel Moderator:**
Dina Reda El-Damak, *University of Science and Technology at Zewail City, Egypt*

The panel on “Our Path to Circuit Design”, with panelists from diverse regions, backgrounds and career levels, will touch upon topics such as:

- networking and mentoring,
- choosing or changing a career path, a research topic, or an advisor,
- time management, work-life balance, and mental and physical well-being,
- managing day-to-day life in both graduate school and industry,
- dealing with challenges and conflict, and more.

Panelists:

Alvin Loke, *NXP, San Jose, CA*

Andreia Cathelin, *ST Microelectronics, Grenoble, France*

Canan Dagdeviren, *MIT, Cambridge, MA*

Ada Poon, *Stanford University, Stanford, CA*

Brian Floyd, *North Carolina State University, Raleigh, NC*

Plenary Session I — Invited Papers

Session Chair:

Kevin Zhang, *Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan*
ISSCC Conference Chair

Session Co-Chair:

Edith Beigné, *Meta, Menlo Park, CA*
ISSCC International Technical Program Chair

6:45 AM**FORMAL OPENING OF THE CONFERENCE****7:00 AM****1.1 Catalysts of the Impossible:****Silicon, Software, and Smarts for the Era of SysMoore**

Aart de Geus, *Chairman & Co-CEO, Synopsys, Mountain View, CA*

As we confront global scale challenges with immense intertwined datasets, the distillation of usable insights will require an exponential increase in AI processing capability. The impossibility horizon – sustained by the slowing of Moore's Law – will be pierced by rapid advancements in materials, devices, software, and architecture (the 'SysMoore' era). Autonomous design *instruments* – super-tools fusing together hundreds of algorithms precision-guided by AI – are unlocking opportunity for circuit designers ushering in a new wave of architectural vitality.

In the follow up to 'Builders of the Imaginary', we will unveil the next chapter in autonomous design, piecing together a new breed of super-monolithic devices, dense interconnects, and chiplets, into software-defined, heterogeneous architectures.

7:45 AM**1.2 Intelligent Sensing: Enabling the Next "Automation Age"**

Marco Cassis, *President, Analog, MEMS and Sensors Group*

Head of STMicroelectronics' Strategy, System Research and Applications,
Innovation Office, Geneva, Switzerland / Tokyo, Japan

Sensors have undergone extraordinary proliferation since the beginning of the 21st Century. Thanks to IoT, connected smart sensors can now be found all around us. This makes it possible to collect a wealth of data autonomously and continuously without human intervention, automating routine activities while unlocking previously unattainable insights and functionality. As we enter the Automation Age, the information generated from these sensors can be processed and acted on locally to take action in the physical world.

Sensing, artificial intelligence, and actuation will enable autonomous end-to-end system solutions in existing and new application fields including automotive, digital health, agriculture, environmental control, and decarbonization. The Semiconductor Industry is driving this transformation and sensors, smart embedded actuators, analog interfaces, connectivity, security and embedded AI, offer a perfect toolset for companies to continue to innovate. To fuel this innovation, we need to develop energy-efficient, high-accuracy, autonomous, ultra-compact, and trusted ICs. These chips need to feature state-of-the-art system and embedded security techniques to protect the gathered data, its processing and the resulting actuation. New and super-efficient computational hardware technologies supporting AI and machine learning are already transforming at-the-edge data processing and are pushing the envelope on intelligent functionality and IoT network scalability.

Future advances will rely on these evolving IC technologies as well as associated packaging solutions. These will include super-integration, wafer-to-wafer bonding, and system-in-package, to enable the heterogeneous integration of multiple technologies.

Processors

Session Chair: **Hugh Mair**, Mediatek, Fairview, TXSession Co-Chair: **Shidhartha Das**, ARM, Cambridge, United Kingdom

8:30 AM

2.1 Ponte Vecchio: A Multi-Tile 3D Stacked Processor for Exascale Computing

*W. Gomes¹, A. Koker², P. Stover³, D. Ingerly¹, S. Siers², S. Venkataraman⁴, C. Pelto¹, T. Shah⁵, A. Rao², F. O'Mahony¹, E. Karl¹, L. Cheney², I. Rajwan², H. Jain⁴, R. Cortez², A. Chandrasekhar⁴, B. Kanthi⁴, R. Koduri⁶, ¹Intel, Portland, OR; ²Intel, Folsom, CA; ³Intel, Chandler, AZ; ⁴Intel, Bengaluru, India
⁵Intel, Austin, TX; ⁶Intel, Santa Clara, CA*

8:40 AM

2.2 Sapphire Rapids: The Next-Generation Intel Xeon Scalable Processor

*N. Nassifi¹, A. O. Munch¹, C. L. Molnar¹, G. Pasdas², S. V. Iyer², Z. Yang¹, O. Mendoza¹, M. Huddart¹, S. Venkataraman³, R. Marom⁴, A. M. Kern¹, B. Bowhill¹, D. R. Mulvihill⁵, S. Nimmagadda³, V. Kalidindi¹, J. Krause¹, M. M. Haq¹, R. Sharma¹, K. Duda⁵, ¹Intel, Hudson, MA; ²Intel, Santa Clara, CA
³Intel, Bangalore, India; ⁴Intel, Haifa, Israel; ⁵Intel, Fort Collins, CO*

8:50 AM

2.3 IBM Telum: A 16-Core 5+ GHz DCM

*O. Geva¹, C. Berry¹, R. Sonnelitter¹, D. Wolpert¹, A. Collura¹, T. Strach², D. Phan¹, C. Lichtenau², A. Buyuktosunoglu³, H. Harre², J. Zitz¹, C. Marquart¹, D. Malone¹, T. Webe², A. Jatkowski¹, J. Isakson⁴, D. Hamid¹, M. Cichanowski⁴, M. Romain¹, F. Hasan⁴, K. Williams¹, J. Surprise¹, C. Cavitt¹, M. Cohen¹
¹IBM Systems and Technology, Poughkeepsie, NY
²IBM Systems and Technology, Boeblingen, Germany
³IBM Research, Yorktown Heights, NY; ⁴IBM Systems and Technology, Austin, TX*

9:00 AM

2.4 POWER10™: A 16-Core SMT8 Server Processor with 2TB/s Off-Chip Bandwidth in 7nm Technology

*R. M. Rao¹, C. Gonzalez², E. Fluhr³, A. Mathews³, A. Bianchi³, D. Dreps³, D. Wolpert⁴, E. Lai³, G. Strevig³, G. Wiedemeier³, P. Salz², R. Kruse³, ¹IBM, Bengaluru, India; ²IBM, Yorktown Heights, NY
³IBM, Austin, TX; ⁴IBM, Poughkeepsie, NY; ⁵IBM, Boeblingen, Germany*

9:10 AM

2.5 A 5nm 3.4GHz Tri-Gear ARMv9 CPU Subsystem in a Fully Integrated 5G Flagship Mobile SoC

*A. Nayak¹, H. Chen¹, H. Mair¹, R. Lagerquist¹, T. Chen¹, A. Rajagopalan¹, G. Gammie¹, R. Madhavaram¹, M. Jagota¹, C. Chung¹, J. Wiedemeier¹, B. Meera¹, C-Y. Yeh², M. Lin², C. Lin², V. Lin², J. Lin², Y. Chen², B. Chen², C-Y. Wu², R. ChangChien², R. Tzeng², K. Yang², A. Thippana¹, E. Wang², S. Hwang²
¹MediaTek, Austin, TX; ²MediaTek, Hsinchu, Taiwan*

9:20 AM

2.6 A 16nm 785GMACs/J 784-Core Digital Signal Processor Array with a Multilayer Switch Box Interconnect, Assembled as a 2x2 Dielet with 10µm-Pitch Inter-Dielet I/O for Runtime Multi-Program Reconfiguration

U. Rathore^{}, S. S. Nagi^{*}, S. Iyer, D. Marković, ^{*}Equally-Credited Authors (ECAs)
 University of California, Los Angeles, CA*

9:30 AM

2.7 Zen3: The AMD 2nd-Generation 7nm x86-64 Microprocessor Core

DS2 *T. Burd¹, W. Li¹, J. Pistole¹, S. Venkataraman¹, M. McCabe¹, T. Johnson¹, J. Vinh¹, T. Yiu¹, M. Wasio¹, H-H. Wong¹, D. Lieu¹, J. White², B. Manger², J. Lindner², J. Olson², S. Bakke², J. Sniderman², C. Henrion³, R. Schreiber⁴, E. Busta³, B. Johnson³, T. Jackson³, A. Miller³, R. Miller³, M. Pickett³, A. Horiuchi³, J. Dvorak³, S. Balagangadharan⁵, S. Ammikkalinga⁵, P. Kumar⁵
¹AMD, Santa Clara, CA; ²AMD, Boxborough, MA; ³AMD, Fort Collins, CO; ⁴AMD, Austin, TX
⁵AMD, Bangalore, India*

Analog Techniques & Sensor Interfaces

Session Chair: Viola Schaffer, *Texas Instruments, Freising, Germany*

Session Co-Chair: Jiawei Xu, *Fudan University, Shanghai, China*

8:30 AM

3.1 A Single-Crystal-Oscillator-Based Clock-Management IC with 18× Start-Up Time Reduction and 0.68ppm/°C Duty-Cycled Machine-Learning-Based RCO Calibration

J. Jung, S. Oh, J. Kim, G. Ha, J. Lee, S. Kim, E. Park, J. Lee, Y. Yoon, S. Bae, W. Kim, Y. Lim, K. Lee, J. Huh, J. Lee, T. B. Cho

Samsung Electronics, Hwaseong, Korea

8:40 AM

3.2 A 52MHz -158.2dBc/Hz PN @ 100kHz Digitally Controlled Crystal Oscillator Utilizing a Capacitive-Load-Dependent Dynamic Feedback Resistor in 28nm CMOS

J. Jung, S. Kim, W. Kim, J. Han, E. Park, S. Hwang, S. Oh, S. Han, K. Lee, J. Huh, J. Lee

Samsung Electronics, Hwaseong, Korea

8:50 AM

3.3 A 174μV_{RMS} Input Noise, 1GS/s Comparator in 22nm FDSOI with a Dynamic-Bias Preamplifier Using Tail Charge Pump and Capacitive Neutralization Across the Latch

H. S. Bindra, J. Ponte, B. Nauta

University of Twente, Enschede, The Netherlands

9:00 AM

3.4 A Second-Order Temperature-Compensated On-Chip R-RC Oscillator Achieving 7.93ppm/°C and 3.3pJ/hz in -40°C to 125°C Temperature Range

Y. Ji^{1,2}, J. Liao¹, S. Arjmandpour^{1,3}, A. Novello¹, J.-Y. Sim², T. Jang¹

¹ETH Zürich, Zürich, Switzerland

²Pohang University of Science and Technology, Pohang, Korea

³Sharif University of Technology, Tehran, Iran

9:10 AM

3.5 A ±25A Versatile Shunt-Based Current Sensor with 10kHz Bandwidth and ±0.25% Gain Error from -40°C to 85°C Using 2-Current Calibration

Z. Tang¹, R. Zamparette¹, Y. Furuta², T. Nezuka², K. A. A. Makinwa¹

¹Delft University of Technology, Delft, The Netherlands

²MIRISE Technologies, Aichi, Japan

9:20 AM

3.6 A MEMS Coriolis-Based Mass-Flow-to-Digital Converter with 100μg/h/√Hz Noise Floor and Zero Stability of ±0.35mg/h

A. C. de Oliveira, S. Pan, K. A. A. Makinwa

Delft University of Technology, Delft, The Netherlands

9:30 AM

3.7 A 2.6mW 10pT/√Hz 33kHz Magnetoimpedance-Based Magnetometer with Automatic Loop-Gain and Bandwidth Enhancement

I. Akita¹, T. Kawano², H. Aoyama², S. Tatematsu², M. Hioki¹

¹Advanced Industrial Science and Technology (AIST), Tsukuba, Japan

²Aichi Steel, Tohkai, Japan

9:40 AM

3.8 A BJT-Based CMOS Temperature Sensor Achieving an Inaccuracy of ±0.45°C (3σ) from -50°C to 180°C and a Resolution-FoM of 7.2pJ·K² at 150°C

B. Wang¹, M-K. Law², A. Bermak¹

¹Hamad Bin Khalifa University, Doha, Qatar

²University of Macau, Macau, China

mm-Wave and Sub-THz ICs for Communication and Sensing

Session Chair: Yiwu Tang, *Qualcomm Technologies, San Diego, CA*

Session Co-Chair: Ho-Jin Song, *POSTECH, Pohang, Korea*

8:30 AM

4.1 Fully Integrated 2D Scalable TX/RX Chipset for D-Band Phased-Array-on-Glass DS1 Modules

M. Elkhoully¹, J. Ha¹, M. J. Holyoak¹, D. Hendry², M. Sayginer¹, R. Enright¹, I. Kimionis¹, Y. Baeyens¹, S. Shahramian¹

¹Nokia Bell Labs, New Providence, NJ; ²now with L3 Harris, Queensland, Australia

8:40 AM

4.2 A Fully Integrated 160Gb/s D-Band Transmitter with 1.1pJ/b Efficiency in 22nm FinFET Technology

*S. Callender^{*1}, A. Whitcombe^{*2}, A. Agrawal^{*1}, R. Bhat¹, M. Rahman³, C. C. Lee⁴, P. Sagazio¹, G. Dogiamis⁵, B. Carlton¹, M. Chakravorti¹, S. Pellerano¹, C. Hull¹, ^{*}Equally-Credited Authors (ECAs)*

¹Intel, Hillsboro, OR; ²Intel, Santa Clara, CA; ³now with IIT Delhi, New Delhi, India

⁴now with Nebula Microsystems, Richardson, TX; ⁵Intel, Chandler, AZ

8:50 AM

4.3 A 140GHz Transceiver with Integrated Antenna, Inherent-Low-Loss Duplexing and DS2 Adaptive Self-Interference Cancellation for FMCW Monostatic Radar

X. Chen¹, M. I. W. Khan¹, X. Yi^{1,2}, X. Li^{1,3}, W. Chen³, J. Zhu⁴, Y. Yang⁴, K. E. Kolodziej⁵, N. M. Monroe¹, R. Han¹

¹Massachusetts Institute of Technology, Cambridge, MA

²South China University of Technology, Guangzhou, China; ³Tsinghua University, Beijing, China

⁴University of Technology Sydney, Ultimo, Australia; ⁵MIT Lincoln Laboratory, Lexington, MA

9:00 AM

4.4 A 23-to-29GHz Receiver with mm-Wave N-Input-N-Output Spatial Notch Filtering and Autonomous Notch-Steering Achieving 20-to-40dB mm-Wave Spatial Rejection and -14dBm In-Notch IP1dB

L. Zhang, M. Babaie, Delft University of Technology, Delft, The Netherlands

9:10 AM

4.5 Electronic THz Pencil Beam Forming and 2D Steering for High Angular-Resolution DS1 Operation: A 98×98-Unit 265GHz CMOS Reflectarray with In-Unit Digital Beam Shaping and Squint Correction

N. M. Monroe¹, G. C. Dogiamis², R. Stinge¹, P. Myers², X. Chen¹, R. Han¹

¹Massachusetts Institute of Technology, Cambridge, MA; ²Intel Corporation, Chandler, AZ

9:20 AM

4.6 A 430GHz CMOS Concurrent Transceiver Pixel Array for High Angular Resolution Reflection-Mode Active Imaging

Y. Zhu¹, P. R. Byreddy¹, S. Dong¹, K. K. O¹, W. Cho²

¹University of Texas at Dallas, Richardson, TX; ²Oklahoma State University, Stillwater, OK

9:30 AM

4.7 A 300GHz 52mW CMOS Receiver with On-Chip LO Generation

O. Memioğlu, Y. Zhao, B. Razavi, University of California, Los Angeles, CA

9:40 AM

4.8 A 3.4mW/element Radiation-Hardened Ka-Band CMOS Phased-Array Receiver Utilizing Magnetic-Tuning Phase Shifter for Small Satellite Constellation

X. Fu, Y. Wang, D. You, X. Wang, A. A. Fadila, Y. Zhang, S. Kato, C. Wang, Z. Li, J. Pang, A. Shirane, K. Okada

Tokyo Institute of Technology, Tokyo, Japan

Imagers, Range Sensors and Displays

Session Chair: *Mutsumi Hamaguchi, Sharp, Tenri, Japan*Session Co-Chair: *Seong-Jin Kim, Ulsan National Institute of Science and Technology, Ulsan, Korea*

8:30 AM

5.1 A 0.37W 143dB-Dynamic-Range 1Mpixel Backside-Illuminated Charge-Focusing SPAD Image Sensor with Pixel-Wise Exposure Control and Adaptive Clocked Recharging*Y. Ota, K. Morimoto, T. Sasago, M. Shinohara, Y. Kuroda, W. Endo, Y. Maehashi, S. Maekawa, H. Tsuchiya, A. Abdelghafar, S. Hikosaka, M. Motoyama, K. Tojima, K. Uehira, J. Iwata, F. Inui, Y. Matsuno, K. Sakurai, T. Ichikawa, Canon, Kanagawa, Japan*

8:40 AM

DS1 5.2 A 64x64-Pixel Flash LiDAR SPAD Imager with Distributed Pixel-to-Pixel Correlation for Background Rejection, Tunable Automatic Pixel Sensitivity and First-Last Event Detection Strategies for Space Applications*E. Manuzzato¹, A. Tontini¹, A. Seljak^{1,2}, M. Perenzoni¹*¹Fondazione Bruno Kessler, Trento, Italy; ²Jozef Stefan Institute, Ljubljana, Slovenia

8:50 AM

DS1 5.3 An 80x60 Flash LiDAR Sensor with In-Pixel Histogramming TDC Based on Quaternary Search and Time-Gated Δ -Intensity Phase Detection for 45m Detectable Range and Background Light Cancellation*S. Park¹, B. Kim¹, J. Cho², J-H. Chun^{2,3}, J. Cho^{2,3}, S-J. Kim¹*¹Ulsan National Institute of Science and Technology, Ulsan, Korea; ²SolidVue, Suwon, Korea³Sungkyunkwan University, Suwon, Korea

9:00 AM

5.4 A 38 μ m Range Precision Time-of-Flight CMOS Range Line Imager with Gating Driver Jitter Reduction Using Charge-Injection Pseudo Photocurrent Reference*K. Yasutomi, T. Furuhashi, K. Sagawa, T. Takasawa, K. Kagawa, S. Kawahito*
Shizuoka University, Hamamatsu, Japan

9:10 AM

5.5 A 1/1.57-inch 50Mpixel CMOS Image Sensor with 1.0 μ m All-Directional Dual Pixel by 0.5 μ m-Pitch Full-Depth Deep-Trench Isolation Technology*T. Jung, M. Fujita, J. Cho, K. Lee, D. Seol, S. An, C. Lee, Y. Jeong, M. Jung, S. Park, S. Baek, S. Jung, S. Lee, J. Yun, E. S. Shim, H. Han, E. Park, H. Sul, S. Kang, K. Lee, J. Ahn, D. Chang*
Samsung Electronics, Hwasung, Korea

9:20 AM

5.6 A 4.9Mpixel Programmable-Resolution Multi-Purpose CMOS Image Sensor for Computer Vision*H. Murakami¹, E. Bohannon¹, J. Childs¹, G. Gui¹, E. Moule¹, K. Hanzawa², T. Koda¹, C. Takano², T. Shimizu³, Y. Takizawa³, A. Basavalingappa¹, R. Childs¹, C. Cziesler¹, R. Jarnot¹, K. Nishimura³, S. Rogerson¹, Y. Nitta¹,*¹Sony Electronics, San Jose, CA; ²Sony Semiconductor Solutions, Atsugi, Japan³Sony LSI Design, Atsugi, Japan

9:30 AM

5.7 A Fully Digital Time-Mode CMOS Image Sensor with 22.9pJ/frame-pixel and 92dB Dynamic Range*S. Kim, T. Kim, K. Seo, G. Han, Yonsei University, Seoul, Korea*

9:40 AM

5.8 A 64Mpixel CMOS Image Sensor with 0.56 μ m Unit Pixels Separated by Front Deep-Trench Isolation*S. Park, C. Lee, S. Park, H. Park, T. Lee, D. Park, M. Heo, I. Park, H. Yeo, Y. Lee, J. Lee, B. Lee, D-C. Lee, J. Kim, B. Kim, J. Pyo, S. Quan, S. You, I. Ro, S. Choi, S-I. Kim, I-S. Joe, J. Park, C-H. Koo, J-H. Kim, C. K. Chang, T. Kim, J. Kim, J. Lee, H. Kim, C-R. Moon, H-S. Kim, Samsung Electronics, Hwaseong, Korea*

9:50 AM

DS1 5.9 A 10b Source-Driver IC with LSB-Stacked LV-to-HV-Amplify DAC Achieving 2688 μ m²/channel and 4.8mV DVO for Mobile OLED Displays*G-W. Lim¹, G-G. Kang¹, H. Ma², M. Jeong², H-S. Kim¹*¹KAIST, Daejeon, Korea; ²Samsung Display, Yongin, Korea

Ultra-High-Speed Wireline

Session Chair: Thomas Toiff, Cisco Systems, Thalwil, Switzerland

Session Co-Chair: Amir Amirkhany, Samsung Display America Lab, San Jose, CA

8:30 AM

6.1 A 1.41pJ/b 224Gb/s PAM-4 SerDes Receiver with 31dB Loss Compensation

DS1 Y. Segal¹, A. Laufer¹, A. Khairi¹, Y. Krupnik¹, M. Cusmai¹, I. Levin¹, A. Gordon¹, Y. Sabag¹, V. Rahinski¹, G. Ori¹, N. Familia¹, S. Litski¹, T. Warshavsky¹, U. Virobnik¹, Y. Horwitz¹, A. Balankutty², S. Kiran², S. Palermo³, P. M. Li⁴, A. Cohen¹

¹Intel, Jerusalem, Israel; ²Intel, Hillsboro, OR; ³Texas A&M University, College Station, TX

⁴Intel, San Jose, CA

8:40 AM

6.2 A 112.5Gb/s ADC-DSP-Based PAM-4 Long-Reach Transceiver with >50dB Channel Loss in 5nm FinFET

Z. Guo¹, A. Mostafa¹, A. Elshazly¹, B. Chen¹, B. Wang¹, C. Han¹, C. Wang¹, D. Zhou¹, D. Visani¹, E. Hsiao¹, F. Chu¹, F. Lu¹, G. Cui¹, H. Zhang¹, H. Wang¹, H. Zhao¹, J. Lin¹, J. Gu¹, L. Luo², L. Jiang¹, M. Singh¹, M. Gambhir¹, M. Hasan¹, M. Wu¹, M. J. Yoo¹, P. Liu¹, S. Kollu¹, T. Ye², X. Zhao², X. Yang¹, Y. Huang¹, X. Han¹, Y. Sun¹, Z. Yu¹, Z. H. Jiang¹, Z. Adal¹, Z. Yan¹

¹Marvell, Santa Clara, CA; ²Marvell, Shanghai, China

8:50 AM

6.3 A 2.29pJ/b 112Gb/s Wireline Transceiver with RX 4-Tap FFE for Medium-Reach Applications in 28nm CMOS

B. Ye, K. Sheng, W. Gai, H. Niu, B. Zhang, Y. He, S. Jia, C. Chen, J. Yu

Peking University, Beijing, China

9:00 AM

6.4 An 182mW 1-60Gb/s Configurable PAM-4/NRZ Transceiver for Large Scale ASIC Integration in 7nm FinFET Technology

N. Kocaman¹, U. Singh¹, B. Raghavan¹, A. Iyer¹, K. Thasari¹, S. Surana¹, J. W. Jung¹, J. Jeong¹, H. Zhang¹, A. Vasani¹, Y. Shim¹, Z. Huang¹, A. Garg¹, H-B. Lee¹, B. Wu², F. Liu¹, R. Wang¹, M. Loh², A. Wang², M. Caresosa¹, B. Zhang¹, A. Momtaz¹

¹Broadcom, Irvine, CA; ²Broadcom, San Jose, CA

9:10 AM

6.5 A 1.6Tb/s Chiptlet over XSR-MCM Channels using 113Gb/s PAM-4 Transceiver with Dynamic Receiver-Driven Adaptation of TX-FFE and Programmable Roaming Taps in 5nm CMOS

G. Gangasani¹, D. Hanson¹, D. Storaska¹, H. H. Xu¹, M. Kelly¹, M. Shannon¹, M. Sorna¹, M. Wielgos¹, P. B. Ramakrishna², S. Shi², S. Parker¹, U. K. Shukla², W. Kelly¹, W. Su³, Z. Yu⁴

¹Marvell, Hopewell Junction, NY; ²Marvell, Bangalore, India; ³Marvell, Shanghai, China

⁴Marvell, Santa Clara, CA

9:20 AM

6.6 A 1-58.125Gb/s, 5-33dB IL Multi-Protocol Ethernet-Compliant Analog PAM-4 Receiver with 16 DFE Taps in 10nm

B. Zand, M. Bichan, A. Mahmoodi, M. Shashaani, J. Wang, R. Shulyzki, J. Guthrie, K. Tyshchenko, J. Zhao, E. Liu, N. Soltani, A. Freeman, R. Anand, S. Rubab, R. Khela, S. Sharifian, K. Herterich

Intel, Toronto, Canada

9:30 AM

6.7 A 50Gb/s PAM-4 Bi-Directional Plastic Waveguide Link with Carrier Synchronization Using PI-Based Costas Loop

DS1 H-I. Song¹, H. Choi^{1,2}, J. Y. Yoo¹, H-S. Won¹, C. M. Lee¹, H. Jin¹, T. Y. Kim¹, W. Kwon², K. Lim¹, K. Kwon¹, C-A. Kim¹, T. Kim¹, J. G. Jo¹, J. Eu¹, S. Park¹, H-M. Bae²

¹Point2 technology, Seoul, Korea; ²KAIST, Daejeon, Korea

NAND Flash Memory

Session Chair: *Violante Moschiano, Micron Semiconductor, Avezzano, Italy*
Session Co-Chair: *Seung-Jae Lee, Samsung, Hwasung-si, Kyeonggi-do, Korea*

8:30 AM

7.1 A 1-Tb 4b/Cell 4-Plane 162-Layer 3D Flash Memory with a 2.4-Gb/s I/O Speed Interface

J. Yuh¹, J. Li¹, H. Li¹, Y. Oyama¹, C. Hsu¹, P. Anantula¹, S. Jeong¹, A. Amarnath¹, S. Darne¹, S. Bhatia¹, T. Tang¹, A. Arya¹, N. Rastogi¹, N. Ookuma¹, H. Mizukoshi¹, A. Yap¹, D. Wang¹, S. Kim¹, Y. Wu¹, M. Peng¹, J. Lu¹, T. Ip¹, S. Malhotra¹, D. Han¹, M. Okumura¹, J. Liu¹, J. Sohn¹, H. Chibvongodze¹, M. Balaga¹, A. Matsuda¹, C. Puri¹, C. Chen¹, I. K V¹, C. G¹, V. Ramachandra¹, Y. Kato¹, R. Kumar¹, H. Wang¹, F. Moogata¹, I. Yoon¹, K. Kanda², T. Shimizu², N. Shibata², T. Shigeoka², K. Yanagidaira², T. Kodama², R. Fukuda², Y. Hirashima², M. Abe²

¹Western Digital, Milpitas, CA

²KIOXIA Corporation, Yokohama, Japan

8:40 AM

7.2 A 1-Tb Density 4b/Cell 3D-NAND Flash on 176-Tier Technology with 4-Independent Planes for Read using CMOS-Under-the-Array

T. Pekny¹, L. Vu¹, J. Tsai¹, D. Srinivasan¹, E. Yu¹, J. Pabustan¹, J. Xu¹, S. Deshmukh¹, K-F. Chan¹, M. Piccardi¹, K. Xu¹, G. Wang¹, K. Shakeri¹, V. Patel¹, T. Iwasaki¹, T. Wang¹, P. Musunuri¹, C. Gu¹, A. Mohammadzadeh¹, A. Ghalam¹, V. Moschiano², T. Val², J. Park¹, J. Lee¹, R. Ghodsi¹

¹Micron Technology, San Jose, CA

²Micron Technology, Avezzano, Italy

8:50 AM

7.3 A 1-Tb, 4b/Cell, 176-Stacked-WL 3D-NAND Flash Memory with Improved Read Latency and a 14.8Gb/mm² Density

W. Cho, J. Jung, J. Kim, J. Ham, S. Lee, Y. Noh, D. Kim, W. Lee, K. Cho, K. Kim, H. Lee, S. Chai, E. Jo, H. Cho, J-S. Kim, C. Kwon, C. Park, H. Nam, H. Won, T. Kim, K. Park, S. Oh, J. Ban, J. Park, J. Shin, T. Shin, J. Jang, J. Mun, J. Choi, H. Choi, S-W. Choi, W. Park, D. Yoon, M. Kim, J. Lim, C. An, H. Shim, H. Oh, H. Park, S. Shim, H. Huh, H. Choi, S. Lee, J. Sim, K. Gwon, J. Kim, W. Jeong, J. Choi, K-W. Jin
 SK hynix, Icheon, Korea

9:00 AM

7.4 A 1Tb 3b/Cell 8th-Generation 3D-NAND Flash Memory with 164MB/s Write Throughput and a 2.4Gb/s Interface

M. Kim, S. W. Yun, J. Park, H. K. Park, J. Lee, Y. S. Kim, D. Na, S. Choi, Y. Song, J. Lee, H. Yoon, K. Lee, B. Jeong, S. Kim, J. Park, C. A. Lee, J. Lee, J. Lee, J. Y. Chun, J. Jang, Y. Yang, S. H. Moon, M. Choi, W. Kim, J. Kim, S. Yoon, P. Kwak, M. Lee, R. Song, S. Kim, C. Yoon, D. Kang, J-Y. Lee, J. Song

Samsung Electronics, Hwaseong, Korea

9:10 AM

7.5 A 512Gb In-Memory-Computing 3D-NAND Flash Supporting Similar-Vector-Matching DS2 Operations on Edge-AI Devices

H-W. Hu^{1,2}, W-C. Wang^{1,3}, C-K. Chen¹, Y-C. Lee¹, B-R. Lin¹, H-M. Wang¹, Y-P. Lin¹, Y-C. Lin¹, C-C. Hsieh¹, C-M. Hu¹, Y-T. Lai¹, H-S. Chen¹, Y-H. Chang⁴, H-P. Li¹, T-W. Kuo^{3,5}, K-C. Wang¹, M-F. Chang², C-H. Hung¹, C-Y. Lu¹

¹Macronix, Hsinchu, Taiwan

²National Tsing Hua University, Hsinchu, Taiwan

³National Taiwan University, Taipei, Taiwan

⁴Academia Sinica, Taipei, Taiwan

⁵City University of Hong Kong, Hong Kong, China

Plenary Session II — Invited Papers

Session Chair:

Kevin Zhang, *Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan*
ISSCC Conference Chair

Session Co-Chair:

Edith Beigné, *Meta, Menlo Park, CA*
ISSCC International Technical Program Chair

7:00 AM**1.3 The Art of Scaling:****Distributed and Connected to Sustain the Golden Age of Computation**

Inyup Kang, *President, Samsung Electronics, Hwaseong, Korea*

The history of computer was nothing short of a miracle. Thanks to the rapid innovations in semiconductor manufacturing technology, we have started from gigantic machines that filled a whole room, to cheap and tiny microchips that billions of people can afford and keep in their pockets (or should I say, hands?) all day long. Still, even with this level of progress, mobile devices are barely capable of replicating the “brain” of a jellyfish, and the trend shows that we are already hitting our limits in semiconductor scaling. In this paper, we define the Cost-Performance Ratio (CPR) metric that captures the trend in a single equation. We suggest that we shall find solutions in each area of intra-chip, inter-chip, and inter-device level, and highlight the domain-specific computing, 3D packaging, and advanced communication as the main drivers to the next level of computing, satisfying humans’ unquenchable greed.

7:20 AM**ISSCC, SSCS, IEEE Award Presentations****7:45 AM****1.4 The Future of the High-Performance Semiconductor Industry and Design**

Renée James, *Founder, Chairman, & CEO, Ampere Computing, Santa Clara, CA*

While the explosive growth of today’s modern cloud was fueled by high performance, present-day efficient modern cloud services have moved to a new phase of compute that require scalability and elasticity, while still achieving the highest performance levels to run a myriad of cloud services. The new breed of software underlying today’s cloud services is initiating a third phase of compute unencumbered by architectural complexity designed for client- and server-enterprise applications. Initially, cloud computing was able to leverage traditional processor architectures to deliver value to the end customers. However, massive adoption of cloud-based services has amplified the limitations of the incumbent architectures that were designed for a very different software model in client-server enterprises. The requirement of high-performance for cloud computing has fundamentally changed from one of peak performance at a CPU-level to overall performance at the system-level. This system-level performance refers to maximizing system-level throughput while staying within or further reducing power and cost envelopes, and with much higher emphasis on predictable and consistent performance. This cloud-driven computing requires a fundamental shift in the processor, as well as in SOC architectures and designs, and demands continued innovation to stay ahead of cloud computing growth for the next decade. These innovations need to address the entire vertical stack from software, architecture, design, to packaging and manufacturing domains. The paper will discuss a new approach in architectural thinking and design based on cloud computing as the driving force for demand.

Advanced RF Building Blocks

Session Chair: Hua Wang, *ETH Zurich, Zurich, Switzerland, Switzerland*

Session Co-Chair: Masoud Babaie, *Delft University of Technology, Delft, The Netherlands*

8:30 AM

8.1 A 0.0078mm² 3.4mW Wideband Positive-Feedback-Based Noise-Cancelling LNA in 28nm CMOS Exploiting G_m Boosting

Z. Liu, C. C. Boon, C. Li, K. Yang, Y. Dong, T. Guo

Nanyang Technological University, Singapore, Singapore

8:40 AM

DS1 8.2 A 2-to-2.48GHz Voltage-Interpolator-Based Fractional-N Type-I Sampling PLL in 22nm FinFET Assisting Fast Crystal Startup

S. Kundu, T. Huusari, H. Luo, A. Agrawal, E. Alban, S. Shahraini, T. Xiong, D. Lake, S. Pellerano, J. Mix, N. Kurd, M. Abdel-moneum, B. Carlton

Intel, Hillsboro, OR

8:50 AM

8.3 A 9-to-12GHz Coupled-RTWO FMCW ADPLL with 97fs RMS Jitter, -120dBc/Hz PN at 1MHz Offset, and with Retrace Time of 12.5ns and 2 μ s Chirp Settling Time

H. Shanan¹, D. Dalton², V. Chillara³, P. Dato⁴

¹Analog Devices, Somerset, NJ

²Xilinx, Cork, Ireland

³Vishay, Cork, Ireland

⁴Bosch, Valencia, Spain

High-Quality GHz-to-THz Frequency Generation and RadiationSession Chair: Conan Zhan, *MediaTek, Hsinchu, Taiwan*Session Co-Chair: Swami Sankaran, *Texas Instruments, Dallas, TX*

9:00 AM

9.1 Series-Resonance BiCMOS VCO with Phase Noise of -138dBc/Hz at 1MHz Offset from 10GHz and -190dBc/Hz FoM*A. Franceschin, D. Riccardi, A. Mazzanti*

University of Pavia, Pavia, Italy

9:10 AM

9.2 A 0.049mm² 7.1-to-16.8GHz Dual-Core Triple-Mode VCO Achieving 200dB FoM_A in 22nm FinFET*J. Gong^{1,2}, B. Patra³, L. Enthoven^{1,2}, J. V. Staveren^{1,2}, F. Sebastiano^{1,2}, M. Babaie^{1,2}*¹Delft University of Technology, Delft, The Netherlands²QuTech, Delft, The Netherlands³Intel, Hillsboro, OR

9:20 AM

9.3 A 53.6-to-60.2GHz Many-Core Fundamental Oscillator with Scalable Mesh Topology Achieving -136.0dBc/Hz Phase Noise at 10MHz Offset and 190.3dBc/Hz Peak FoM in 65nm CMOS*H. Jia, R. Ma, W. Deng, Z. Wang, B. Chi*

Tsinghua University, Beijing, China

9:30 AM

9.4 A Highly Power Efficient 2×3 PIN-Diode-Based Intercoupled THz Radiating Array at 425GHz with 18.1dBm EIRP in 90nm SiGe BiCMOS*S. Razavian¹, A. Babakhan²*¹University of California, Los Angeles, CA²University of California, Los Angeles

Nyquist and Incremental ADCsSession Chair: Jan Westra, *Broadcom, Bunnik, The Netherlands*Session Co-Chair: Ping Gui, *Southern Methodist University, Dallas, TX*

8:30 AM

10.1 A 10GS/s 8b 25fJ/c-s 2850 μ m² Two-Step Time-domain ADC Using Delay-Tracking Pipelined-SAR TDC with 500fs Time Step in 14nm CMOS Technology*J. Liu, M. Hassanpourghadi, M. S-W. Chen*

University of Southern California, Los Angeles, CA

8:40 AM

10.2 A 0.82mW 14b 130MS/s Pipelined-SAR ADC with a Distributed Averaging Correlated Level Shifting (DACLS) Ringamp and Bypass-Window Backend*J-C. Wang, T-H. Kuo*

National Cheng Kung University, Tainan, Taiwan

8:50 AM

10.3 A 0.004mm² 200MS/s Pipelined SAR ADC with kT/C Noise Cancellation and Robust Ring-Amp*M. Zhan¹, L. Jie¹, X. Tang², N. Sun¹*¹Tsinghua University, Beijing, China²Peking University, Beijing, China

9:00 AM

10.4 A 0.97mW 260MS/s 12b Pipelined-SAR ADC with Ring-TDC-Based Fine Quantizer for PVT Robust Automatic Cross-Domain Scale Alignment*H. Zhao, F. F. Dai*

Auburn University, Auburn, AL

9:10 AM

10.5 A 24b 2MS/s SAR ADC with 0.03ppm INL and 106.3dB DR in 180nm CMOS*J. Steensgaard¹, R. Reay², R. Perry², D. Thomas², G. Tu², G. Reitsma²*¹Analog Devices, Sequim, WA²Analog Devices, Santa Clara, CA

9:20 AM

10.6 A 4.96 μ W 15b Self-Timed Dynamic-Amplifier-Based Incremental Zoom ADC*Y. Liu¹, M. Zhao¹, Y. Zhao¹, X. Yu¹, N. N. Tan¹, L. Ye², Z. Tan¹*¹Zhejiang University, Hangzhou, China²Peking University, Beijing, China

9:30 AM

10.7 A 0.014mm² 10kHz-BW Zoom-Incremental-Counting ADC Achieving 103dB SNDR and 100dB Full-Scale CMRR*L. Jie¹, M. Zhan¹, X. Tang², N. Sun¹*¹Tsinghua University, Beijing, China²Peking University, Beijing, China

Compute-in-Memory and SRAM

Session Chair: Eric Karl, Intel, Portland, OR

Session Co-Chair: Yasuhiko Taito, Renesas Electronics Corporation, Kodaira, Japan

8:30 AM

11.1 **DS2** A 1ynm 1.25V 8Gb, 16Gb/s/pin GDDR6-based Accelerator-in-Memory supporting 1TFLOPS MAC Operation and Various Activation Functions for Deep-Learning Applications

S. Lee, K. Kim, S. Oh, J. Park, G. Hong, D. Ka, K. Hwang, J. Park, K. Kang, J. Kim, J. Jeon, N. Kim, Y. Kwon, K. Vladimir, W. Shin, J. Won, M. Lee, H. Joo, H. Choi, J. Lee, D. Ko, Y. Jun, K. Cho, I. Kim, C. Song, C. Jeong, D. Kwon, J. Jang, I. Park, J. Chun, J. Cho, SK hynix, Icheon, Korea

8:40 AM

11.2 A 22nm 4Mb STT-MRAM Data-Encrypted Near-Memory Computation Macro with a 192GB/s Read-and-Decryption Bandwidth and 25.1-55.1TOPS/W 8b MAC for AI Operations

Y-C. Chiu^{*1}, C-S. Yang^{*1}, S-H. Teng¹, H-Y. Huang¹, F-C. Chang¹, Y. Wu¹, Y-A. Chien¹, F-L. Hsieh¹, C-Y. Li¹, G-Y. Lin¹, P-J. Chen¹, T-H. Pan¹, C-C. Lo¹, W-S. Khwa², R-S. Liu¹, C-C. Hsieh¹, K-T. Tang¹, C-P. Lo², Y-D. Chih², T-Y. J. Chang², M-F. Chang^{1,2}, ^{*}Equally-Credited Authors (ECAs)

¹National Tsing Hua University, Hsinchu, Taiwan; ²TSMC, Hsinchu, Taiwan

8:50 AM

11.3 A 40-nm, 2M-Cell, 8b-Precision, Hybrid SLC-MLC PCM Computing-in-Memory Macro with 20.5 - 65.0TOPS/W for Tiny-AI Edge Devices

W-S. Khwa^{*1}, Y-C. Chiu^{*2}, C-J. Jhang², S-P. Huang², C-Y. Lee², T-H. Wen², F-C. Chang², S-M. Yu¹, T-Y. Lee¹, M-F. Chang^{1,2}, ^{*}Equally-Credited Authors (ECAs)

¹TSMC Corporate Research, Hsinchu, Taiwan; ²National Tsing Hua University, Hsinchu, Taiwan

9:00 AM

11.4 An 8-Mb DC-Current-Free Binary-to-8b Precision ReRAM Nonvolatile Computing-in-Memory Macro using Time-Space-Readout with 1286.4 - 21.6TOPS/W for Edge-AI Devices

J-M. Hung¹, Y-H. Huang¹, S-P. Huang¹, F-C. Chang¹, T-H. Wen¹, C-I. Su², W-S. Khwa², C-C. Lo¹, R-S. Liu¹, C-C. Hsieh¹, K-T. Tang¹, Y-D. Chih², T-Y. J. Chang², M-F. Chang^{1,2}

¹National Tsing Hua University, Hsinchu, Taiwan; ²TSMC, Hsinchu, Taiwan

9:10 AM

11.5 Single-Mode CMOS 6T-SRAM Macros with Keeper-Loading-Free Peripherals and Row-Separate Dynamic Body Bias Achieving 2.53fW/bit Leakage for AIoT Sensing Platforms

Y. Zhang¹, C. Xue¹, X. Wang¹, T. Liu¹, J. Gao¹, P. Chen¹, J. Liu², L. Sun², L. Shen¹, J. Ru¹, L. Ye^{1,3}, R. Huang¹

¹Peking University, Beijing, China; ²Nano Core Chip Electronic Technology, Hangzhou, China

³Advanced Institute of Information Technology of Peking University, Hangzhou, China

9:20 AM

11.6 A 5-nm 254-TOPS/W 221-TOPS/mm² Fully-Digital Computing-in-Memory Macro Supporting Wide-Range Dynamic-Voltage-Frequency Scaling and Simultaneous MAC and Write Operations

H. Fujiwara¹, H. Mori¹, W-C. Zhao¹, M-C. Chuang¹, R. Naous², C-K. Chuang¹, T. Hashizume³, D. Sun¹, C-F. Lee¹, K. Akarvardar², S. Adham⁴, T-L. Chou¹, M. E. Sinangil², Y. Wang¹, Y-D. Chih¹, Y-H. Chen¹, H-J. Liao¹, T-Y. J. Chang¹

¹TSMC, Hsinchu, Taiwan; ²TSMC, San Jose, CA; ³TSMC, Yokohama, Japan; ⁴TSMC, Austin, TX

9:30 AM

11.7 **DS2** A 1.041-Mb/mm² 27.38-TOPS/W Signed-INT8 Dynamic-Logic-Based ADC-less SRAM Compute-In-Memory Macro in 28nm with Reconfigurable Bitwise Operation for AI and Embedded Applications

B. Yan¹, J-L. Hsu², P-C. Yu², C-C. Lee², Y. Zhang³, W. Yue¹, G. Me², Y. Yang¹, Y. Yang², H. Li⁴, Y. Chen⁴, R. Huang¹,

¹Peking University, Beijing, China; ²NeoNexus, Singapore, Singapore

³Pimchip Technology, Beijing, China; ⁴Duke University, Durham, NC

9:40 AM

11.8 A 28nm 1Mb Time-Domain Computing-in-Memory 6T-SRAM Macro with a 6.6ns Latency, 1241GOPS and 37.01TOPS/W for 8b-MAC Operations for Edge-AI Devices

P-C. Wu^{*1}, J-W. Su^{*2}, Y-L. Chung¹, L-Y. Hong¹, J-S. Ren¹, F-C. Chang¹, Y. Wu¹, H-Y. Chen¹, C-H. Lin¹, H-M. Hsiao², S-H. Li², S-S. Sheu², S-C. Chang², W-C. Lo², C-C. Lo¹, R-S. Liu¹, C-C. Hsieh¹, K-T. Tang¹, C-I. Wu², M-F. Chang¹

^{*}Equally-Credited Authors (ECAs)

¹National Tsing Hua University, Hsinchu, Taiwan; ²Industrial Technology Research Institute, Hsinchu, Taiwan

Monolithic System for Robot and Bio Applications

Session Chair: Milin Zhang, *Tsinghua University, Beijing, China*

Session Co-Chair: Daniel Morris, *Meta, Menlo Park, CA*

8:30 AM

12.1 A 210 × 340 × 50µm Integrated CMOS System for Micro-Robots with Energy Harvesting, Sensing, Processing, Communication and Actuation

L. Xu¹, M. Lassiter², X. Wu¹, Y. Kim¹, J. Lee¹, M. Yasuda³, M. Kawaminami⁴, M. Miskin², D. Blaauw¹, D. Sylvester¹

¹University of Michigan, Ann Arbor, MI; ²University of Pennsylvania, Philadelphia, PA

³United Semiconductor Japan, Kuwana, Japan; ⁴United Semiconductor Japan, Yokohama, Japan

8:40 AM

12.2 A 200 x 256 Image Sensor Heterogeneously Integrating a 2D Nanomaterial-Based Photo-FET Array and CMOS Time-to-Digital Converters

H. Hinton¹, H. Jang¹, W. Wu¹, M-H. Lee², M. Seo², H-J. Shin², S. Park², D. Ham¹

¹Harvard University, Cambridge, MA; ²Samsung Advanced Institute of Technology, Suwon, Korea

8:50 AM

12.3 A Self-powering Wireless Soil-pH and Electrical Conductance Monitoring IC with Hybrid Microbial Electrochemical and Photovoltaic Energy Harvesting

C-Y. Wu¹, C-W. Liu¹, J-S. Chen¹, C-S. Huang¹, T-H. Lu¹, L-C. Chen¹, I-C. Ou¹, S-K. Lee², Y-C. Chen², P-H. Chen¹, C-T. Liu², Y-C. Liao², Y-T. Liao¹

¹National Yang Ming Chiao Tung University, Hsinchu, Taiwan

²National Taiwan University, Taipei, Taiwan

9:00 AM

12.4 A 256-Channel Actively-Multiplexed µECoG Implant with Column-Parallel Incremental $\Delta\Sigma$ ADCs Employing Bulk-DACs in 22-nm FDSOI Technology

X. Huang^{1,2}, H. Londoño-Ramírez^{1,2,3}, M. Ballini^{1,4}, C. Van Hoof^{1,2}, J. Genoe^{1,2}, S. Haesler^{1,2,3,5}, G. Gielen^{1,2}, N. Van Helleputte¹, C. Mora Lopez¹

¹imec, Leuven, Belgium; ²KU Leuven, Leuven, Belgium

³Neuroelectronics Research Flanders, Leuven, Belgium; ⁴now with TDK InvenSense, Milan, Italy

⁵Vlaams Instituut voor Biotechnologie, Leuven, Belgium

9:10 AM

12.5 A CMOS Cellular Interface Array for Digital Physiology Featuring High-Density Multi-Modal Pixels and Reconfigurable Sampling Rate

DS1

*A. Y. Wang^{*1}, Y. Sheng^{*1}, W. Li², D. Jung³, G. Junek¹, J. Park⁴, D. Lee¹, M. Wang², S. Maharjan², S. Kumashi¹, J. Hao², Y. S. Zhang², K. Eggan⁵, H. Wang^{1,6}*

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¹Georgia Institute of Technology, Atlanta, GA

²Brigham and Women's Hospital, Harvard University, Cambridge, MA; ³Qualcomm, San Diego, CA

⁴Intel, Hillsboro, OR; ⁵Harvard University, Cambridge, MA; ⁶ETH Zürich, Zurich, Switzerland

9:20 AM

12.6 A CMOS Molecular Electronics Chip for Single-Molecule Biosensing

DS1

D. A. Hall¹, N. Ananthapadmanabhan², C. Cho², L. Zheng², P. P. Pan², C. W. Fuller², P. P. Padayatti², C. Gardner², D. Gebhardt², Z. Majzik², P. Sinha², P. W. Mola², B. Merriman²

¹University of California, San Diego, CA; ²Roswell Biotechnology, San Diego, CA

9:30 AM

12.7 1024 3D-Stacked Monolithic NEMS Array with 375µm2 0.5mW 0.28ppm Frequency Deviation Pixel-level Readout for Zeptogram Gravimetric Sensing

G. Billiot, P. Mattei, B. Vysotskyi, A. Reynaud, L. Hutin, C. Plantier, E. Rolland, M. Gely, G. Usai, C. Tabone, G. Pillonnet, S. Robinet, S. Hentz

CEA-Léti, Grenoble, France

Digital Techniques for Clocking, Variation Tolerance and Power Management

Session Chair: Tanay Karnik, *Intel, Hillsboro, OR*

Session Co-Chair: Ping-Hsuan Hsieh, *National Tsing Hua University, Hsinchu, Taiwan*

8:30 AM

13.1 Clock Generator with ISO26262 ASIL-D Grade Safety Mechanism for SoC Clocking Application

D. Lim, S. Shin, S. Lee, K. Kwon, J. An, W. Yu, C. Jeong, W. Kim, M. Choi, J. Shin
Samsung Electronics, Hwaseong, Korea

8:40 AM

13.2 A 97fs_{rms}-Jitter and 68-Multiplication Factor, 8.16GHz Ring-Oscillator Injection-Locked Clock Multiplier with Power-Gating Injection-Locking and Background Multi-Functional Digital Calibrator

*S. Park*¹, S. Yoo*², Y. Shin¹, J. Lee¹, J. Choi¹*

*Equally-Credited Authors (ECAs)

¹KAIST, Daejeon, Korea; ²Qualcomm, San Diego, CA

8:50 AM

13.3 A 0.021mm² 65nm CMOS 2.5GHz Digital Injection-Locked Clock Multiplier with Injection Pulse Shaping Achieving -79dBc Reference Spur and 0.496mW/GHz Power Efficiency

R. Xu¹, D. Ye¹, S. Li¹, C.-J. R. Shi²

¹Fudan University, Shanghai, China; ²University of Washington, Seattle, WA

9:00 AM

13.4 Fully Automated Hardware-Driven Clock-Gating Architecture with Complete Clock Coverage for 5nm Exynos Mobile SoC

J.-G. Lee, H. Jeon, Y. Choi, A. Kim, Samsung Electronics, Hwaseong, Korea

9:10 AM

13.5 Deterministic Frequency Boost and Voltage Enhancements on the POWER10™ Processor

B. T. Vanderpool¹, P. J. Restle², E. J. Fluhr³, G. S. Still⁴, F. Campisano³, I. Carmichael³, E. Marz⁵, R. Batra³, R. Willaman³

¹IBM, Rochester, MN; ²IBM, Yorktown Heights, NY; ³IBM, Austin, TX

⁴IBM, Research Triangle Park, NC; ⁵IBM, Essex Junction, VT

9:20 AM

13.6 A 0.65V 1316μm² Fully Synthesizable Digital Temperature Sensor Using Wire Metal Achieving 0.16nJ-%²-Accuracy FoM in 5nm FinFET CMOS

J. Park, J. Kim, K. Kim, J.-H. Yang, M. Choi, J. Shin, Samsung Electronics, Gyeonggi, Korea

9:30 AM

13.7 Energy Minimization of Duty-Cycled Systems Through Optimal Stored-Energy Recycling from Idle Domains

C.-H. Huang¹, A. Mandal¹, D. Peña-Colaiocco¹, E. Pereira Da Silva², V. Sathé¹

¹University of Washington, Seattle, WA; ²NXP Semiconductors, Austin, TX

9:40 AM

13.8 A 194nW Energy-Performance-Aware IoT SoC Employing a 5.2nW 92.6% Peak Efficiency Power Management Unit for System Performance Scaling, Fast DVFS and Energy Minimization

X. Liu, S. Kamineni, J. Breiholz, B. H. Calhoun, S. Li, University of Virginia, Charlottesville, VA

GaN, High-Voltage and Wireless Power

Session Chair: Bernhard Wicht, *University of Hannover, Hannover, Germany*

Session Co-Chair: Patrik Arno, *ST Microelectronics, Grenoble, France, Metropolitan*

8:30 AM

14.1 A Monolithic GaN-Based Driver and GaN Power HEMT with Diode-Emulated GaN Technique for 50MHz Operation and Sub-0.2ns Deadtime Control

Y-Y. Kao¹, T-W. Wang¹, S-H. Hung¹, Y-H. Wen¹, T-H. Yang¹, S-Y. Li¹, K-H. Chen¹, Y-H. Lin², S-R. Lin², T-Y. Tsa²

¹National Yang Ming Chiao Tung University, Hsinchu, Taiwan

²Realtek Semiconductor, Hsinchu, Taiwan

8:40 AM

14.2 A 110V/230V 0.3W Offline Chip-Scale Power Supply with Integrated Active Zero-Crossing Buffer and Voltage-Interval-Based Dual-Mode Control

C. Rindfleisch, B. Wicht, Leibniz University Hannover, Hannover, Germany

8:50 AM

14.3 A Monolithic GaN Direct 48V/1V AHB Switching Power IC with Auto-Lock Auto-Break Level Shifting, Self-Bootstrapped Hybrid Gate Driving, and On-Die Temperature Sensing

D. Yan, D. B. Ma, University of Texas, Dallas, TX

9:00 AM

14.4 A 2.5–5MHz 87% Peak Efficiency 48V-to-1V Integrated Hybrid DC-DC Converter Adopting Ladder SC Network with Capacitor Assisted Dual Inductor Filtering

C. Chen, J. Liu, H. Lee, University of Texas, Dallas, TX

9:10 AM

14.5 2-Tx Digital Envelope-Tracking Supply Modulator Achieving 200MHz Channel Bandwidth and 93.6% Efficiency for 2G/3G/LTE/NR RF Power Amplifiers

J-S. Bang, D. Kim, J. Lee, S. Jung, Y. Choo, S. Park, Y-H. Jung, J-Y. Ko, T. Nomiyama, J. Baek, J. Han, S-H. Lee, I-H. Kim, J-S. Paek, J. Lee, T. B. Cho

Samsung Electronics, Hwaseong, Korea

9:20 AM

14.6 A 27W D2D Wireless Power Transfer System with Compact Single-Stage Regulated Class-E Architecture and Adaptive ZVS Control

X. Ma^{1,2}, Y. Lu², W-H. Ki¹

¹Hong Kong University of Science and Technology, Hong Kong, China

²University of Macau, Macau, China

9:30 AM

14.7 A 1.2W 51%-Peak-Efficiency Isolated DC-DC Converter with a Cross-Coupled Shoot-Through-Free Class-D Oscillator Meeting the CISPR-32 Class-B EMI Standard

D. Pan¹, G. Li¹, F. Miao¹, W. Sun¹, X. Gong², L. Zhang², L. Cheng¹

¹University of Science and Technology of China, Hefei, China

²Suzhou Novosense Microelectronics, Suzhou, China

9:40 AM

14.8 A 68.3% Efficiency Reconfigurable 400-/800-mW Capacitive Isolated DC-DC Converter with Common-Mode Transient Immunity and Fast Dynamic Response by Through-Power-Link Hysteretic Control

J. Tang, L. Zhao, C. Huang, Iowa State University, Ames, IA

Highlighted Chip Releases: Digital/ML

Session Chair: Dennis Sylvester, *University of Michigan, Ann Arbor, MI*

Session Co-Chair: Thomas Burd, *AMD, Santa Clara, CA*

21.1 SambaNova SN10 RDU: A 7nm Dataflow Architecture to Accelerate Software 2.0

R. Prabhakar, S. Jairath, J. L. Shin
SambaNova Systems, Palo Alto, CA

21.2 A64FX: 52-Core Processor Designed for the 442PetaFLOPS Supercomputer Fugaku

S. Yamamura, Y. Akizuki, H. Sekiguchi, T. Maruyama, T. Sano, H. Miyazaki, T. Yoshida
Fujitsu, Kawasaki, Japan

21.3 Bonanza Mine: An Ultra-Low-Voltage Energy-Efficient Bitcoin Mining ASIC

DS2 *V. B. Suresh¹, C. S. Katta², S. Rajagopalan², T. Z. Zhou³, A. Pate¹, R. Rakha², N. K. Gopalakrishna², S. Mathew¹, A. Hukko²*

¹Intel, Hillsboro, OR

²Intel, Santa Clara, CA

³Intel, San Diego, CA

21.4 The Wormhole AI Training Processor

D. Ignjatovic, D. W. Bailey, L. Bajic
Tenstorrent, Toronto, Canada

7:00-7:45
Panel Q&A

This year, Demonstration Session 1 extending in selected regular papers, both Academic and Industrial, will take place on Wednesday, February 23rd starting at 7:00 am. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2022, as noted by the symbol **DS1**

- 3.8 **A BJT-Based CMOS Temperature Sensor Achieving an Inaccuracy of $\pm 0.45^{\circ}\text{C}$ (3σ) from -50°C to 180°C and a Resolution-FoM of $7.2\text{pJ}\cdot\text{K}^2$ at 150°C**
- 4.1 **Fully Integrated 2D Scalable TX/RX Chipset for D-Band Phased-Array-on-Glass Modules**
- 4.5 **Electronic THz Pencil Beam Forming and 2D Steering for High Angular-Resolution Operation: A 98×98 -Unit 265GHz CMOS Reflectarray with In-Unit Digital Beam Shaping and Squint Correction**
- 5.2 **A 64×64 -Pixel Flash LiDAR SPAD Imager with Distributed Pixel-to-Pixel Correlation for Background Rejection, Tunable Automatic Pixel Sensitivity and First-Last Event Detection Strategies for Space Applications**
- 5.3 **An 80×60 Flash LiDAR Sensor with In-Pixel Histogramming TDC Based on Quaternary Search and Time-Gated Δ -Intensity Phase Detection for 45m Detectable Range and Background Light Cancellation**
- 5.9 **A 10b Source-Driver IC with LSB-Stacked LV-to-HV-Amplify DAC Achieving $2688\mu\text{m}^2/\text{channel}$ and 4.8mV DVO for Mobile OLED Displays**
- 6.1 **A 1.41pJ/b 224Gb/s PAM-4 SerDes Receiver with 31dB Loss Compensation**
- 6.7 **A 50Gb/s PAM-4 Bi-Directional Plastic Waveguide Link with Carrier Synchronization Using PI-Based Costas Loop**
- 8.2 **A 2-to-2.48GHz Voltage-Interpolator-Based Fractional-N Type-I Sampling PLL in 22nm FinFET Assisting Fast Crystal Startup**
- 12.5 **A CMOS Cellular Interface Array for Digital Physiology Featuring High-Density Multi-Modal Pixels and Reconfigurable Sampling Rate**
- 12.6 **A CMOS Molecular Electronics Chip for Single-Molecule Biosensing**
- 14.2 **A 110V/230V 0.3W Offline Chip-Scale Power Supply with Integrated Active Zero-Crossing Buffer and Voltage-Interval-Based Dual-Mode Control**
- 18.5 **A 12 A Imax, Fully Integrated Multi-Phase Voltage Regulator with 91.5% Peak Efficiency at 1.8 to 1V, Operating at 50 MHz and Featuring a Digitally Assisted Controller with Automatic Phase Shedding and Soft Switching in 4nm Class FinFET CMOS**
- 19.3 **A 28GHz Compact 3-Way Transformer-Based Parallel-Series Doherty Power Amplifier with 20.4%/14.2% PAE at 6-/12-dB Power Back-Off and $25.5\text{dBm } P_{\text{SAT}}$ in 55nm Bulk CMOS**
- 20.2 **A Time-Division Multiplexed 8-Channel Non-Contact ECG Recording IC with a Common-Mode Interference Tolerance of $20V_{\text{PP}}$**
- 25.6 **An 84dB-SNDR Low-OSR 4th-Order Noise-Shaping SAR with an FIA-Assisted EF-CRFF Structure and Noise-Mitigated Push-Pull Buffer-in-Loop Technique**
- 32.1 **BatDrone: A 9.83M-focal-points/s 7.76 μs -Latency Ultrasound Imaging System with On-Chip Per-Voxel RX Beamfocusing for 7m-Range Drone Applications**

Highlighted Chip Releases: Systems and Quantum Computing

Session Chair: **Fabio Sebastiano**, *Delft University of Technology, Delft, The Netherlands*

Session Co-Chair: *Alice Wang, Everactive, Plano, TX*

26.1 Beyond-Classical Computing Using Superconducting Quantum Processors

J. Bardin^{1,2}

¹Google Quantum AI, Goleta, CA

²University of Massachusetts, Amherst, MA

26.2 Design Considerations for Superconducting Quantum Systems

*G. Zettles^{*1}, S. Willenborg^{*1}, B. Johnson², A. Wack², B. Allison¹*

^{*}Equally-Credited Authors (ECAs)

¹IBM, Rochester, MN

²IBM, Yorktown Heights, NY

26.3 Augmented Reality – The Next Frontier of Image Sensors and Compute Systems

C. Liu, S. Chen, T-H. Tsai, B. De Salvo, J. Gomez

Meta Reality Labs, Redmond, WA

26.4 3D V-Cache: The Implementation of a Hybrid-Bonded 64MB Stacked Cache for a 7nm x86-64 CPU

*J. Wu¹, R. Agarwal², M. Ciraula¹, C. Dietz¹, B. Johnson¹, D. Johnson¹, R. Schreiber³,
R. Swaminathan³, W. Walker¹, S. Naffziger¹*

¹AMD, Fort Collins, CO

²AMD, Santa Clara, CA

³AMD, Austin, TX

7:45 - 8:30
Panel Q&A

This year, Demonstration Session 2 extending in selected regular papers, both Academic and Industrial, will take place on Wednesday, February 23rd starting at 7:45 am. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2022, as noted by the symbol **DS2**

- 2.7 Zen3: The AMD 2nd-Generation 7nm x86-64 Microprocessor Core**
- 4.3 A 140GHz Transceiver with Integrated Antenna, Inherent-Low-Loss Duplexing and Adaptive Self-Interference Cancellation for FMCW Monostatic Radar**
- 7.5 A 512Gb In-Memory-Computing 3D-NAND Flash Supporting Similar-Vector-Matching Operations on Edge-AI Devices**
- 11.1 A 1ynm 1.25V 8Gb, 16Gb/s/pin GDDR6-based Accelerator-in-Memory supporting 1TFLOPS MAC Operation and Various Activation Functions for Deep-Learning Applications**
- 11.7 A 1.041-Mb/mm² 27.38-TOPS/W Signed-INT8 Dynamic-Logic-Based ADC-less SRAM Compute-In-Memory Macro in 28nm with Reconfigurable Bitwise Operation for AI and Embedded Applications**
- 15.4 Hiddenite: 4K-PE Hidden Network Inference 4D-Tensor Engine Exploiting On-Chip Model Construction Achieving 34.8-to-16.0TOPS/W for CIFAR-100 and ImageNet**
- 15.8 Analog Matrix Processor for Edge AI Real-Time Video Analytics**
- 16.3 A 40nm 60.64TOPS/W ECC-Capable Compute-in-Memory/Digital 2.25MB/768KB RRAM/SRAM System with Embedded Cortex M3 Microprocessor for Edge Recommendation Systems**
- 16.4 Flex6502: A Flexible 8b Microprocessor in 0.8 μ m Metal-Oxide Thin-Film Transistor Technology Implemented with a Complete Digital Design Flow Running Complex Assembly Code**
- 16.6 A 65nm 63.3 μ W 15Mbps Transceiver with Switched-Capacitor Adiabatic Signaling and Combinatorial-Pulse-Position Modulation for Body-Worn Video-Sensing AR Nodes**
- 21.3 Bonanza Mine: An Ultra-Low-Voltage Energy-Efficient Bitcoin Mining ASIC**
- 24.2 A 1.66Gb/s and 5.8pJ/b Transcutaneous IR-UWB Telemetry System with Hybrid Impulse Modulation for Intracortical Brain-Computer Interfaces**
- 27.3 A 24-to-30GHz 256-Element Dual-Polarized 5G Phased Array with Fast Beam-Switching Support for >30,000 Beams**
- 33.1 A 1.05A/m Minimum Magnetic Field Strength Single-Chip Fully Integrated Biometric Smart Card SoC Achieving 1014.7ms Transaction Time with Anti-Spoofing Fingerprint Authentication**
- 33.3 A HD 31fps 7 \times 7-View Light-Field Factorization Processor for Dual-Layer 3D Factored Display**
- 33.4 DSPU: A 281.6mW Real-Time Depth Signal Processing Unit for Deep Learning-Based Dense RGB-D Data Acquisition with Depth Fusion and 3D Bounding Box Extraction in Mobile Platforms**
- 34.3 A Threshold-Implementation-Based Neural-Network Accelerator Securing Model Parameters and Inputs Against Power Side-Channel Attacks**

ML Processors

Session Chair: SukHwan Lim, Samsung Electronics, Hwaseong-si, Korea

Session Co-Chair: Sophia Shao, University of California, Berkeley, Berkeley, CA

8:30 AM

15.1 A Multi-Mode 8K-MAC HW-Utilization-Aware Neural Processing Unit with a Unified Multi-Precision Datapath in 4nm Flagship Mobile SoCJ-S. Park¹, C. Park¹, S. Kwon¹, H-S. Kim¹, T. Jeon¹, Y. Kang¹, H. Lee¹, D. Lee¹, J. Kim¹, Y. Lee¹, S. Park¹, J-W. Jang², S. Ha¹, M. Kim¹, J. Bang¹, S. H. Lim¹, I. Kang¹¹Samsung Electronics, Hwaseong, Korea²Samsung Advanced Institute of Technology, Suwon, Korea

8:40 AM

15.2 A 65nm Systolic Neural CPU Processor for Combined Deep Learning and General-Purpose Computing with 95% PE Utilization, High Data Locality and Enhanced End-to-End Performance

Y. Ju, J. Gu, Northwestern University, Evanston, IL

8:50 AM

15.3 COMB-MCM: Computing-on-Memory-Boundary NN Processor with Bipolar Bitwise Sparsity Optimization for Scalable Multi-Chiplet-Module Edge Machine LearningH. Zhu^{*1}, B. Jiao^{*1}, J. Zhang^{*1}, X. Jia¹, Y. Wang¹, T. Guan², S. Wang², D. Niu², H. Zheng², C. Chen¹, M. Wang¹, L. Zhang¹, X. Zeng¹, Q. Liu¹, Y. Xie¹, M. Liu¹, *Equally-Credited Authors (ECAs)¹Fudan University, Shanghai, China; ²Alibaba DAMO Academy, Shanghai, China

9:00 AM

DS2 15.4 Hiddenite: 4K-PE Hidden Network Inference 4D-Tensor Engine Exploiting On-Chip Model Construction Achieving 34.8-to-16.0TOPS/W for CIFAR-100 and ImageNetK. Hirose^{*}, J. Yu^{*}, K. Ando, Y. Okoshi, Á. López García-Arias, J. Suzuki, T. V. Chu, K. Kawamura, M. Motomura, *Equally-Credited Authors (ECAs), Tokyo Institute of Technology, Yokohama, Japan

9:10 AM

15.5 A 28nm 29.2TFLOPS/W BF16 and 36.5TOPS/W INT8 Reconfigurable Digital CIM Processor with Unified FP/INT Pipeline and Bitwise In-Memory Booth Multiplication for Cloud Deep Learning AccelerationF. Tu^{1,2}, Y. Wang¹, Z. Wu¹, L. Liang², Y. Ding², B. Kim², L. Liu¹, S. Wei¹, Y. Xie², S. Yin¹¹Tsinghua University, Beijing, China; ²University of California, Santa Barbara, CA

9:20 AM

15.6 DIANA: An End-to-End Energy-Efficient Digital and Analog Hybrid Neural Network SoCK. Ueyoshi¹, I. A. Papistas², P. Houshmand¹, G. M. Sarda^{1,2}, V. Jain¹, M. Shi¹, Q. Zheng¹, S. Giraldo¹, P. Vranckx², J. Doevenspeck², D. Bhattacharjee², S. Cosemans², A. Mallik², P. Debacker², D. Verkest², M. Verhelst^{1,2}, ¹KU Leuven, Leuven, Belgium; ²imec, Leuven, Belgium

9:30 AM

15.7 ARCHON: A 332.7TOPS/W 5b Variation-Tolerant Analog CNN Processor Featuring Analog Neuronal Computation Unit and Analog MemoryJ-D. Seo¹, M. Seok², S. Cho¹, ¹KAIST, Daejeon, Korea; ²Columbia University, New York, NY

9:40 AM

15.8 Analog Matrix Processor for Edge AI Real-Time Video Analytics**DS2** L. Fick¹, S. Skrzyniarz¹, M. Parikh¹, M. B. Henry², D. Fick¹¹Mythic, Austin, TX; ²Mythic, Redwood City, CA

9:50 AM

15.9 A 0.8V Intelligent Vision Sensor with Tiny Convolutional Neural Network and Programmable Weights Using Mixed-Mode Processing-in-Sensor Technique for Image ClassificationT-H. Hsu^{*}, G-C. Chen^{*}, Y-R. Chen, C-C. Lo, R-S. Liu, M-F. Chang, K-T. Tang, C-C. Hsieh

*Equally-Credited Authors (ECAs), National Tsing Hua University, Hsinchu, Taiwan

Emerging Domain-Specific Digital Circuits and Systems

Session Chair: Huichu Liu, *Meta, Menlo Park, CA*

Session Co-Chair: Mijung Noh, *Samsung Electronics, Hwaseong-si, Korea*

8:30 AM

16.1 DIMC: 2219TOPS/W 2569F²/b Digital In-Memory Computing Macro in 28nm Based on Approximate Arithmetic Hardware

D. Wang¹, C-T. Lin¹, G. K. Chen², P. Knag², R. K. Krishnamurthy², M. Seok¹

¹Columbia University, New York, NY

²Intel, Portland, OR

8:40 AM

16.2 A 40nm 64kb 26.56TOPS/W 2.37Mb/mm² RRAM Binary/Compute-in-Memory Macro with 4.23× Improvement in Density and >75% Use of Sensing Dynamic Range

S. D. Spetalnick¹, M. Chang¹, B. Crafton¹, W-S. Khwa², Y-D. Chih³, M-F. Chang², A. Raychowdhury¹

¹Georgia Institute of Technology, Atlanta, GA

²TSMC Corporate Research, Hsinchu, Taiwan

³TSMC Design Technology, Hsinchu, Taiwan

8:50 AM

16.3 A 40nm 60.64TOPS/W ECC-Capable Compute-in-Memory/Digital 2.25MB/768KB RRAM/SRAM System with Embedded Cortex M3 Microprocessor for Edge Recommendation Systems

DS2

M. Chang¹, S. D. Spetalnick¹, B. Crafton¹, W-S. Khwa², Y-D. Chih³, M-F. Chang², A. Raychowdhury¹

¹Georgia Institute of Technology, Atlanta, GA

²TSMC Corporate Research, Hsinchu, Taiwan

³TSMC Design Technology, Hsinchu, Taiwan

9:00 AM

16.4 Flex6502: A Flexible 8b Microprocessor in 0.8μm Metal-Oxide Thin-Film Transistor Technology Implemented with a Complete Digital Design Flow Running Complex Assembly Code

DS2

H. Çeliker^{1,2}, A. Sou³, B. Cobb³, W. Dehaene^{1,2}, K. Myny^{1,2}

¹imec, Leuven, Belgium

²KU Leuven ESAT, Leuven, Belgium

³PragmatIC Semiconductor Ltd, Cambridge, United Kingdom

9:10 AM

16.5 FlexSpin: A Scalable CMOS Ising Machine with 256 Flexible Spin Processing Elements for Solving Complex Combinatorial Optimization Problems

Y. Su¹, T-H. Kim¹, B. Kim²

¹Nanyang Technological University, Singapore, Singapore

²University of California, Santa Barbara, CA

9:20 AM

16.6 A 65nm 63.3μW 15Mbps Transceiver with Switched-Capacitor Adiabatic Signaling and Combinatorial-Pulse-Position Modulation for Body-Worn Video-Sensing AR Nodes

DS2

B. Chatterjee, A. Datta, M. Nath, G. K. K, N. Modak, S. Sen

Purdue University, West Lafayette, IN

9:30 AM

16.7 An Optimal Digital Beamformer for mm-Wave Phased Arrays with 660MHz Instantaneous Bandwidth in 28nm CMOS

D. Peña-Colaiocco, C-H. Huang, K-D. Chu, J. C. Rudell, V. Sathe

University of Washington, Seattle, WA

Advanced Wireline Links and TechniquesSession Chair: **Bo Zhang**, *Broadcom, Irvine, CA*Session Co-Chair: **Wei-Zen Chen**, *National Yang Ming Chiao Tung University, Hsinchu, Taiwan*

8:30 AM

17.1 A 4.6pJ/b 200Gb/s Analog DP-QPSK Coherent Optical Receiver in 28nm CMOS*K. Sheng**, *H. Niu**, *B. Zhang**, *W. Gai*, *B. Ye*, *H. Zhou*, *C. Chen*

*Equally-Credited Authors (ECAs)

Peking University, Beijing, China

8:40 AM

17.2 A 2.4pJ/b 100Gb/s 3D-Integrated PAM-4 Optical Transmitter with Segmented SiP MOSCAP Modulators and a 2-Channel 28nm CMOS Driver*A. Hashemi Talkhoocheh*¹, *W. Zhang*², *M. Wang*¹, *D. J. Thomson*², *M. Ebert*², *L. Ke*², *G. T. Reed*², *A. Emami*¹¹California Institute of Technology, Pasadena, CA²University of Southampton, Southampton, United Kingdom

8:50 AM

17.3 A 10Gb/s Digital Isolator Using Coupled Split-Ring Resonators with 24kVpk Surge Capability and 100kV/ μ S Common-Mode Transient Immunity*J. Xu*, *R. Yun*, *B. Chen*

Analog Devices, Wilmington, MA

9:00 AM

17.4 A 56GHz 23mW Fractional-N PLL with 110fs Jitter*Y. Zhao*, *O. Memioğlu*, *B. Razavi*

University of California, Los Angeles, CA

9:10 AM

17.5 A 480-Multiplication-Factor 13.2-to-17.3GHz Sub-Sampling PLL Achieving 6.6mW Power and -248.1dB FoM Using a Proportionally Divided Charge Pump*L. Zhang*, *A. Niknejad*

University of California, Berkeley, CA

9:20 AM

17.6 A 65nm CMOS, 3.5-to-11GHz, Less-Than-1.45LSB-INL_{pp}, 7b Twin Phase Interpolator with a Wideband, Low-Noise Delta Quadrature Delay-Locked Loop for High-Speed Data Links*Z. Wang*, *P. R. Kinget*

Columbia University, New York, NY

9:30 AM

17.7 A 9b-Linear 14GHz Integrating-Mode Phase Interpolator in 5nm FinFET Process*A. K. Mishra*¹, *Y. Li*², *P. Agarwal*², *S. Shekhar*¹¹University of British Columbia, Vancouver, Canada²MaxLinear, Carlsbad, CA

DC-DC Converters

Session Chair: Harish Krishnamurthy, Intel, Hillsboro, OR

Session Co-Chair: Xun Liu, The Chinese University of Hong Kong, Shenzhen, Shenzhen, China

8:30 AM

- 18.1 A 1.23W/mm² 83.7%-Efficiency 400MHz 6-Phase Fully-Integrated Buck Converter in 28nm CMOS with On-Chip Capacitor Dynamic Re-Allocation for Inter-Inductor Current Balancing and Fast DVS of 75mV/ns**

*J-H. Cho¹, D-K. Kim¹, H-H. Bae¹, Y-J. Lee^{1,2}, S-T. Koh¹, Y. Choo², J-S. Paek², H-S. Kim¹*¹KAIST, Daejeon, Korea; ²Samsung Electronics, Hwaseong, Korea

8:40 AM

- 18.2 A 12V/24V-to-1V DSD Power Converter with 56mV Droop and 0.9 μ s 1% Settling Time for a 3A/20ns Load Transient**

J. Yuan, Z. Liu, F. Wu, L. Cheng

University of Science and Technology of China, Hefei, China

8:50 AM

- 18.3 A 4A 12-to-1 Flying Capacitor Cross-Connected DC-DC Converter with Inserted D>0.5 Control Achieving >2x Transient Inductor Current Slew Rate and 0.73x Theoretical Minimum Output Undershoot of DSD**

*T. Hu¹, M. Huang¹, Y. Lu¹, R. P. Martins^{1,2}*¹University of Macau, Macau, China; ²University of Lisboa, Lisbon, Portugal

9:00 AM

- 18.4 A Monolithic 3:1 Resonant Dickson Converter with Variable Regulation and Magnetic-Based Zero-Current Detection and Autotuning**

P. H. McLaughlin, K. Datta, J. T. Stauth

Dartmouth College, Hanover, NH

9:10 AM

- DS1 18.5 A 12 A I_{max}, Fully Integrated Multi-Phase Voltage Regulator with 91.5% Peak Efficiency at 1.8 to 1V, Operating at 50 MHz and Featuring a Digitally Assisted Controller with Automatic Phase Shedding and Soft Switching in 4nm Class FinFET CMOS**

*C. Schaeff¹, T. Salus², R. Rayess³, S. Kulasekaran⁴, M. Manusharow⁴, K. Radhakrishnan⁴, J. Douglas⁴*¹Intel, Hillsboro, OR; ²Intel, Haifa, Israel; ³Intel, Hudson, MA; ⁴Intel, Chandler, AZ

9:20 AM

- 18.6 A 5V Input 98.4% Peak Efficiency Reconfigurable Capacitive-Sigma Converter with Greater than 90% Peak Efficiency for the Entire 0.4~1.2V Output Range**

X. Yang, L. Zhao, M. Zhao, Z. Tan, L. He, Y. Ding, W. Li, W. Qu

Zhejiang University, Hangzhou, China

9:30 AM

- 18.7 A 2~5MHz Multiple DC Output Hybrid Boost Converter with Scalable CR Boosting Scheme Achieving 91% Efficiency at a Conversion Ratio of 12**

C. Chen, J. Liu, H. Lee

University of Texas, Dallas, TX

9:40 AM

- 18.8 A Battery-Input Sub-1V Output 92.9% Peak Efficiency 0.3A/mm² Current Density Hybrid SC-Parallel-Inductor Buck Converter with Reduced Inductor Current in 65nm CMOS**

*G. Cai¹, Y. Lu¹, R. Martins^{1,2}*¹University of Macau, Macau, China; ²University of Lisboa, Lisbon, Portugal

Power Amplifiers and Building Blocks

Session Chair: Hongtao Xu, Fudan University, Shanghai, China

Session Co-Chair: Yves Baeyens, Nokia - Bell Labs, New Providence, NJ

8:30 AM

19.1 A 110-to-130GHz SiGe BiCMOS Doherty Power Amplifier with Slotline-Based Power-Combining Technique Achieving >22dBm Saturated Output Power and >10% Power Back-Off Efficiency

X. Li¹, W. Chen¹, S. Li¹, H. Wu¹, X. Ye², R. Han³, Z. Feng¹

¹Tsinghua University, Beijing, China

²South China University of Technology, Guangzhou, China

³Massachusetts Institute of Technology, Boston, MA

8:40 AM

19.2 A 1V 32.1dBm 92-to-102GHz Power Amplifier with a Scalable 128-to-1 Power Combiner Achieving 15% Peak PAE in a 65nm Bulk CMOS Process

W. Zhu, J. Wang, R. Wang, J. Zhang, C. Li, S. Yin, Y. Wang

Tsinghua University, Beijing, China

8:50 AM

19.3 A 28GHz Compact 3-Way Transformer-Based Parallel-Series Doherty Power Amplifier with 20.4%/14.2% PAE at 6-/12-dB Power Back-Off and 25.5dBm P_{SAT} in 55nm Bulk CMOS

DS1

Z. Ma^{1,2}, K. Ma¹, K. Wang¹, F. Meng¹

¹Tianjin University, Tianjin, China

²University of Electronic Science and Technology of China, Chengdu, China

9:00 AM

19.4 A 26-to-39GHz Broadband Ultra-Compact High-Linearity Switchless Hybrid N/PMOS Bi-Directional PA/LNA Front-End for Multi-Band 5G Large-Scaled MIMO System

J. Park¹, H. Wang^{1,2}

¹Georgia Institute of Technology, Atlanta, GA

²ETH Zurich, Zurich, Switzerland

9:10 AM

19.5 A 16nm, +28dBm Dual-Band All-Digital Polar Transmitter Based on 4-core Digital PA for Wi-Fi6E Applications

B. Khamaisi¹, D. Ben-Haim¹, A. Nazimov¹, A. Ben-Bassat¹, S. Gross¹, N. Shay¹, G. Asa¹, V. Spector¹, Y. Eilat¹, A. Azam², E. Borokhovich¹, I. Shternberg¹, P. Skliar¹, E. Solomon¹, A. Beidas¹, T. A. Hazira¹, A. Lane¹, E. Shaviv¹, G. Nudelman¹, E. Dahan¹, M. Shemer¹, N. Kimiagarov¹, A. Rav², O. Degani¹

¹Intel, Haifa, Israel

²Intel, Oregon, OR

9:20 AM

19.6 A Broadband Mm-Wave VSWR-Resilient Joint True Power Detector and Impedance Sensor Supporting Single-Ended Antenna Interfaces

D. J. Munzer¹, N. S. Mannem¹, E. Garay¹, H. Wang^{1,2}

¹Georgia Institute of Technology, Atlanta, GA

²ETH Zurich, Zurich, Switzerland

9:30 AM

19.7 A 1-to-18GHz Distributed-Stacked-Complementary Triple-Balanced Passive Mixer With up to 33dBm IIP3 and Integrated LO Driver in 45nm CMOS SOI

C. Hill^{1,2}, J. F. Buckwalter²

¹Lintronic Semiconductors, Somerville, MA

²University of California, Santa Barbara, CA

Body and Brain Interfaces

Session Chair: **Sohmyung Ha**, *New York University Abu Dhabi, Abu Dhabi, United Arab Emirates*

Session Co-Chair: **Rikky Muller**, *University of California, Berkeley, CA*

8:30 AM

- 20.1 A 0.5mΩ/√Hz 106dB SNR 0.45cm² Dry-Electrode Bioimpedance Interface with Current Mismatch Cancellation and Boosted Input Impedance of 100MΩ at 50kHz**
Q. Pan, T. Qu, B. Tang, F. Shan, Z. Hong, J. Xu, Fudan University, Shanghai, China

8:40 AM

- DS1 20.2 A Time-Division Multiplexed 8-Channel Non-Contact ECG Recording IC with a Common-Mode Interference Tolerance of 20V_{pp}**
K-J. Choi, J-Y. Sim, Pohang University of Science and Technology, Pohang, Korea

8:50 AM

- 20.3 A 0.7V 17fJ/step-FOM_W 178.1dB-FOM_{SNDR} 10kHz-BW 560mV_{pp} True-ExG Biopotential Acquisition System with Parasitic-Insensitive 421MΩ Input Impedance in 0.18μm CMOS**
S. Lee¹, Y. Choi¹, G. Kim¹, S. Baik¹, T. Seol¹, H. Jang¹, D. Lee¹, M. Je², J-W. Choi¹, A. K. George¹, J. Lee¹
¹Daegu Gyeongbuk Institute of Science and Technology, Daegu, Korea; ²KAIST, Daejeon, Korea

9:00 AM

- 20.4 A 256-Channel 0.227μJ/class Versatile Brain Activity Classification and Closed-Loop Neuromodulation SoC with 0.004mm²-1.51μW/channel Fast-Settling Highly Multiplexed Mixed-Signal Front-End**
U. Shin^{1,2}, L. Somappa¹, C. Ding¹, B. Zhu^{1,2}, Y. Vyza¹, A. Trouillet¹, S. P. Lacour^{1,3}, M. Shoaran^{1,3}
¹EPFL, Lausanne, Switzerland; ²Cornell University, Ithaca, NY
³Center for Neuroprosthetics, Geneva, Switzerland

9:10 AM

- 20.5 A Miniaturized Wireless Neural Implant with Body-Coupled Data Transmission and Power Delivery for Freely Behaving Animals**
*C. Lee^{*1}, B. Kim^{*2}, J. Kim¹, S. Lee^{3,4}, T. Jeon¹, W. Choi¹, S. Yang^{3,4}, J-H. Ahn¹, J. Bae², Y. Chae¹*
^{*}Equally-Credited Authors (ECAs); ¹Yonsei University, Seoul, Korea
²Kangwon National University, Chuncheon, Korea; ³Incheon National University, Incheon, Korea
⁴gBrain, Incheon, Korea

9:20 AM

- 20.6 A Reconfigurable Sub-Array Multiplexing Microelectrode Array System with 24,320 Electrodes and 380 Readout Channels for Investigating Neural Communication**
J-H. Cha¹, J-H. Park¹, Y. Park¹, H. Shin², K. S. Hwang², I-J. Cho², S-J. Kim¹
¹Ulsan National Institute of Science and Technology, Ulsan, Korea
²Korea Institute of Science and Technology, Seoul, Korea

9:30 AM

- 20.7 An SpO₂ Sensor Using Reconstruction-Free Sparse Sampling for 70% System Power Reduction**
S. Faraji Alamouti¹, C. Yalcin¹, J. Jan¹, J. Ting¹, A. C. Arias¹, R. Muller^{1,2}
¹University of California, Berkeley, CA; ²Chan Zuckerberg Biohub, San Francisco, CA

9:40 AM

- 20.8 A 145.2dB-DR Baseline-Tracking Impedance Plethysmogram IC for Neckband-Based Blood Pressure and Cardiovascular Monitoring**
C. S. Park¹, H. Kim¹, K. Lee¹, D. S. Keum², D. P. Jang³, J. J. Kim¹
¹Ulsan National Institute of Science and Technology, Ulsan, Korea
²SOSO H&C, Daegu, Korea; ³Hanyang University, Seoul, Korea

Cryo-Circuits and Ultra-Low-Power Intelligent IoT

Session Chair: **Sudip Shekhar**, *University of British Columbia, Vancouver, Canada*

Session Co-Chair: **Radu Berdan**, *Kioxia, Tokyo, Japan*

7:00 AM

22.1 A Cryo-CMOS Low-Power Semi-Autonomous Qubit State Controller in 14nm FinFET Technology

D. J. Frank¹, S. Chakraborty¹, K. Tien¹, P. Rosno², T. Fox¹, M. Yeck¹, J. A. Glick¹, R. Robertazzi¹, R. Richetta², J. F. Bulzacchelli¹, D. Ramirez², D. Yilma², A. Davies², R. V. Joshi¹, S. D. Chambers², S. Lekuch¹, K. Inoue¹, D. Underwood¹, D. Wisnieff¹, C. Baks¹, D. Bethune³, J. Timmerwilke¹, B. R. Johnson¹, B. P. Gaucher¹, D. J. Friedman¹

¹IBM T. J. Watson Research Center, Yorktown Heights, NY

²IBM Systems, Rochester, MN; ³IBM Almaden Research Center, San Jose, CA

7:10 AM

22.2 A Cryo-CMOS Controller IC with Fully Integrated Frequency Generators for Superconducting Qubits

K. Kang^{}, D. Minn^{*}, S. Bae, J. Lee, S. Bae, G. Jung, S. Kang, M. Lee, H-J. Song, J-Y. Sim*

^{*}Equally-Credited Authors (ECAs), Pohang University of Science and Technology, Pohang, Korea

7:20 AM

22.3 A Cryogenic SiGe BiCMOS Hybrid Class B/C Mode-Switching VCO Achieving 201dBc/Hz Figure-of-Merit and 4.2GHz Frequency Tuning Range

Y. Peng^{1,2}, A. Ruffino¹, J. Benserhir¹, E. Charbon¹

¹Ecole Polytechnique Fédérale de Lausanne, Neuchâtel, Switzerland

²Southern University of Science and Technology, Shenzhen, China

7:30 AM

22.4 A WiFi and Bluetooth Backscattering Combo Chip Featuring Beam Steering via a Fully-Reflective Phased-Controlled Multi-Antenna Termination Technique Enabling Operation Over 56 Meters

S-K. Kuo, M. Dunna, D. Bharadia, P. P. Mercier, University of California, San Diego, CA

7:40 AM

22.5 A 108nW 0.8mm² Analog Voice Activity Detector (VAD) Featuring a Time-Domain CNN as a Programmable Feature Extractor and a Sparsity-Aware Computational Scheme in 28nm CMOS

F. Chen¹, K-F. Un¹, W-H. Yu¹, P-I. Mak¹, R. P. Martins^{1,2}

¹University of Macau, Macau, China

²University of Lisboa, Lisbon, Portugal

7:50 AM

22.6 A 23 μ W Solar-Powered Keyword-Spotting ASIC with Ring-Oscillator-Based Time-Domain Feature Extraction

K. Kim¹, C. Gao¹, R. Graça¹, I. Kiselev¹, H-J. Yoo², T. Delbruck¹, S-C. Liu¹

¹University of Zurich and ETH Zurich, Zurich, Switzerland

²KAIST, Daejeon, Korea

8:00 AM

22.7 An 82nW 0.53pJ/SOP Clock-Free Spiking Neural Network with 40 μ s Latency for AIoT Wake-Up Functions Using Ultimate-Event-Driven Bionic Architecture and Computing-in-Memory Technique

Y. Liu¹, Z. Wang^{1,2}, W. He¹, L. Shen¹, Y. Zhang¹, P. Chen¹, M. Wu¹, H. Zhang¹, P. Zhou³, J. Liu³, G. Sun¹, J. Ru¹, L. Ye^{1,2}, R. Huang¹

¹Peking University, Beijing, China

²Advanced Institute of Information Technology of Peking University, Hangzhou, China

³Nano Core Chip Electronic Technology, Hangzhou, China

Frequency Synthesizers

Session Chair: Jun Yin, *University of Macau, Taipa, Macau*

Session Co-Chair: Jeremy Dunworth, *Qualcomm Technologies, La Jolla, CA*

7:00 AM

23.1 A Cascaded PLL (LC-PLL + RO-PLL) with a Programmable Double Realignment Achieving 204fs Integrated Jitter (100kHz to 100MHz) and -72dB Reference Spur

T-H. Tsai¹, R-B. Sheen¹, S-Y. Hsu¹, Y-T. Chang¹, C-H. Chang¹, R. B. Staszewski²

¹TSMC, Hsinchu, Taiwan

²University College Dublin, Dublin, Ireland

7:10 AM

23.2 A 188fs_{rms}-Jitter and -243dB-FoM_{jitter} 5.2GHz-Ring-DCO-Based Fractional-N Digital PLL with a 1/8 DTC-Range-Reduction Technique Using a Quadruple-Timing-Margin Phase Selector

C. Hwang^{}, H. Park^{*}, T. Seong, J. Choi*

^{*}Equally-Credited Authors (ECAs), KAIST, Daejeon, Korea

7:20 AM

23.3 A 2.6-to-4.1GHz Fractional-N Digital PLL Based on a Time-Mode Arithmetic Unit Achieving -249.4dB FoM and -59dBc Fractional Spurs

Z. Gao¹, J. He¹, M. Fritz², J. Gong¹, Y. Shen¹, Z. Zong¹, P. Chen³, G. Spalink², B. Eitel², K. Yamamoto⁴,

R. B. Staszewski^{1,3}, M. S. Alavi¹, M. Babaie¹

¹Delft University of Technology, Delft, The Netherlands

²Sony Europe, Stuttgart, Germany

³University College Dublin, Dublin, Ireland

⁴Sony Semiconductor Solutions, Atsugi, Japan

7:30 AM

23.4 A 100MHz-Reference, 8GHz/16GHz, 177fs_{rms}/223fs_{rms} RO-Based IL-ADPLL Incorporating Reference Octupler with Probability-Based Fast Phase-Error Calibration

H. Kim¹, H-S. Oh², W. Jung¹, Y. Song¹, J. Oh³, D-K. Jeong¹

¹Seoul National University, Seoul, Korea

²University of California, Berkeley, CA

³Columbia University, New York, NY

7:40 AM

23.5 A Sub-100MHz Reference-Driven 25-to-28GHz Fractional-N PLL with -250dB FoM

D. Yang¹, D. Murphy¹, H. Darabi¹, A. Behzad¹, A. Abidi², S. Au¹, S. Mundlapudi¹, K. Shi¹, W. Leng²

¹Broadcom, San Jose, CA

²University of California, Los Angeles, CA

7:50 AM

23.6 A 68.6fs_{rms}-Total-Integrated-Jitter and 1.56μs-Locking-Time Fractional-N Bang-Bang PLL Based on Type-II Gear Shifting and Adaptive Frequency Switching

*S. M. Dartizio^{*1}, F. Buccoleri^{*1}, F. Tesolin¹, L. Avallone², A. Santiccioli¹, A. Iesurum³, G. Steffan²,*

D. Cherniak², L. Bertulesi¹, A. Bevilacqua³, C. Samori¹, A. L. Lacaita¹, S. Levantino¹

^{*}Equally-Credited Authors (ECAs)

¹Politecnico di Milano, Milan, Italy; ²Infineon Technologies, Villach, Austria

³University of Padova, Padova, Italy

8:00 AM

23.7 A 25.8GHz Integer-N PLL with Time-Amplifying Phase-Frequency Detector Achieving 60fs_{rms} Jitter, -252.8dB FoM_J, and Robust Lock Acquisition Performance

X. Geng, Y. Tian, Y. Xiao, Z. Ye, Q. Xie, Z. Wang

University of Electronic Science and Technology of China, Chengdu, China

Low-Power and UWB Radios for Communication and Ranging

Session Chair: *Maryam Tabesh, Google, Mountain View, CA*

Session Co-Chair:

Jan Prummel, Dialog Semiconductor B.V., A Renesas Company, 's-Hertogenbosch, The Netherlands

7:00 AM

24.1 A Long-Range Narrowband RF Localization System with a Crystal-Less Frequency-Hopping Receiver

C-W. Tseng¹, D. Komma¹, K-Y. Chen¹, R. Rothe¹, Z. Feng¹, M. Yasuda², M. Kawaminami³, H-S. Kim¹, D. Blaauw¹

¹University of Michigan, Ann Arbor, MI

²United Semiconductor Japan, Kuwana, Japan; ³United Semiconductor Japan, Yokohama, Japan

7:10 AM

24.2 A 1.66Gb/s and 5.8pJ/b Transcutaneous IR-UWB Telemetry System with Hybrid Impulse Modulation for Intracortical Brain-Computer Interfaces

M. Song¹, Y. Huang^{1,2}, Y. Shen¹, C. Shi^{1,3}, A. Breeschoten¹, M. Konijnenburg¹, H. Visser¹, J. Romme¹, B. Dutta⁴, M. S. Alavi², C. Bachmann¹, Y-H. Liu¹

¹imec-Netherlands, Eindhoven, The Netherlands

²Delft University of Technology, Delft, The Netherlands

³Eindhoven University of Technology, Eindhoven, The Netherlands; ⁴imec, Leuven, Belgium

7:20 AM

24.3 A 6.5-to-10GHz IEEE 802.15.4/4z-Compliant 1T3R UWB Transceiver

R. Chen, Y. Xiao, Y. Chen, H. Xu, P. Yu, Q. Peng, X. Li, X. Guo, J. Huang, N. Li, X. Hu, R. Ou, W. Liu, B. Chen, W. Zhang, X. Xin, B. Zhao, Z. Chen

Newradio Technology, Shenzhen, China

7:30 AM

24.4 A 22nm 0.84mm² BLE Transceiver with Self IQ-Phase Correction Achieving 39dB Image Rejection and On-Chip Antenna Impedance Tuning

K. Shibata, H. Matsui, H. Asano, Y. Kusaka, K. Ueda, N. Matsuno, H. Sato

Renesas Electronics, Tokyo, Japan

7:40 AM

24.5 A 266 μ W Bluetooth Low-Energy (BLE) Receiver Featuring an N-Path Passive Balun-LNA and a Pipeline Down-Mixing BB-Extraction Scheme Achieving 77dB SFDR and -3dBm OOB-B_{-1dB}

H. Shao¹, P-I. Mak¹, G. Qi², R. P. Martins^{1,3}

¹University of Macau, Macau, China

²Sun Yat-Sen University, Zhuhai, China

³University of Lisboa, Lisbon, Portugal

7:50 AM

24.6 A 110 μ W 2.5kb/s -103dBm-Sensitivity Dual-Chirp Modulated ULP Receiver Achieving -41dB SIR

M. Moosavifar, J. Im*, T. Odelberg, D. Wentzloff*

*Equally-Credited Authors (ECAs)

University of Michigan, Ann Arbor, MI

8:00 AM

24.7 An LPWAN Radio with a Reconfigurable Data/Duty-Cycled-Wake-Up Receiver

K-M. Kim¹, K-S. Choi¹, H. Jung^{1,2}, B. Yun¹, S. Kim², W. Oh², E-S. Lee³, S. Park², E-R. Jeong³, J. Ko², S-G. Lee¹

¹KAIST, Daejeon, Korea; ²PHYCHIPS, Daejeon, Korea

³Hanbat National University, Daejeon, Korea

Noise-Shaping ADCs

Session Chair: *Dominique Morche*, CEA-LETI, Grenoble, FranceSession Co-Chair: *Yan Zhu*, University of Macau, Taipa, Macau

7:00 AM

25.1 A 4.4 μ W 2.5kHz-BW 92.1dB-SNDR 3rd-Order VCO-Based ADC with Pseudo Virtual Ground Feedforward Linearization*C. Pochet, D. Hall*

University of California, San Diego, CA

7:10 AM

25.2 A 2.87 μ W 1kHz-BW 94.0dB-SNDR 2-0 MASH ADC using FIA with Dynamic-Body-Biasing Assisted CLS Technique*Y. Hu¹, Y. Zhao¹, W. Qu¹, L. Ye², M. Zhao¹, Z. Tan¹*¹Zhejiang University, Hangzhou, China²Peking University, Beijing, China

7:20 AM

25.3 A 0.0375mm² 203.5 μ W 108.8dB DR DT Single-Loop DSM Audio ADC Using a Single-Ended Ring-Amplifier-Based Integrator in 180nm CMOS*C. Y. Lee, U-K. Moon*

Oregon State University, Corvallis, OR

7:30 AM

25.4 A 5GS/s 360MHz-BW 68dB-DR Continuous-Time 1-1-1 Filtering MASH $\Delta\Sigma$ ADC in 40nm CMOS*Q. Liu^{1,2}, L. Breems^{1,2}, C. Zhang^{1,2}, S. Bajoria^{1,2}, M. Bolatkale^{2,3}, R. Rutten², G. Radulov¹*¹Eindhoven University of Technology, Eindhoven, The Netherlands²NXP Semiconductors, Eindhoven, The Netherlands³Delft University of Technology, Delft, The Netherlands

7:40 AM

25.5 A 28nm 6GHz 2b Continuous-Time $\Delta\Sigma$ ADC with -101dBc THD and 120MHz Bandwidth Using Digital DAC Error Correction*M. Bolatkale¹, R. Rutten¹, H. Brekelmans¹, S. Bajoria¹, Y. Gao¹, B. Burdick², L. Breems¹*¹NXP Semiconductors, Eindhoven, The Netherlands²NXP Semiconductors, Hamburg, Germany

7:50 AM

DS1 25.6 An 84dB-SNDR Low-OSR 4th-Order Noise-Shaping SAR with an FIA-Assisted EF-CRFF Structure and Noise-Mitigated Push-Pull Buffer-in-Loop Technique*T. Wang, T. Xie, Z. Liu, S. Li*

Georgia Institute of Technology, Atlanta, GA

SE3: Semiconductor Supply Chain

- Organizers:** **Rahul M. Rao**, *IBM, Bangalore, India*
- Co-Organizers:** **Mijunh Noh**, *Samsung Electronics, Hwaseong-si, Korea*
Massimo Alioto, *National University of Singapore, Singapore*
Chia-Hsiang Yang, *National Taiwan University, Taipei, Taiwan*
- Moderator:** **Jimmy Goodrich**, *Semiconductor Industry Association, Washington, DC*

The Semiconductor supply chain is a highly specialized global complex system stretching from design houses to manufacturing fabs, to test and assembly units, and integration factories, which varies by the nature of the company, market and product. The pandemic of 2020, with component shortages, along with the geopolitical trade conflicts, and the threat of counterfeiting, have highlighted the challenges and need for a better orchestrated and diversified management chain. This panel will highlight the risks ahead, and ways to get ahead of these challenges through market awareness, transparency, open platforms, global supplier landscape, and academic research.

Panelists:

- Shawn Han**, *Samsung Foundry, Seoul, Korea*
Jung Yoon, *IBM, Poughkeepsie, NY*
Bindiya Vakil, *Resilinc, Milpitas, CA*
Michael Reiha, *Soitec Microelectronics, Singapore*
Fredrik Tillman, *Ericsson, Lund, Sweden*
Willy C. Shih, *Harvard Business School, Boston, MA*

SE4: The Bright and Dark Side of Artificial Intelligence (AI)

- Co-Organizers:** **Denis Daly**, *Apple, Cambridge, MA*
Sriram Vangal, *Intel, Hillsboro, OR*
Jae-sun Seo, *Arizona State University, Tempe, AZ*
- Moderator:** **Tinoosh Mohsenin**, *University of Maryland, Baltimore, MD*

What is the golden vision for futuristic AI platforms? What are compelling AI use-cases and where are the risks? For instance, AI holds a great deal of promise for cybersecurity and human-centric robots. However, these sectors also have some of the highest potential for fallout. The panel will discuss forward-looking policy developments and ethical, legal, and societal issues related to AI, including socio-economic challenges.

Panelists:

- Kailash Gopalakrishnan**, *IBM T. J. Watson Research Center, Yorktown Heights, NY*
Evgeni Gousev, *Qualcomm, San Diego, CA*
Nele Mentens, *KU Leuven, Leuven, Belgium, and Leiden University, Leiden, The Netherlands*
Robert Muchsel, *Analog Devices, Dallas, TX*
Lama Nachman, *Intel, Santa Clara, CA*
Hoi-Jun Yoo, *KAIST, Daejeon, Korea*

mm-Wave & Sub-6GHz Receivers and Transceivers for 5G RadiosSession Chair: Shahriar Shahramian, *Nokia – Bell Labs, New Providence, NJ*Session Co-Chair: Byung-Wook Min, *Yonsei University, Seoul, Korea*

7:00 AM

27.1 A 16-Channel, 28/39GHz Dual-Polarized 5G FR2 Phased-Array Transceiver IC with a Quad-Stream IF Transceiver Supporting Non-Contiguous Carrier Aggregation up to 1.6GHz BW*A. Verma¹, V. Bhagavatula¹, A. Singh¹, W. Wu¹, H. Nagarajan¹, P-K. Lau¹, X. Yu¹, O. Elsayed¹, A. Jain¹, A. Sarkar¹, F. Zhang¹, C-C. Kuo¹, P. McElwee¹, P-Y. Chiang¹, C. Guo¹, Z. Bai¹, T. Chang¹, A. Mann¹, A. Rydin¹, X. Zhao¹, J. Lee², D. Yoon², C-W. Yao¹, S. I. Lu¹, S. W. Son¹, T. B. Cho²*¹Samsung Semiconductor, San Jose, CA²Samsung Electronics, Hwaseong, Korea

7:10 AM

27.2 A Power-Efficient 24-to-71GHz CMOS Phased-Array Receiver Utilizing Harmonic-Selection Technique Supporting 36dB Inter-Band Blocker Rejection for 5G NR*J. Pang, Y. Zhang, Z. Li, M. Tang, Y. Liao, A. A. Fadila, A. Shirane, K. Okada*

Tokyo Institute of Technology, Tokyo, Japan

7:20 AM

DS2 27.3 A 24-to-30GHz 256-Element Dual-Polarized 5G Phased Array with Fast Beam-Switching Support for >30,000 Beams*B. Sadhu¹, A. Paidimarri¹, W. Lee¹, M. Yeck¹, C. Ozdag¹, Y. Tojo², J-O. Plouchart¹, X. Gu¹, Y. Uemichi², S. Chakraborty¹, Y. Yamaguchi², N. Guan², A. Valdes-Garcia¹*¹IBM T. J. Watson Research Center, Yorktown Heights, NY²Fujikura, Sakura, Japan

7:30 AM

27.4 A Hybrid Coupler-First 5GHz Noise-Cancelling Dual-Mode Receiver with +10dBm In-Band IIP3 in Current-Mode and 1.7dB NF in Voltage-Mode*K. Yang, C. C. Boon, Z. Liu, J. Piao, T. Guo, Y. Dong, C. Li, A. Zhou, Z. Yang, X. Wang, Y. Liu*

Nanyang Technological University, Singapore, Singapore

7:40 AM

27.5 A Single-Path Digital-IF Receiver Supporting Inter/Intra 5-CA with a Single Integer LO-PLL in 14nm CMOS FinFET*B. Sung, H-G. Seok, J. Kim, J. Lee, T. Jang, I. Jang, Y. Kim, A. Yu, J-H. Jang, J. Lee, J. Bae, E. Park, S. Lee, S. Lee, J. Kim, B. Kim, Y. Lim, S. Oh, J. Lee, B. Cho, I. Kang*

Samsung Electronics, Hwaseong, Korea

DRAM and InterfaceSession Chair: Bor-Doou Rong, *Etron, Hsinchu, Taiwan*Session Co-Chair: Hye-Ran Kim, *Samsung Electronics, Hwasung, Korea*

7:00 AM

28.1 A 192-Gb 12-High 896-GB/s HBM3 DRAM with a TSV Auto-Calibration Scheme and Machine-Learning-Based Layout Optimization

M.-J. Park, H. S. Cho, T.-S. Yun, S. Byeon, Y. J. Koo, S. Yoon, D. U. Lee, S. Choi, J. Park, J. Lee, K. Cho, J. Moon, B.-K. Yoon, Y.-J. Park, S.-M. Oh, C. K. Lee, T.-K. Kim, S.-H. Lee, H.-W. Kim, Y. Ju, S.-K. Lim, S. G. Baek, K. Y. Lee, S. H. Lee, W. S. We, S. Kim, Y. Choi, S.-H. Lee, S. M. Yang, G. Lee, I.-K. Kim, Y. Jeon, J.-H. Park, J. C. Yun, C. Park, S.-Y. Kim, S. Kim, D.-Y. Lee, S.-H. Oh, T. Hwang, J. Shin, Y. Lee, H. Kim, J. Lee, Y. Hur, S. Lee, J. Jang, J. Chun, J. Cho
SK hynix, Icheon, Korea

7:10 AM

28.2 A 16Gb 27Gb/s/pin T-coil based GDDR6 DRAM with Merged-MUX TX, Optimized WCK Operation, and Alternative-Data-Bus

D. Lee, H.-J. Kwon, D. Kwon, J. Baek, C. Cho, S. Kim, D. An, C. Chang, U. Lim, J. Im, W. Sung, H.-R. Kim, S.-Y. Park, H. Kim, H. Seol, J. Kim, J. Shin, K.-Y. Kang, Y.-H. Kim, S. Kim, W. Park, S.-J. Kim, C. Lee, S. Lee, T. Park, C. Oh, H. Ban, H. Ko, H. Song, T.-Y. Oh, S. Hwang, K. S. Oh, J. Choi, J. Lee
Samsung Electronics, Hwaseong, Korea

7:20 AM

28.3 A 16Gb 9.5Gb/s/pin LPDDR5X SDRAM with Low-Power Schemes Exploiting Dynamic Voltage-Frequency Scaling and Offset-Calibrated Readout Sense Amplifiers in a Fourth Generation 10nm DRAM Process

D.-H. Kim, B. Song, H.-A. Ahn, W. Ko, S. Do, S. Cho, K. Kim, S.-H. Oh, H.-Y. Joo, G. Park, J.-H. Jang, Y.-H. Kim, D. Lee, J. Jung, Y. Kwon, Y. Kim, J. Jung, S. O, S. Lee, J. Lim, J. Son, J. Min, H. Do, J. Yoon, I. Hwang, J. Park, H. Shim, S. Yoon, D. Choi, J. Lee, S. Woo, E. Hong, J. Choi, J.-S. Kim, S. Han, J. Bang, B. Park, J. Kim, S.-K. Choi, G.-H. Han, Y.-C. Sung, W.-I. Bae, J.-D. Lim, S. Lee, C. Yoo, S. J. Hwang, J. Lee
Samsung Electronics, Hwaseong, Korea

7:30 AM

28.4 A 20 Gb/s/pin 1.18pJ/b 1149 μ m² Single-Ended Inverter-based 4-tap Addition-Only Feed-Forward Equalization Transmitter with Improved Robustness to Coefficient Errors in 28nm CMOS

C. Moon, J. Seo, M. Lee, I. Jang, B. Kim, Pohang University of Science and Technology, Pohang, Korea

7:40 AM

28.5 A 0.385-pJ/bit 10-Gb/s TIA-Terminated Di-Code Transceiver with Edge-Delayed Equalization, ECC, and Mismatch Calibration for HBM Interfaces

H. Park¹, Y. Choi¹, J. Sim¹, J. Choi¹, Y. Kwon¹, J. Song², C. Kim¹

¹Korea University, Seoul, Korea; ²Incheon National University, Incheon, Korea

7:50 AM

28.6 A 78.8-fJ/b/mm 12.0-Gb/s/Wire Capacitively Driven On-Chip Link Over 5.6mm with an FFE-Combined Ground-Forcing Biasing Technique for DRAM Global Bus Line in 65nm CMOS

S. Lee, J. Yun, S. Kim, Seoul National University, Seoul, Korea

8:00 AM

28.7 A 20-Gb/s/pin 0.0024-mm² Single-Ended DECS TRX with CDR-less Self-Slicing/Auto-Deserialization to Improve Tolerance on Duty Cycle Error and RX Supply Noise for DCC/CDR-less Short-Reach Memory Interfaces

J. Seo¹, S. Lee², M. Lee¹, C. Moon¹, B. Kim¹

¹Pohang University of Science and Technology, Pohang, Korea

²Samsung Electronics, Hwaseong, Korea

8:10 AM

28.8 A Supply-Noise-Induced Jitter-Cancelling Clock Distribution Network for LPDDR5 Mobile DRAM featuring a 2nd-order Adaptive Filter

*Y. Jung^{*1}, S. Lee^{*2}, H. Kim³, S. Cho⁴*, *Equally-Credited Authors (ECAs)

¹Samsung Electronics, Hwaseong-si, Korea; ²SK hynix, Icheon, Korea

³Korea Aerospace Research Institute, Daejeon, Korea; ⁴KAIST, Daejeon, Korea

ML Chips for Emerging ApplicationsSession Chair: Jun Deguchi, *Kioxia, Kawasaki, Japan*Session Co-Chair: Jae-sun Seo, *Arizona State University, Tempe, AZ*

8:30 AM

29.1 184QPS/W 64Mb/mm² 3D Logic-to-DRAM Hybrid Bonding with Process-Near-Memory Engine for Recommendation System*D. Niu¹, S. Li¹, Y. Wang¹, W. Han¹, Z. Zhang², Y. Guan², T. Guan³, F. Sun¹, F. Xue¹, L. Duan¹, Y. Fang¹, H. Zheng¹, X. Jiang⁴, S. Wang⁴, F. Zuo⁴, Y. Wang⁴, B. Yu⁴, Q. Ren⁴, Y. Xie¹*¹Alibaba DAMO Academy, Sunnyvale, CA²Alibaba DAMO Academy, Beijing, China³Alibaba DAMO Academy, Shanghai, China⁴UnilC, Xian, China

8:40 AM

29.2 A 28nm 27.5TOPS/W Approximate-Computing-Based Transformer Processor with Asymptotic Sparsity Speculating and Out-of-Order Computing*Y. Wang¹, Y. Qin¹, D. Deng¹, J. Wei¹, Y. Zhou¹, Y. Fan¹, T. Chen², H. Sun¹, L. Liu¹, S. Wei¹, S. Yin¹*¹Tsinghua University, Beijing, China²Tsing Micro, Beijing, China

8:50 AM

29.3 A 28nm 15.59 μ J/Token Full-Digital Bitline-Transpose CIM-Based Sparse Transformer Accelerator with Pipeline/Parallel Reconfigurable Modes*F. Tu^{1,2}, Z. Wu¹, Y. Wang¹, L. Liang², L. Liu², Y. Ding², L. Liu¹, S. Wei¹, Y. Xie², S. Yin¹*¹Tsinghua University, Beijing, China²University of California, Santa Barbara, CA

9:00 AM

29.4 ReckOn: A 28nm Sub-mm² Task-Agnostic Spiking Recurrent Neural Network Processor Enabling On-Chip Learning over Second-Long Timescales*C. Frenkel, G. Indiveri*

University of Zurich and ETH Zurich, Zurich, Switzerland

Power Management TechniquesSession Chair: Min Chen, *Analog Devices, Santa Clara, CA*Session Co-Chair: Li Geng, *Xi'an Jiaotong University, Xi'an, China*

8:30 AM

30.1 A 32nA Fully Autonomous Multi-Input Single-Inductor Multi-Output Energy Harvesting and Power Management Platform with 1.2×10^5 Dynamic Range, Integrated MPPT, and Multi-Modal Cold Start-Up*S. Li, X. Liu, B. H. Calhoun*

University of Virginia, Charlottesville, VA

8:40 AM

30.2 A 130V Triboelectric Energy-Harvesting Interface in 180nm BCD with Scalable Multi-Chip-Stacked Bias-Flip and Daisy-Chained Synchronous Signaling Technique*J. Lee, S-H. Lee, G-G. Kang, J-H. Kim, G-H. Cho, H-S. Kim*

KAIST, Daejeon, Korea

8:50 AM

30.3 A Reconfigurable Series-Parallel Charger for Dual-Battery Applications with 89W 97.7% Efficiency in Direct Charging Mode*S. Lee, T. Jeong, Y. Cho, J. Yoo, S. Cho, M. Kwon, D. Cho, S. H. Kang, J. W. Heo, H-S. Oh, S. U. Kwak*

Samsung Electronics, Hwaseong, Korea

9:00 AM

30.4 A 0.76V V_{in} Triode Region 4A Analog LDO with Distributed Gain Enhancement and Dynamic Load-Current Tracking in Intel 4 CMOS Featuring Active Feedforward Ripple Shaping and On-Chip Power Noise Analyzer*X. Liu, H. Krishnamurthy, R. Liu, K. Ravichandran, Z. Ahmed, N. Desai, N. Butzen, J. Tschanz, V. De*

Intel, Portland, OR

Audio Amplifiers

Session Chair: Qinwen Fan, *Delft University of Technology, Delft, The Netherlands*

Session Co-Chair: Mahdi Kashmiri, *Broadcom, San Jose, CA*

8:30 AM

31.1 A -117dBc THD (-132dBc HD3) and 126dB DR Audio Decoder with Code-Change-Insensitive RT-DEM Algorithm and Circuit Technique for Relaxing Velocity Saturation Effect of Poly Resistors

S-H. Wen, C-H. Hsiao, S-H. Chien, Y-C. Chen, K-H. Chen, K-D. Chen

MediaTek, Hsinchu, Taiwan

8:40 AM

31.2 A 121.4dB DR, -109.8dB THD+N Capacitively-Coupled Chopper Class-D Audio Amplifier

H. Zhang¹, M. Berkhout², K. A. A. Makinwa¹, Q. Fan¹

¹*Delft University of Technology, Delft, The Netherlands*

²*Goodix Technology, Nijmegen, The Netherlands*

8:50 AM

31.3 A 121dB DR, 0.0017% THD+N, 8× Jitter-Effect Reduction Digital-Input Class-D Audio Amplifier with Supply-Voltage-Scaling Volume Control and Series-Connected DSM

W-H. Sun, S-H. Chien, T-H. Kuo

National Cheng Kung University, Tainan, Taiwan

9:00 AM

31.4 A -91dB THD+N Resistor-Less Class-D Piezoelectric Speaker Driver Using a Dual Voltage/ Current Feedback for LC Resonance Damping

S. Karmakar¹, M. Berkhout², K. A. A. Makinwa¹, Q. Fan¹

¹*Delft University of Technology, Delft, The Netherlands*

²*Goodix Technology, Nijmegen, The Netherlands*

Ultrasound and Beamforming Applications

Session Chair: Jun-Chau Chien, National Taiwan University, Taipei, Taiwan

Session Co-Chair: Jerald Yoo, National University of Singapore, Singapore, Singapore

8:30 AM

32.1 **BatDrone: A 9.83M-focal-points/s 7.76 μ s-Latency Ultrasound Imaging System with On-Chip Per-Voxel RX Beamfocusing for 7m-Range Drone Applications**

DS1

*L. Wu^{*1}, J. Guo^{*1}, R. Jiang¹, Y. Peng², H. Wu¹, J. Li¹, Y. Dong¹, M. Zhang¹, Z. Li¹, K. A. Ng³, C-W. Tsai¹, L. Zhang¹, L. Lin⁴, L. Lin², J. Yoo^{1,5}*

^{*}Equally-Credited Authors (ECAs)

¹National University of Singapore, Singapore, Singapore

²University of California, Berkeley, CA

³Digipen Institute of Technology, Singapore, Singapore

⁴Southern University of Science and Technology, Shenzhen, China

⁵The N.1 Institute for Health, Singapore, Singapore

8:40 AM

32.2 **A Pitch-Matched ASIC with Integrated 65V TX and Shared Hybrid Beamforming ADC for Catheter-Based High-Frame-Rate 3D Ultrasound Probes**

Y. Hopf¹, B. Ossenkopp¹, M. Soozande², E. Noothout¹, Z-Y. Chang¹, C. Chen¹, H. Vos^{1,2}, H. Bosch², M. Verweij^{1,2}, N. de Jong^{1,2}, M. Pertijs¹

¹Delft University of Technology, Delft, The Netherlands

²Erasmus MC, Rotterdam, The Netherlands

8:50 AM

32.3 **A 1.2mW/channel 100 μ m-Pitch-Matched Transceiver ASIC with Boxcar-Integration-Based RX Micro-Beamformer for High-Resolution 3D Ultrasound Imaging**

P. Guo¹, F. Fool¹, E. Noothout¹, Z-Y. Chang¹, H. J. Vos^{1,2}, J. G. Bosch², M. D. Verweij^{1,2}, N. de Jong^{1,2}, M. A. P. Pertijs¹

¹Delft University of Technology, Delft, The Netherlands

²Erasmus MC, Rotterdam, The Netherlands

9:00 AM

32.4 **An Electronically Tunable Multi-Frequency Air-Coupled CMUT Receiver Array with sub-100 μ Pa Minimum Detectable Pressure Achieving a 28kb/s Wireless Uplink Across a Water-Air Interface**

A. Singhvi, A. Fitzpatrick, A. Arbabian

Stanford University, Stanford, CA

9:10 AM

32.5 **A Multimode 157 μ W 4-Channel 80dB_A-SNDR Speech-Recognition Frontend with Self-DOA Correction Adaptive Beamformer**

*T. Kang^{*1}, S. Lee^{*1}, S. Song¹, M. R. Haghgha², M. P. Flynn¹*

^{*}Equally-Credited Authors (ECAs)

¹University of Michigan, Ann Arbor, MI

²Intel, Santa Clara, CA

Domain-Specific ProcessorsSession Chair: **Sanu Mathew**, *Intel, Portland, OR*Session Co-Chair: **Chia-Hsiang Yang**, *National Taiwan University, Taipei, Taiwan*

8:30 AM

DS2 33.1 A 1.05A/m Minimum Magnetic Field Strength Single-Chip Fully Integrated Biometric Smart Card SoC Achieving 1014.7ms Transaction Time with Anti-Spoofing Fingerprint Authentication*J-S. Chang, E. Jang, Y. Choi, M. Song, S. Lee, G-J. Kang, J. Kim, S-W. Kang, U. Song, C-Y. Cho, J. Lee, K. Seo, S. Song, S. U. Kwak*

Samsung Electronics, Hwaseong, Korea

8:40 AM

33.2 A 96.2nJ/class Neural Signal Processor with Adaptable Intelligence for Seizure Prediction*Y-Y. Hsieh, Y-C. Lin, C-H. Yang*

National Taiwan University, Taipei, Taiwan

8:50 AM

DS2 33.3 A HD 31fps 7×7-View Light-Field Factorization Processor for Dual-Layer 3D Factored Display*L-Q. Weng, L-D. Chen, H-C. Cheng, A-Y. Zheng, K-P. Lin, C-T. Huang*

National Tsing Hua University, Hsinchu, Taiwan

9:00 AM

DS2 33.4 DSPU: A 281.6mW Real-Time Depth Signal Processing Unit for Deep Learning-Based Dense RGB-D Data Acquisition with Depth Fusion and 3D Bounding Box Extraction in Mobile Platforms*D. Im, G. Park, Z. Li, J. Ryu, S. Kang, D. Han, J. Lee, H-J. Yoo*

KAIST, Daejeon, Korea

Hardware Security

Session Chair: Chiraag Juvekar, Analog Devices, Boston, MA

Session Co-Chair: Ingrid Verbauwhede, KU Leuven, Leuven, Belgium

8:30 AM

34.1 A 28nm 48KOPS 3.4 μ J/Op Agile Crypto-Processor for Post-Quantum Cryptography on Multi-Mathematical Problems

Y. Zhu¹, W. Zhu¹, M. Zhu², C. Li¹, C. Deng¹, C. Chen¹, S. Yin¹, S. Yin¹, S. Wei¹, L. Liu¹

¹Tsinghua University, Beijing, China

²Micro Innovation Integrated Circuit Design, Wuxi, China

8:40 AM

34.2 Side-Channel Attack Counteraction via Machine Learning-Targeted Power Compensation for Post-Silicon HW Security Patching

Q. Fang^{*1}, L. Lin^{*1,2}, Y. Z. Wong¹, H. Zhang¹, M. Alioto¹

*Equally-Credited Authors (ECAs)

¹National University of Singapore, Singapore, Singapore

²Southern University of Science and Technology, Shenzhen, China

8:50 AM

34.3 **DS2** A Threshold-Implementation-Based Neural-Network Accelerator Securing Model Parameters and Inputs Against Power Side-Channel Attacks

S. Maji¹, U. Banerjee², S. H. Fuller^{1,3}, A. P. Chandrakasan¹

¹Massachusetts Institute of Technology, Cambridge, MA

²Indian Institute of Science, Bengaluru, India

³Analog Devices, Wilmington, MA

9:00 AM

34.4 An 8.3-to-18Gbps Reconfigurable SCA-Resistant/Dual-Core/Blind-Bulk AES Engine in Intel 4 CMOS

R. Kumar, V. B. Suresh, M. A. Anders, S. K. Hsu, A. Agarwal, V. K. De, S. K. Mathew
Intel, Hillsboro, OR

F1: Compute-in-X (CiX): Overcoming the Data Bottleneck in AI Processing

- Organizer:** *Kyu-Hyoun (KH) Kim, IBM T. J. Watson, Yorktown Heights, NY*
- Committee:** *Geoffrey W. Burr, IBM Research, San Jose, CA*
Jun Deguchi, Kioxia, Kawasaki, Japan
Eric Wang, TSMC, Hsinchu, Taiwan
Chih-Cheng Hsieh, National Tsing Hua University, Hsinchu, Taiwan
- Champions:** *Yan Li, Western Digital, Milpitas, CA*
Fatih Hamzaoglu, Intel, Hillsboro, OR

As AI network- and dataset-sizes keep growing, the flow of data – from various tiers of the memory hierarchy to the compute-engines, and back – becomes critically important. In the worst-case, this data-flow can start to constrain further improvements in both system-performance and the energy-efficiency of future AI processing systems.

The idea of processing data at the spot where it is stored or generated, instead of moving it back and forth, has led to a broad variety of promising compute-in- x system concepts; where, x can be a memory array, a memory die, a memory package, the storage, a sensor, the network, etc.

This forum will highlight the state-of-the-art for several such compute-in- x system concepts, as well as related in-the-near-future challenges and opportunities for the SSCS community.

Agenda

<u>Time</u>	<u>Topic</u>
7:00 AM	Introduction <i>Kyu-Hyoun (KH) Kim, IBM T. J. Watson, Yorktown Heights, NY</i>
7:15 AM	AI Memory Challenges and How to Solve Them For Data-Flow Accelerators <i>Swagath Venkataramani, IBM T. J. Watson, Yorktown Heights, NY</i>
7:30 AM	Nano-Systems for AI: N3XT 3D with Dense-Memory, Illusion-Scaleup, Co-Design <i>Subhasish Mitra, Stanford University, Stanford, CA</i>
7:45 AM	Computing In and Near Memory: Practical Challenges and Future Directions <i>Nam Sung Kim, University of Illinois, Urbana, IL</i>
8:00 AM	Future Prospects of Computing In or Near Flash Memories <i>Hang-Ting (Oliver) Lue, Macronix International, Hsinchu, Taiwan</i>
8:15 AM	We've Rethought Our Commute; Can We Rethink Our Data's Commute? <i>Frank Hady, Intel, Portland, OR</i>
8:30 AM	6G: Convergence of Communication, Computing, Control and Sensing <i>Mallik Tatipamula, Ericsson, Santa Clara, CA</i>
8:45 AM	Charge-Domain Signal Compression in Ultra-High-Speed CMOS Image Sensors <i>Keiichiro Kagawa, Shizuoka University, Hamamatsu, Japan</i>
9:00 AM	Neuromorphic Computing <i>Steve B. Furber, The University of Manchester, Manchester, United Kingdom</i>

F2: Chip Design for Low-Power, Robust, and Secure IoT Devices

- Organizer:** *Patrick Mercier, University of California, San Diego, CA*
- Committee:** *Rabia Tugce Yazicigil, Boston University, Boston, MA*
Jan Prummel, Dialog Semiconductor B.V., A Renesas Company,
's-Hertogenbosch, The Netherlands
Luca Benini, ETHZ and UNIBO, Zurich, Switzerland
Gael Pillonnet, CEA-Léti, Grenoble, France
Hidehiro Shiga, KIOXIA, Yokohama, Japan
- Champions:** *Yun-Shiang Shu, MediaTek, Taipei, Taiwan*
Andreia Cathelin, STMicroelectronics, Crolles, France
Bruce Rae, STMicroelectronics, Edinburgh, United Kingdom

The Internet of Things is currently in the process of transitioning from concept to execution, and yet, many technical challenges remain. In particular, emerging IoT devices require increasingly small form factors and therefore must consume very low power, all while operating in congested wireless environments with security designed-in from the ground up. Emerging devices also require built-in machine-learning capabilities in tiny footprints while consuming low power.

This forum covers topics ranging from how to build energy-efficient yet long-range and robust IoT-centric wireless links, how to build low-power sensor interfaces, how to design physically and cryptographically-secure protocols, how to integrate signal processing and machine learning into small nodes, and how to perform efficient yet compact power management/energy harvesting.

Agenda

<u>Time</u>	<u>Topic</u>
7:00 AM	Introduction <i>Patrick Mercier, University of California, San Diego, CA</i>
7:15 AM	Connecting Massive IoT in the New Decade and Beyond <i>Tingfan Ji, Qualcomm, San Diego, CA</i>
7:30 AM	Sensor Interface, Analog, and Mixed-Signal Circuits for Miniaturized IoT Devices <i>Taekwang Jang, ETH Zurich, Zurich, Switzerland</i>
7:45 AM	Wide-Range Wireless Communication Circuits for NB-IoT and eMTC <i>Kim B. Östman, Nordic Semiconductor, Turku, Finland</i>
8:00 AM	Low-Power Wireless Communication Technologies for Emerging Short-Range Internet-of-Things <i>Po-Han Peter Wang, Broadcom, San Diego, CA</i>
8:15 AM	Manufacturing Semiconductors is Complex. How About Manufacturing Secure Semiconductors? <i>Miroslav Knezevic, NXP, Austin, TX</i>
8:30 AM	Memory System Design to Innovate Edge Computing for IoT Devices <i>Takashi Ito, Renesas Electronics, Tokyo, Japan</i>
8:45 AM	Energy-Constrained Tiny-ML for IoT Applications <i>Tony Tae-Hyoung Kim, Nanyang Technological University, Singapore, Singapore</i>
9:00 AM	Extending Battery Life Through Lower I_0 without Compromising System Performance or Solution Size <i>Keith Kunz, Texas Instruments, Tucson, AZ</i>

F3: The Path to 6G: Architectures, Circuits, Technologies for Sub-THz Communications, Sensing, and Imaging

- Organizer:** *Giuseppe Gramegna, IMEC, Leuven, Belgium*
- Committee:** *Shuhei Amakawa, Hiroshima University, Higashihiroshima, Japan*
Matteo Bassi, Infineon Technologies, Villach, Austria
Patrick Reynaert, KU Leuven, Leuven, Belgium
Swaminathan Sankaran, Texas Instruments, Dallas, TX
Ho-Jin Song, Pohang University of Science and Technology, Pohang, Korea
- Champions:** *Andreia Cathelin, STMicroelectronics, Crolles, France*
Kostas Doris, NXP, Eindhoven, The Netherlands
Chih-Ming Hung, MediaTek, Taipei, Taiwan

The demand for faster communications and wider coverage keeps fueling research towards 6G that will leverage higher frequencies within a broader application spectrum. This is stimulating rapid transformations and innovations in several fields, such as communication, sensing, and imaging. A wide range of new architectures, circuits and technologies are under investigation to support this trend. In this forum, experts will illuminate the way to the future of Sub-THz design and applications by transversally focusing on circuits, architectures, and also technology, packaging, and testing solutions.

Agenda

<u>Time</u>	<u>Topic</u>
7:00 AM	Introduction <i>Giuseppe Gramegna, IMEC, Leuven, Belgium</i>
7:15 AM	6G Communications: Vision and Challenges <i>Gary Xu, Samsung, Plano, TX</i>
7:30 AM	Emerging Device and Heterogenous Integration Technologies for sub-THz Applications <i>Nadine Collaert, IMEC, Leuven, Belgium</i>
7:45 AM	Highly Integrated D-Band Phased Arrays for 6G Wireless Communications <i>Mohamed Elkhoully, Bell Laboratories, New Providence, NJ</i>
8:00 AM	Sub-Terahertz Transceivers in Silicon <i>Minoru Fujishima, Hiroshima University, Higashi-Hiroshima, Japan</i>
8:15 AM	ICs and Transceiver Module Design for 100-300GHz Wireless <i>Mark J. W. Rodwell, University of California, Santa Barbara, CA</i>
8:30 AM	Sub-THz InP-Based Wireless Connection Techniques Toward 6G <i>Hiroshi Hamada, NTT DoCoMo, Yokosuka, Japan</i>
8:45 AM	Measurement and Validation of Sub-THz Radios: What Will it Take? <i>Roger Nichols, Keysight Technologies, Santa Rosa, CA</i>
	WITHDRAWN: Concepts, Architectures and Circuits for Sub-THz Sensing and Imaging

SE5: Shifting Tides of Innovation – Where is Cutting-Edge Research Happening Today?

Organizers: **Alicia Klinefelter**, *NVIDIA, Durham, NC*
Mingoo Seok, *Columbia University, New York, NY*

Co-Organizers: **Sophia Shao**, *University of California, Berkeley, CA*
Chiraag Juvekar, *Analog Devices, Cambridge, MA*

Moderator: **Alicia Klinefelter**, *NVIDIA, Durham, NC*

As research becomes more complex, multidisciplinary and system oriented, the focal point of innovation has begun to shift. Resource constraints such as people per project or the cost of working in the latest technology node also impacts who can participate in cutting-edge research. Industry does not have strong incentives to publish their most innovative and competitive work, leaving many in the dark as to what the state of the art is within companies. Even within industry, innovation can come from research, product, or startups. On the academic side, funding bodies and trends can also impact the innovation process. How can we close this gap and who really has the edge? Is industry-guided academic research the way to get the best of both worlds? The traditional debate has been between academia and industry, but there are many more facets to the discussion. This panel explores a variety of perspectives of how innovation occurs across the industry.

Panelists:

James Myers, *Arm, Cambridge, United Kingdom*

Tezaswi Raja, *NVIDIA, Santa Clara, CA*

Nam Sung Kim, *University of Illinois, Urbana-Champaign, IL*

Scott Hanson, *Ambiq, Austin, TX*

Christal Gordon, *Booz Allen Hamilton, McLean, VA*

Thomas Parry, *SystematIC Design, Rotterdam, The Netherlands*

SE6: Next Trillion-Dollar Market

Co-Organizers: **Jane Gu**, *University of California, Davis, Davis, CA*
Wei-Zen Chen, *National Yang Ming Chiao Tung University, Hsin-Chu, Taiwan*
Kazuko Nishimura, *Panasonic, Moriguchi, Japan*
Patrick Mercier, *University of California, San Diego, La Jolla, CA*

Moderator: **Tom Lee**, *Stanford University, Stanford, CA*

Innovations and technologies, which impact humanity in many aspects, enable rapidly evolving and emerging applications: including 5G and beyond wireless communications, wireline communications, autonomous vehicle, sensing, artificial intelligence (AI), machine learning, internet of things (IoT), internet of everything (IoE), virtual reality (VR), augmented reality (AR), silicon photonics, quantum computing, etc. Which of these will be the next trillion-dollar market driver for chips?

A collection of distinguished experts, from various domains, had been assembled to discuss the challenges and opportunities for growth in multiple, potentially large, sectors; the enabling technologies in each sector; and the ones required, particularly, from the semiconductor industry, as well as their timelines and questions raised by **you**, the audience.

Panelists:

Lawrence Loh, *Mediatek, Hsinchu City, Taiwan*

Vladimir Stojanovic, *University of California, Berkeley, Berkeley, CA*

Hayato Wakabayashi, *Sony Semiconductor Solutions, Atsugi, Japan*

Nancy Shemwell, *Trilogy Networks, Dallas, TX*

Bill Dally, *NVIDIA, Incline Village, NV*

Jay Gambetta, *IBM Quantum, Yorktown Heights, NY*

F4: Paving the Way to 200Gb/s Transceivers

Organizers: *Patrick Yue*, Hong Kong University of Science and Technology, Clear Water Bay, Hong Kong
Sudip Shekhar, University of British Columbia, Vancouver, Canada

Committee: *Thomas Toifl*, Cisco Systems, Thalwil, Switzerland
Bo Zhang, Broadcom, Irvine, CA
Munehiko Nagatani, NTT, Kanagawa, Japan
Milin Zhang, Tsinghua University, Beijing, China

Champions: *Franz Dielacher*, Infineon Technologies, Villach, Austria
Bill Redman-White, HiLight Semiconductor, Southampton, United Kingdom

This Forum aims to provide a comprehensive background for the upcoming 200Gb/s electrical and optical links. Seven industry and academic experts will address the state of the art and offer insightful projections on related topics, including standards, circuits and technology. The Forum will begin with the design considerations for different standardizations of end-to-end channels at 224Gb/s. Next, the challenges and opportunities of serial transceiver design, signaling schemes beyond PAM4, equalization, DSP, and advanced forward-error-correction techniques will be presented. Switching gears to the technology side of things, advancements in silicon photonic technologies to support 200Gb/s operation will be discussed. A design example of a coherent optical transceiver will conclude the forum presentation.

Agenda

<u>Time</u>	<u>Topic</u>
7:00 AM	Introduction <i>Patrick Yue</i> , Hong Kong University of Science and Technology, Clear Water Bay, Hong Kong
7:15 AM	224 Gb/s Transceiver, End-to-End Channels, and Standardizations <i>Mike Li</i> , Intel, San Jose, CA
7:30 AM	200Gb/s Serial Transceiver Design: Challenges and Opportunities <i>Jonathan Rogers</i> , Alphawave IP, Toronto, Canada
7:45 AM	200Gb/s: Beyond PAM4 <i>Gain Kim</i> , DGIST, Daegu, Korea
8:00 AM	DSP-Based Transceivers for 200Gb/s: Challenges and the Path Forward <i>Tamer Ali</i> , Mediatek, Irvine, CA
8:15 AM	Advanced FEC for 200Gb/s Transceiver Applications <i>Xinyuan Wang</i> , Huawei Technologies, Beijing, China
	WITHDRAWN: Semiconductor Technology – the Path Forward for the Coming Decades
8:30 AM	Silicon Photonics Technology for Next-Generation Transceivers <i>Joris Van Campenhout</i> , IMEC, Leuven, Belgium
8:45 AM	Coherent Optical Transceivers for >200Gb/s per Wavelength <i>Alex Rylyakov</i> , Nokia, New York, NY

F5: How to Improve AI Efficiency Further: New Devices, Architectures and Algorithms

Organizers: *Rangharajan Venkatesan, NVIDIA, Santa Clara, CA*
Alicia Klinefelter, NVIDIA, Durham, NC

Committee: *Kea-Tiong Tang, National Tsing Hua University, Hsinchu, Taiwan*
Ru Huang, Peking University, Beijing, China
Mingoo Seok, Columbia University, New York, NY
Shidhartha Das, Arm, Cambridge, United Kingdom

Champions: *Yan Li, Western Digital, Milpitas, CA*
Fatih Hamzaoglu, Intel, Hillsboro, OR

Machine learning (ML) algorithms and applications continue to evolve at a rapid pace relative to Moore's Law. There is simultaneously a demand for bigger and more complex ML models, ever-growing computational throughput and improved energy efficiency over the coming decade. As we start to hit the limits of technology scaling, what are the latest design strategies to improve performance and energy efficiency of machine learning processors of the future? Further, can ML-based tools improve hardware design methodology? This forum aims to explore novel circuits, architectures, algorithms, as well as ML-based chip design tools that will push the limits of AI efficiency.

Agenda

<u>Time</u>	<u>Topic</u>
7:00 AM	Introduction <i>Rangharajan Venkatesan, NVIDIA, Santa Clara, CA</i>
7:15 AM	GPU Architectures for Efficient Deep Learning <i>Ronny Krashinsky, NVIDIA, Santa Clara, CA</i>
7:30 AM	Mixed-Signal Compute-in-Memory Processing for Energy Efficient Algorithms <i>Laura Fick, Mythic, Cedar Park, TX</i>
7:45 AM	Neuromorphic Intelligence: Using Populations of Inhomogeneous Spiking Neurons to Carry Out Robust Computation in Neuromorphic Processors <i>Giacomo Indiveri, University of Zurich and ETH Zurich, Zurich, Switzerland</i>
8:00 AM	Artificial Intelligence Processor Using Diffractive Photonic Computing <i>Xing Lin, Tsinghua University, Beijing, China</i>
8:15 AM	Quantization Techniques for Low-Precision Inference and Training <i>Kailash Gopalakrishnan, IBM Research, Yorktown Heights, NY</i>
8:30 PM	Graphs: Powerful But Hard to Beat <i>Stijn Eyerman, Intel, Kontich, Belgium</i>
8:45 PM	Acceleration for Graph Neural Network Inference <i>Sachin S. Sapatnekar, University of Minnesota, Minneapolis, MN</i>
9:00 PM	Machine Learning in Chip Design Tools <i>Evangeline Young, Chinese University of Hong Kong, Shatin, Hong Kong</i>

F6: Computer Systems Under Attack – Paying the Performance Price for Protection

Organizer: *Massimo Alioto, National University of Singapore, Singapore*

Committee: *Ingrid Verbauwhede, KU Leuven, ESAT-COSIC, Leuven, Belgium*
Sanu Mathew, Intel, Hillsboro, OR
Mingoo Seok, Columbia University, New York, NY
Dong Uk Lee, SK hynix, Icheon-si, Korea
Rabia Tugce Yazicigil, Boston University, Boston, MA

Champion: *Vivek De, Intel, Hillsboro, OR*

Present-day computer systems are increasingly under attack on multiple fronts with new vulnerabilities being discovered every day at system, architecture, memory and physical level. While countermeasures against such attacks exist, they often impose significant overheads in performance and power. This forum will give an overview of recent security vulnerabilities, including speculative side-channels, memory exploits, physical attacks and discuss the overheads of detecting/mitigating against them. The forum also includes post-quantum cryptographic algorithms and homomorphic encryption accelerators that promise very high security value propositions, while imposing orders-of-magnitude increase in computational complexity.

Agenda

<u>Time</u>	<u>Topic</u>
7:00 AM	Introduction <i>Massimo Alioto, National University of Singapore, Singapore</i>
7:15 AM	Overview of Security Challenges, Applications, Common Practice and Directions in SOC Design <i>Serge Leef, Darpa, Bellevue, WA</i>
7:30 AM	Microarchitectural Side-Channel Attacks <i>Todd Austin, University of Michigan, Ann Arbor, MI</i>
7:45 AM	Microarchitectural Vulnerabilities: Evolving Landscape <i>Carlos Rozas, Intel, Portland, OR</i>
8:00 AM	DRAM Circuit Design for Protecting Natural/Artificial Faults and Reliability Degradation <i>Dongkyun Kim, SK hynix, Icheon-si, Korea</i>
8:15 AM	Memory Architecture Mitigations and Impact on System-Level Performance <i>Ruby Lee, Princeton University, Princeton, NJ</i>
8:30 AM	Physical Side-Channel Attacks and Counteraction Through Design Automation <i>Ileana Buhan, Radboud University, Nijmegen, The Netherlands</i>
8:45 AM	Integrated Sense-and-React Countermeasures Against Physical Attacks <i>Noriyuki Miura, Osaka University, Osaka, Japan</i>
9:00 AM	Hardware Implementation Challenges in Post-Quantum Encryption and Fully Homomorphic Encryption <i>Sujoy Sinha Roy, Graz University of Technology, Graz, Austria</i>

Short Course:
High Speed/High Performance Data Converters:
Metrics, Architectures, and Emerging Topics

Q&A Time:	Topic:
7:00 AM	Introduction by Chair, Daniel Friedman <i>IBM Thomas J. Watson Research Center, Yorktown Heights, NY</i>
7:05 AM	Introduction to ADCs/DACs: Metrics, Topologies, Trade Space, and Applications Boris Murmann , <i>Stanford University, Stanford, CA</i>
7:35 AM	Ultra-High-Data-Rate ADCs and DACs: Architectures and Implementations Gabriele Manganaro , <i>MediaTek, Woburn, MA</i>
8:05 AM	High-Precision and Low-Power ADCs Pieter Harpe , <i>Eindhoven University of Technology, Eindhoven, The Netherlands</i>
8:35 AM	Emerging Data-Converter Concepts Nan Sun , <i>Tsinghua University, Beijing, China</i>

Introduction

Data converters provide the gateway between the analog and digital worlds. They play a critical role in a vast range of systems, and integrated converters represent a central and growing element in high performance designs in applications from wireline to wireless and more. In this course, we start with an introduction to data converters, discussing key topologies, metrics, and the associated trade space. We continue with a discussion of ultra-high data rate converter design approaches before moving to high precision and low power converter topics. In our final session, we discuss emerging data converter concepts that will shape the future of research in this area.

Live Q&A - February 26, 7:05 AM PST

SC1:

Introduction to ADCs/DACs: Metrics, Topologies, Trade Space, and Applications*Boris Murmann, Stanford University, Stanford, CA*

This presentation provides a short introduction to ADCs and DACs. The intent is to prepare the audience for the subsequent talks that will cover intricate details of modern, fine-tuned realizations. Topics include elementary data converter building blocks and their imperfections, converter topologies and their basic tradeoffs, performance metrics and figures of merit, as well as selected application aspects.

Boris Murmann is a Professor of Electrical Engineering at Stanford University. He joined Stanford in 2004 after completing his Ph.D. degree in electrical engineering at the University of California, Berkeley in 2003. From 1994 to 1997, he was with Neutron Microelectronics, Germany, where he developed low-power and smart-power ASICs in automotive CMOS technology. Since 2004, he has worked as a consultant with numerous Silicon Valley companies. Dr. Murmann's research interests are in mixed-signal integrated circuit design, with special emphasis on sensor interfaces, data converters and embedded machine learning. He has served the Data Converter Subcommittee Chair and Technical Program Chair of the IEEE International Solid-State Circuits Conference (ISSCC). He is a Fellow of the IEEE.

Live Q&A - February 26, 7:35 AM PST

SC2:

Ultra-High-Data-Rate ADCs and DACs: Architectures and Implementations*Gabriele Manganaro, MediaTek, Woburn, MA*

Ten years ago or so, the term high-speed data converter was synonymous with sample rates on the order of a few hundreds of MHz, barring rare exceptions. Today, medium resolution ADCs (10-to-12b) and DACs clocked at tens of GHz, and even faster 6-to-8b converters, have been demonstrated without melting the die. So how could this level of advancement happen in the face of the end of Dennard scaling? The answer lies with the combination of architecture innovation and digital assistance. This presentation will give an overview of this rapidly (no pun intended) developing topic, aiming to illustrate the key design principles, their practical applicability, and will complement this material with examples of recently published multi-GSPS data converters.

Gabriele Manganaro (Fellow IEEE) holds a Dr. Eng. (1994) and a Ph.D. degree (1997) in Electronics from the University of Catania, Italy. He has worked in analog IC design, primarily in high-speed data converters design, both in Europe and the USA for over twenty years. He's presently a Director of Technology at MediaTek in Woburn, Massachusetts. He has authored/co-authored more than 60 peer-reviewed papers, three books (notably "Advanced Data Converters", Cambridge University Press, 2011) and has been granted 18 US patents, with more pending.

Live Q&A - February 26, 8:05 AM PST

SC3:

High-Precision and Low-Power ADCs*Pieter Harpe, Eindhoven University of Technology, Eindhoven, The Netherlands*

ADC designs are progressing rapidly over time in terms of architectural developments and circuit innovations. In this talk, we will focus on high-precision designs and on low-power design techniques of ADC topologies such as pipelined ADCs, Delta-Sigma modulators, and SAR (successive-approximation) ADCs. Besides discussing general challenges and solutions, some state-of-the-art ADC examples will be explained in the context of the principles outlined in this lecture, and a short review from a system integration perspective will be given.

Pieter Harpe received M.Sc. and Ph.D. degrees from the Eindhoven University of Technology, The Netherlands. He spent several years as a researcher at imec, The Netherlands, and joined Eindhoven University of Technology in 2011, where he is currently Associate Professor on low-power mixed-signal circuits. Dr. Harpe is co-organizer of the yearly AACD workshop, an analog subcommittee chair for the ESSCIRC conference, and the SSCS CONFedu program chair. He served as an ISSCC ITPC member, SSCS Distinguished Lecturer, and JSSC guest editor. He is a Senior Member of the IEEE and a recipient of the ISSCC 2015 Distinguished Technical Paper Award.

Live Q&A - February 26, 8:35 AM PST

SC4:

Emerging Data-Converter Concepts*Nan Sun, Tsinghua University, Beijing, China*

This talk presents several novel data-converter architectures, including hybrid ADCs that combine traditional architectures (e.g., a noise-shaping SAR) and Nyquist-rate ADCs with continuous-time (CT) front ends (e.g., a CT-pipe and CT-SAR). It also includes scaling-friendly time-domain ADCs that use digital gates to process analog signals. This talk also covers circuit-level innovations, including the use of open-loop and closed-loop dynamic amplifiers for residue amplification, as well as noise cancellation techniques that break the kT/C noise limit.

Nan Sun is a Professor of Electronic Engineering at Tsinghua University. He was Assistant and then Associate Professor with the University of Texas at Austin. He received the B.Sc. degree from Tsinghua University and the PhD degree from Harvard University. He received the NSF Career Award in 2013 and the IEEE SSCS New Frontier Award in 2020. He has graduated 24 PhDs (9 of whom are professors) and published 200 papers, including 30+ JSSC and 40+ ISSCC/VLSI/CICC papers. He serves on the TPC of CICC and A-SSCC. He served as an Associate Editor for IEEE TCAS-I and for JSSC. He also serves as a Distinguished Lecturer for the IEEE Circuits and Systems Society as well as for the IEEE Solid-State Circuits Society.

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We invite you to join or renew today to participate in exclusive educational events, access to leading research and best practice literature, and start your own career legacy by mentoring students and young professionals entering our field. It all starts with becoming a member of the Solid-State Circuits Society where you can:

- Connect with your Peers – valuable networking opportunities through our world-class conferences, publication offerings, social media extensions, and interactive educational opportunities.

- Keep up with the latest trends and cutting-edge developments in our industry – through our electronic newsletters, member magazine “Solid-State Circuits Magazine”, and our award winning “Journal of Solid State Circuits”.

- Access valuable career and educational tools - saving you both time and money with 24/7 access to our website and members-only professional development and educational material; Distinguished Lecturer Tours, Tutorials, and webinars by subject matter experts.

- Access exclusive SSCS Conference Digests for ISSCC, CICC, A-SSCC, ESSCIRC, and Symposium on VLSI Circuits.

CONFERENCE INFORMATION

-Access publications and EBooks – discounted access to vast online document libraries of journals, standards, and conference papers offer you one-third of the world's technical research to keep your knowledge current. Publications included in your SSCS membership are the "RFIC Virtual Journal" (RFVJ) and the "Journal on Exploratory Solid-State Computational Devices and Circuits" (JxCDC), Solid State Letters, and our newest Journal, the "Open Journal of Solid State Circuits" (OJ-SSC) an open access publication.

SSCS MEMBERSHIP SAVES EVEN MORE ON ISSCC REGISTRATION

This year, SSCS members will again receive an exclusive benefit of a \$30 discount on the registration fee for ISSCC in addition to the IEEE discount. Also, the SSCS will again reward our members with a \$10 Starbucks gift card when they attend the Conference as an SSCS member in good standing.

Join or renew your membership with IEEE's Solid-State Circuits Society today at sscs.ieee.org – you will not want to miss out on the opportunities and benefits your membership will provide now and throughout your career.

ITEMS INCLUDED IN REGISTRATION

Technical Sessions: Registration includes admission to all technical and special events. ISSCC does not offer partial conference registrations.

Technical Book Display: **Is still TBD.** Several technical publishers will have collections of professional books and textbooks for sale during the Conference.

Demonstration Sessions: Hardware demonstrations will support selected papers on Wednesday morning, February 23.

Publications: Conference registration includes:

-**The Digest of Technical Papers:** This year, as part of your Conference registration, the e-Digest of Technical Papers will be provided as part of the download. The e-Digest will include all 3 pages for each paper. Note that all 3 pages for each paper will be available on IEEE Xplore.

-**Papers Visuals:** The visuals from all papers presented will be available by download.

-**Demonstration Session Guidebook:** A descriptive guide to the Demonstration Session will be available by download.

-**Note:** Instructions will be provided for access to all downloads. Downloads will be available both during the Conference and for a limited time afterwards.

OPTIONAL EVENTS

Educational Events: Many educational events are available at ISSCC for an additional fee. There are twelve 90-minute Tutorials that will be available virtually, not in person at the conference. The forums and Short Course will be live, in-person. There will be two all-day Forums on Sunday. There are four additional all-day Forums on Thursday as well as an all-day Short Course. The Forums and Short Course include breakfast, lunch and break refreshments. See the schedule for details of the topics and times.

OPTIONAL PUBLICATIONS

ISSCC 2022 Publications: The following ISSCC 2022 digital publications can be purchased in advance or on site:

2022 ISSCC Download USB: All of the downloads included in conference registration, (regular papers and presentations) **(mailed in June)**

2022 Tutorials USB: All of the 90 minute Tutorials **(mailed in June).**

2022 Short Course USB: High Speed/High Performance Data Converters: Metrics, Architectures, and Emerging Topics **(mailed in June).**

The Short Course and Tutorial USBs contain audio and written English transcripts synchronized with the presentation visuals. In addition, the USBs contain a pdf file of the presentations and pdf files of key reference material.

Earlier ISSCC Publications: Selected publications from earlier conferences can be purchased. There are several ways to purchase this material:

-**Items listed on the registration website** can be purchased with registration and picked up at the conference.

-**Visit the ISSCC website** at www.isscc.org and click on the link "SHOP/Shop ISSCC/Shop Now" where you can order online or download an order form to mail, email or fax. For a small shipping fee, this material will be sent to you immediately and you will not have to wait until you attend the Conference to get it.



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