IEEE SOLID-STATE CIRCUITS SOCIETY

ADVANCE PROGRAM



2027 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

FEBRUARY
14, 15, 16, 17, 18

CONFERENCE THEME:

TRUSTED SUSTAINABLE SILICON INTELLIGENCE FROM EDGE TO CLOUD

SAN FRANCISCO
MARRIOTT MARQUIS HOTEL

DRAFT 11-23-2026

5-DAY PROGRAM

SUNDAY ALL-DAY

2 FORUMS: AI/HPC THROUGH MEMORY/ INTERCONNECT/POWER/ARCHITECTURE DC; SCALING ADC/DAC DESIGN

10 TUTORIALS: CIRCUIT DESIGN FOR ROBOTICS/AUTONOMOUS VEHICLES; SWITCHED-CAPACITOR POWER CONVERTERS; CLOCKING FOR ENERGY EFFICIENT PROCESSORS; TIME-DOMAIN ADCs; MACHINE LEARNING ACCELERATOR; DIGITAL CONVERSION FOR MULTI-MODAL SENSING;SCALING/DISTRIBUTION TECHNIQUES FOR mm-WAVE; ANALOG CIRCUIT DESIGN AUTOMATION; RADAR/SENSING; DIE-TO-DIE INTERFACE CIRCUITS

2 EVENING EVENTS: WiC PANEL; STUDENT RESEARCH PREVIEW

THURSDAY ALL-DAY

4 FORUMS: ELECTRICAL/OPTICAL CONNECTIVITY; AI OPTIMIZED SENSING; CIRCUITS/SYSTEMS FOR COMMUNICATION/SENSING/EDGE AI; QUANTUM REVOLUTION

SHORT-COURSE: HARDWARE SECURITY

ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and application to maintain technical currency, and to network with leading experts.

CONFERENCE TECHNICAL HIGHLIGHTS

On Sunday, February 14th, the day before the official opening of the Conference, ISSCC 2027 offers: • A choice of **ten** Tutorials, or

• A choice of **one** of **two** all-day Advanced-Circuit-Design Forums:
"Next-Generation AI and HPC Through Memory, Interconnect, Power, and Architecture Co-Design"
"Data Converters at the Bottleneck: Scaling ADC/DAC Design for 400G/Lane–3.2T Wireline Links"

The 90-minute tutorials offer background information and a review of the basics in specific circuit- and system-design topics. In the all-day Advanced-Circuit-Design Forums, leading experts present state-of-the-art design strategies in a workshop-like format. The Forums are targeted at designers experienced in the technical field.

On Sunday, February 14th, there are two events: ***"The Inner Node: Meditation, Resilience, and Well-Being by Women in Technology"*** starting at 1:30 pm and ***"The Analog Renaissance: Can Unconventional Physical Computing and Optical Interconnects Define the Next Strategic Leap?"*** will be offered starting at 6:00 pm. In addition, the ***Student-Research Preview (SRP),*** featuring a number of sixty-second introductory presentations followed by a poster session from selected graduate-student researchers from around the world will begin at 7:30 pm. First, the SRP will start with an inspirational talk by ***Professor Anantha Chandrakasan (MIT).***

On Monday, February 15th, ISSCC 2027 at 8:00 am offers four plenary papers on the theme: ***"Trusted Sustainable Silcon Intelligence from Edge to Cloud "***.

On Monday at 1:30 pm, there are six parallel technical sessions, followed by a Social Hour at 5:30 pm open to all ISSCC attendees. The Social Hour, held in conjunction with Book Displays and Author Interviews, will also include a Demonstration Session, featuring posters and live demonstrations of selected papers, along with a Corporate/Institution Exhibition.

On Tuesday, February 16th, there are six parallel technical sessions, both morning and afternoon. Book Displays and Author Interviews will be accompanied by a second Demonstration Session, along with the Corporate/Institution Exhibition. Tuesday evening includes the inaugural ***ISSCC Ping-Pong Challenge!***

On Wednesday, February 17th, there will be six parallel technical sessions, both morning and afternoon, followed by Author Interviews.

On Thursday, February 18th, ISSCC offers a choice of five all-day events:

• A Short Course entitled:
"Hardware Security, from Fundamentals to Implementations"

• Four Advanced-Circuit-Design Forums entitled:
"Emerging Electrical and Optical Connectivity: From System Architecture to Circuits"
"AI Optimized Sensing: Approaching Physical World Through Co-Designed Sensors and AI"
"Towards 6G: Circuits and Systems for Joint Communication, Sensing, and Edge AI"
"Enabling the Quantum Revolution: Silicon Systems for High-Precision Quantum Sensing and Computing"

This year, again, there is an option that allows an attendee to sample parts of all **five** Thursday offerings. Registration for educational events on Sunday and Thursday will be filled on a first-come first-served basis. Use of the ISSCC Web-Registration Site (http://www.isscc.org) is strongly encouraged. Registrants will be provided with immediate confirmation on registration for the Conference, Tutorials, Forums, and the Short Course.

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Optional Educational Events

ISSCC 2027 • Sunday, February 14th

Tutorials

8:30 AM

T1: Fundamentals of Circuit Design for Safe Robotics and Autonomous Vehicles

T2: Fundamentals of Switched-Capacitor Power Converter Designs

T3: Fundamentals of Adaptive Clocking for Energy Efficient Processors

10:30 AM

T4: Basics of Time-Domain ADCs: Principle and Simulation

T5: Machine Learning Accelerator Design Methodology

T6: Fundamentals of Supply-to-Digital Conversion for Multi-Modal Sensing with Energy-Harvesting

1:30 PM

T7: Fundamentals of LO Frequency Scaling and Distribution Techniques for mm-Wave

T8: Foundations and Frontiers in Analog Circuit Design Automation

3:30 PM

T9: Fundamentals of LO Generation for Radar and Sensing

T10: Basics of Die-to-Die Interface Circuits

ISSCC 2027 • Sunday, February 14th

Forums

8:00 AM

F1: Next-Generation AI and HPC Through Memory, Interconnect, Power, and Architecture Co-Design

F2: Data Converters at the Bottleneck: Scaling ADC/DAC Design for 448G–3.2T Wireline Links

Events Below are Included with your Conference Registration

ISSCC 2027 • Sunday, February 14th

1:30 PM - 3:00 PM

The Inner Node: Meditation, Resilience, and Well-Being by Women in Technology (Open to All)

3:30 PM - 5:30 PM:

Bingo Networking Event (Open to All)

Special Evening Session

6:00 PM - 7:30 PM:

EE1: The Analog Renaissance: Can Unconventional Physical Computing and Optical Interconnects Define the Next Strategic Leap?

Evening Event

8:00 PM

EE2: Student Research Preview: Short Presentations with Poster Session

ISSCC 2027 SCHEDULE OF EVENTS

Events Below are Included with your Conference Registration

ISSCC 2027 • Monday, February 15th Paper Sessions

8:30 AM	**Session 1:** Plenary - Invited Papers
1:30 PM	**Session 2:** Digital Circuits for Clocking, Power Management and Adaptive Techniques
1:30 PM	**Session 3:** Sensor Interfaces
1:30 PM	**Session 4:** mm-Wave Transceiver Building Blocks
1:30 PM	**Session 5:** Image Sensors and Ranging
1:30 PM	**Session 6:** Next-Generation Electrical and Optical Transceivers
1:30 PM	**Session 7:** Hybrid and Switched-Capacitor Power Converters

3:00 PM to 8:00 PM – Book Displays
3:00 PM to 8:00 PM – Corporations/Institution Exhibition
5:00 PM to 7:00 PM – Demonstration Session
5:30 PM – Author Interviews • Social Hour

ISSCC 2027 • Tuesday, February 16th Paper Sessions

8:00 AM	**Session 8:** Domain-Specific Accelerators and Processors
8:00 AM	**Session 9:** Power Management for AI & High-Performance Computing
8:00 AM	**Session 10:** High-Resolution Noise-Shaping ADCs
10:05 AM	**Session 11:** Integrated CMOS Transceivers and Arrays above 100GHz
8:00 AM	**Session 12:** Wearable and Portable Biosensing
8:00 AM	**Session 13:** High-Performance Die-to-Die and Clock Generation
8:00 AM	**Session 14:** High-Performance Multi-Band Wireless Transceivers and Receivers
10:05 AM	**Session 15:** Compute-in-Memory
1:30 PM	**Session 16:** Highlighted Chip Releases
3:35 PM	**Session 17:** Physical AI and Robotics
1:30 PM	**Session 18:** Ubiquitous Power Management
1:30 PM	**Session 19:** Advanced PLLs and VCOs
1:30 PM	**Session 20:** Advanced Beamforming Techniques for Phased Arrays and Reflectarrays
3:35 PM	**Session 21:** Amplifiers
1:30 PM	**Session 22:** SRAM, HBM and DRAM
1:30 PM	**Session 23:** Optics at the Edge
3:35 PM	**Session 24:** Low-Power Radio and Techniques

9:30 AM to 1:30 PM – Book Displays
9:30 AM to 1:30 PM – Corporations/Institution Exhibition
3:00 PM to 8:00 PM – Book Displays
3:00 PM to 8:00 PM – Corporations/Institution Exhibition
5:00 PM to 7:00 PM – Demonstration Session
5:30 PM – Author Interviews • Social Hour

ISSCC 2027 SCHEDULE OF EVENTS

Events Below are Included with your Conference Registration

ISSCC 2027 • Tuesday, February 16th

Evening Event

8:00 PM

EE3: ISSCC Ping-Pong Challenge 2027

ISSCC 2027 • Wednesday, February 17th Paper Sessions

8:00 AM	**Session 25:**	Compute-In-Memory-Centric SoCs and Domain-Specific Accelerators
10:05 AM	**Session 26:**	Late Breaking Industry Highlights
8:00 AM	**Session 27:**	Ultra-Broadband and High-Speed ADCs
8:00 AM	**Session 28:**	Advanced Digital and RF Techniques for cm-Wave
8:00 AM	**Session 29:**	Advanced Systems for Neural Interfaces and Signal Processing
8:00 AM	**Session 30:**	3D NAND and RRAM Memories
10:05 AM	**Session 31:**	Hardware Security
8:00 AM	**Session 32:**	Displays
10:05 AM	**Session 33:**	Optimization Accelerators
1:30 PM	**Session 34:**	Visual Computing Accelerators and Processors
1:30 PM	**Session 35:**	Oscillators, Frequency and Voltage References
1:30 PM	**Session 36:**	Energy Harvesting, WPT and Piezo Actuators
3:35 PM	**Session 37:**	From Circuits to Waves: Signal Processing in Frequency, Time, and Space
1:30 PM	**Session 38:**	Circuits for Quantum and Other Unconventional Compute
1:30 PM	**Session 39:**	Memory Interfaces
1:30 PM	**Session 40:**	High-Frequency Synthesizers and LO Generation

5:30 PM – Author Interviews

Optional Educational Events

ISSCC 2027 • Thursday, February 18th

Forums

8:00 AM

F3: Emerging Electrical and Optical Connectivity: From System Architecture to Circuits

F4: AI Optimized Sensing: Approaching Physical World Through Co-Designed Sensors and AI

F5: Towards 6G: Circuits and Systems for Joint Communication, Sensing, and Edge AI

F6: Enabling the Quantum Revolution: Silicon Systems for High-Precision Quantum Sensing and Computing

Short Course

8:00 AM

SC: Hardware Security, from Fundamentals to Implementations

ISSCC 2027 Circuit Insights

(Saturday, February 13, 2027, 8:45 AM – 6:00 PM)

Organizer/Moderator:
Ali Sheikholeslami, *University of Toronto, Toronto, Canada*
ISSCC Education Chair

ISSCC 2027 offers the sixth edition of its Circuit Insights on Saturday, February 13, 2027, 8:45 am - 6:00 pm PST. As in the past five years, this event is targeting 3rd- and 4th-year undergraduate students and starting graduate students in the area of circuit design but may be of interest to new circuit design engineers as well. The event will be held in person for a small audience of 50 students (by invitation only) at the ISSCC venue at the Marriott Hotel in San Francisco, and will be recorded for later release on the SSCS/ISSCC YouTube channel.

The event consists of a series of talks on circuit design from industry and academia. Each talk will be 50 minutes long followed by a 10-minute interactive Q&A Session at the end.

The full agenda will be available soon on ISSCC.org/insights

TUTORIALS

There are a total of 10 tutorials this year on 10 different topics. Each tutorial, selected through a competitive process within each subcommittee of the ISSCC, presents the basic concepts and working principles of a single topic. These tutorials are intended for non-experts, graduate students and practicing engineers who wish to explore and understand a new topic.

A Certificate of Completion will be issued to all in-person tutorial attendees who complete a short questionnaire at the end of the tutorial.

Sudip Shekhar
ISSCC Tutorials Chair

8:30 AM

T1: Fundamentals of Circuit Design for Safe Robotics and Autonomous Vehicles

Caspar van Vroonhoven
Analog Devices, Munich, Germany

Robotics and Autonomous Driving are dramatically increasing the need for ICs that meet functional safety requirements: Fail-Safe or even Fail-Operational behavior is required in systems that handle e.g. motion control, steer-by-wire, brake-by-wire and energy management. This tutorial focuses on analog and mixed-signal IC design for such applications. The tutorial will focus on architecture development for safety applications and practical circuit design for safe monitoring and actuation ICs.

Caspar van Vroonhoven holds a Ph.D. degree from Delft University of Technology and is currently a Director of Mixed-Signal IC Design at Analog Devices, working on battery management. He has authored 14 papers, received best-paper awards from ISSCC and other conferences, and holds 12 patents.

8:30 AM

T2: Fundamentals of Switched-Capacitor Power Converter Designs

Mo Huang
University of Macau, Macau, Macau, China

Switched-capacitor (SC) converters enable significantly higher power density when compared to conventional inductive converters. This tutorial provides a comprehensive overview of SC converter design fundamentals, including working principles, output regulation and power-loss analysis. Furthermore, it explains the construction of high-order SC topologies, and continuously scalable-conversion-ratios (CSCR) SC converters that mitigate the inherent efficiency-regulation trade-off.

Mo Huang received the Ph.D. degrees from Sun Yat-sen University, Guangzhou, China, in 2014. He is currently an Associate Professor in the University of Macau. His research interests are power management integrated circuits and systems. He has served as TPC member of ISSCC and CICC.

8:30 AM

T3: Fundamentals of Adaptive Clocking for Energy Efficient Processors

Visvesh S. Sathe
Georgia Institute of Technology, Atlanta, GA

This tutorial provides a comprehensive overview of adaptive clocking, outlining the benefits afforded by various architectures and their associated implementation challenges. We analyze the critical factors that dictate the effectiveness of adaptive clocking and explore key underlying circuit structures. Finally, we discuss common pitfalls encountered when deploying these techniques in silicon.

Visvesh Sathe is an Associate Professor at the Georgia Institute of Technology where his group works on digital, mixed-signal, and integrated power circuit architectures for energy-efficient processing. He has previously held positions at UW and at the Low-power Advanced Development Group at AMD.

10:30 AM

T4: Basics of Time-Domain ADCs: Principle and Simulation

Chi-Hang (Ivor) Chan
University of Macau, Macau, Macau, China

Traditional ADCs quantize voltage amplitudes, but CMOS scaling limits this through lower supply voltages and reduced dynamic range. Modern high-speed ADCs are shifting to the time domain. Time-domain (TD) ADCs leverage time-based circuits, offering a digitally intensive, scaling-friendly alternative. This tutorial covers core TD principles and building blocks like VTCs, TDCs, and time amplifiers, key architectures like GROs and delay lines, and practical simulation and testbench design.

Chi-Hang (Ivor) Chan received his B.S. from the University of Washington and M.S./Ph.D. from the University of Macau, where he is an associate professor at SKL-AMSV. IEEE SSCS Macau Chapter Chair and 2024 ISSCC Takuo Sugano Award winner, he has 50+ JSSC/ISSCC papers focusing on high-speed Nyquist ADCs, NS converters, and low-jitter clock circuits.

10:30 AM

T5: Machine Learning Accelerator Design Methodology

Priyanka Raina
Stanford University, Stanford, CA

Designing high-performance and energy-efficient machine-learning (ML) accelerators requires significant engineering effort, and as the rapidly evolving field of machine learning develops new models, the current approach of designing ad-hoc accelerators does not scale. This talk will introduce recent research on high-level synthesis (HLS)-based design space exploration and generation frameworks for programmable ML accelerators, and compilers for mapping to them.

Priyanka Raina is an Associate Professor of Electrical Engineering at Stanford University. Her research focuses on high-performance, energy-efficient hardware accelerators and agile hardware-software co-design. Her work has received multiple best-paper awards and major faculty honors.

10:30 AM

T6: Fundamentals of Supply-to-Digital Conversion for Multi-Modal Sensing with Energy-Harvesting

Kiichi Niitsu
Kyoto University, Kyoto, Japan

Supply-to-digital architectures bypass the complexity of traditional wireless sensors by utilizing the harvested energy fluctuations as the data payload itself, without needing an explicit ADC. I will introduce the fundamentals and trends of supply-to-digital conversion as well as its example applications in biomedical IoTs, specifically bio-fuel-cell-operated biosensing systems including tear-glucose-driven glucose/timing monitoring smart contact lenses, and stomach-acid-driven digital pills.

Kiichi Niitsu received his B.S., M.S. and Ph.D. in Engineering from Keio University, Japan. He is a professor at Kyoto University. He focuses on circuits and systems for biomedical IoTs. He received the ISSCC Silkroad Award and BioCAS Best Paper/Demo Awards. He serves on the TPCs of the ISSCC and CICC.

1:30 PM

T7: Fundamentals of LO Frequency Scaling and Distribution Techniques for mm-Wave

Vadim Issakov
Braunschweig University of Technology, Braunschweig, Germany

In modern CMOS nodes, the optimal VCO frequency is around 10GHz. Thus, for mm-wave systems we need to scale the LO frequency up and efficiently deliver the LO signal internally. In this tutorial we will cover system-level considerations on frequency planning, bandwidth, phases, power consumption and noise. Theory and circuit techniques for non-linearity-based and injection-locked frequency multipliers are discussed. Phase generation techniques are also addressed.

Vadim Issakov received MSc from TU Munich in 2006 and PhD from the University of Paderborn, in 2010. Same year he joined Infineon. Afterwards, he was with imec, Belgium, and then with Intel. In 2015 he came back to Infineon as Lead Principal mm-wave. Since April 2021 he is with TU Braunschweig.

1:30 PM

T8: Foundations and Frontiers in Analog Circuit Design Automation

Xuan Zhang
Northeastern University, Boston, MA

Artificial intelligence is transforming IC design automation.This tutorial builds that foundation and covers the AI fundamentals that are grounded in transistor-level circuit-design challenges. Topics span circuit-topology generation, performance modeling, design-space optimization, and agentic design frameworks, illustrated through recent frontier research. Attendees will leave with the conceptual vocabulary and the broader perspective to envision how AI and IC design will co-evolve.

Xuan 'Silvia' Zhang is an Associate Professor at Northeastern University. Her research is at the intersection of AI, electronic design automation, and computer architecture, with a focus on open-source AI-driven design flow (https://github.com/xz-group) and AI hardware co-design.

3:30 PM

T9: Fundamentals of LO Generation for Radar and Sensing

Wu-Hsin Chen
Qualcomm, San Diego, CA

This tutorial demonstrates LO design to radar system performance. It derives how chirp bandwidth, chirp-to-chirp phase and array phase set range, velocity and angle resolution, then reviews synthesizer architectures for chirp generation — from fractional-N PLLs to two-point modulation. It connects phase-noise impacts on the radar LO, including TX-RX correlation and spillover-tone limits, covers chirp linearity and LO delivery. The tutorial closes on a discussion of radar for 6G ISAC.

Wu-Hsin Chen is a Principal Engineer at Qualcomm specializing in RFIC design and integration. He received his B.S. and M.S. degrees from National Taiwan University and his Ph.D. in ECE from Purdue University. His work focuses on RF synthesizers, mm-wave LO, and next-generation wireless technologies.

3:30 PM

T10: Basics of Die-to-Die Interface Circuits

Didem Turker Melek
Cadence Design Systems, San Jose, CA

This tutorial provides a detailed discussion of die-to-die links and how to build die-to-die transceiver circuits. Chiplet-driven disaggregation and system-in-package concepts will be introduced, package technologies and prevailing standards in D2D space will be examined. Topics covered will include design challenges for low-power and high bandwidth D2D transceivers, specifically receiver, transmitter and clocking circuits, state-of-the-art design examples and future directions.

Didem Turker Melek is a Sr. Group Director in Silicon Solutions Group at Cadence where she leads the Die-to-Die Product Group. She authored numerous papers and patents on wireline transceivers and received the ISSCC 2019 Outstanding Forum Speaker Award. She has a Ph.D. in EE from Texas A&M University.

Next-Generation AI and HPC Through Memory, Interconnect, Power, and Architecture Co-Design

Organizers: **Alfred Yeung,** *AMD, Santa Clara, CA*
Juang-Ying Chueh, *Etron Technology, Taipei, Taiwan*

Co-Organizers: **Win-San (Vince) Khwa,** *TSMC, Hsinchu, Taiwan*
Nicolas Butzen, *Intel, Hillsboro, OR*
Srividhya Venkataraman, *AMD, Santa Clara, CA*
Tamer Ali, *Mediatek, Irvine, CA*

Champions: **Kousuke Miyaji,** *Shinshu University, Nagano, Japan*
Meng-Fan (Marvin) Chang, *National Tsing Hua University, TSMC, Hsinchu, Taiwan*

AI-HPC infrastructure faces rapid changes in demand as workloads proliferate and model sizes grow, creating compounding bottlenecks across power delivery, memory bandwidth, data-access latency, and thermal constraints. No single layer in the hardware stack can address these challenges alone — innovations at each layer must work together as a co-designed system.

This forum takes a vertical view across the hardware stack, bringing together experts spanning memory architecture, circuit design, photonics, power systems, and thermal engineering. Topics range from data-center architecture, memory and storage bandwidth, and low-latency on-chip memory, through 3D multi-die integration and photonic interconnect, to the system-level challenges of powering, cooling, and securing AI infrastructure at data-center scale.

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Introduction** **Alfred Yeung,** *AMD, Santa Clara, CA*
8:25 AM	**AI System Architecture: From Foundation Models to Data-Center Design** **William Dally,** *Nvidia, Santa Clara, CA*
9:15 AM	**Integrating NAND Flash Memory into AI Computing Systems for Scalable Inference** **Ken Takeuchi,** *University of Tokyo, Tokyo, Japan*
10:05 AM	Break
10:20 AM	**Redesigning AI Systems: Toward Memory-Centric Processing** **Hai Li,** *Duke University, Durham, NC*
11:10 AM	**3D Integration, Hybrid Bonding, and Advanced Packaging** **Ravi Mahajan,** *Intel, Chandler, AZ*
12:00 PM	Lunch
1:20 PM	**High Performance Electrical and Optical Interconnect** **Keren Bergman,** *Columbia University, New York, NY*
2:10 PM	**Data-Center Power-Delivery Architecture** **Mehdi Jatlaoui,** *Murata, Caen, France*
3:00 PM	Break
3:15 PM	**Thermal Management and Cooling: Chip to Rack** **Yuejin Guo,** *Shenzhen University, Shenzhen, China*
4:05 PM	**Reliability and Security for AI Systems** **Charles Matar,** *Synopsys, Sunnyvale, CA*
4:55 PM	Closing Remarks

Data Converters at the Bottleneck: Scaling ADC/DAC Design for 400G/Lane–3.2T Wireline Links

Organizers: **Athanasios (Thanos) Ramkaj,** *AMD, San Jose, CA*
Chin-Yu Lin, *Mediatek, Hsinchu, Taiwan*

Co-Organizers: **Vanessa Chen,** *Carnegie Mellon University, Pittsburgh, PA*
Jay Im, *AMD, San Jose, CA*

Champions: **Kenny Cheng-Hsiang Hsieh,** *TSMC, Hsinchu, Taiwan*
Mike Chen, *University of Southern California, Los Angeles, CA*

Analog-to-digital (ADC) and digital-to-analog (DAC) converters have become the central bottleneck in scaling ultra-high-speed electrical and optical transceivers, dominating power, area, bandwidth, and calibration complexity at 400G/lane and beyond. As system-level requirements — spanning modulation formats, channel loss, jitter, and process scaling — tighten toward the 3.2T era, data-converter design is increasingly dictated by end-to-end system constraints.

This Forum brings together experts from academia and industry to present a converter-centric perspective on next-generation wireline systems, covering architecture, circuit design, and physical implementation. The program first examines the evolution of sub-ADC topologies and time-interleaving techniques alongside high-speed DAC design. It then addresses the critical enabling roles of clocking, analog front-end bandwidth, timing control, and calibration and behavioral modeling methodologies.

Through state-of-the-art silicon demonstrations and design case studies, this Forum delivers a unified view of how converter architectures and their supporting circuits must co-evolve to overcome the challenges of 400G/lane and beyond, paving the way to the 3.2T wireline frontier.

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Introduction** **Athanasios (Thanos) Ramkaj,** *AMD, San Jose, CA*
8:25 AM	**Beyond the Channel: System-Level Co-Optimization of ADC/DAC Requirements for 400G/Lane Electrical and Optical Links** **Rubén Pérez-Aranda,** *Cisco, Madrid, Spain*
9:15 AM	**Sub-ADC Topologies for 400G+ Wireline Links: From Classical Limits to Emerging Alternatives** **Minglei Zhang,** *University of Macau, Macau, China*
10:05 AM	Break
10:20 AM	**Time-Interleaving for 400G: Analysis, Design, and Implementation Trends** **Aida Varzaghani,** *Cadence, San Jose, CA*
11:10 AM	**High-Speed DAC Design for 400G: Distortion, Bandwidth, Jitter and Output Driver Challenges** **Bart Moeneclaey,** *Imec, Ghent, Belgium*
12:00 PM	Lunch
1:20 PM	**Sub-100fs Clocking for Ultra-High-Speed ADC/DAC-Based Wireline Links** **Behzad Razavi,** *UCLA, Los Angeles, CA*
2:10 PM	**ADC/DAC Analog Front-End Design Beyond 100GHz: Bandwidth, Noise, and Layout Constraints** **Marco Cusmai,** *Synopsys, Pavia, Italy*
3:00 PM	Break
3:15 PM	**Data-Converter Imperfections and Calibration for Ultra-High-Speed SerDes: Modeling and Link-Level Impact** **Gain Kim,** *DGIST, Daegu, Korea*
4:05 PM	**ADC/DAC Design for Coherent Optical Transceivers: Resolution, Linearity, and DSP Co-Design at 400G** **Ray Nguyen,** *Marvell, Irvine, CA*
4:55 PM	Closing Remarks

1:30 PM – 3:00 PM

The Inner Node: Meditation, Resilience, and Well-Being by Women in Technology (Open to all Attendees)

In today's fast-paced and constantly connected world, many women in technology balance demanding careers, family responsibilities, and personal aspirations, often leaving little time to recharge. This interactive session explores practical techniques to cultivate resilience, mental clarity, and inner well-being, helping participants navigate challenges with greater ease, focus, and balance.

Speaker: Vinita Deodhar, *Senior Meditation Instructor and National Coordinator, Art of Living Foundation, Boston, MA*

3:30 PM – 5:30 PM

Bingo Networking Event (Open to all Attendees)

Women in Circuits (WiC) together with ISSCC will be holding a networking and mentoring session on Sunday afternoon. Distinguished panelists from the career panel, WiC members, and other participants will play getting-to-know-you bingo to promote engagement between various members of the community. This will give participants the chance to network and mingle with people across a spectrum of seniority in the field in a casual setting.

6:00 PM – 7:30 PM

EE1: The Analog Renaissance: Can Unconventional Physical Computing and Optical Interconnects Define the Next Strategic Leap?

As traditional digital scaling yields diminishing returns, securing long-term leadership in advanced computing requires looking fundamentally beyond standard von Neumann architectures. Just as the limits of copper interconnects accelerate the shift to co-packaged optics, a parallel power and bandwidth crisis is forcing a radical rethink of the compute engine itself. To break these barriers, academia and industry are driving an "Analog Renaissance," choosing to harness the intrinsic, complex physical properties of devices rather than fighting them. This panel explores the strategic realities of unconventional hardware, from continuous-time neuromorphic systems and dense analog in-memory compute, to leveraging thermodynamic noise for probabilistic and quantum-inspired algorithms. We bring together pioneers of these exotic substrates and digital traditionalists to debate a critical question: Can we reliably compute in scale using stochasticity and raw device physics while developing the next generation of interconnects, or will the precision of synchronous digital CMOS always dominate?

Moderator: **Aishwarya Natarajan,** *Hewlett Packard Labs (HPE), Milpitas, CA*

Panelists:
Joyce Poon, *University of Toronto, Toronto, Canada*
Tulika Mitra, *National University of Singapore, Singapore*
Karin Strauss, Microsoft Research, *Redmond, WA*
Aida Todri-Sanial, *TU Eindhoven, Eindhoven, The Netherlands*
Cat Graves, Google DeepMind, *San Francisco, CA*

EE2:
Student Research Preview (SRP)

The Student Research Preview (SRP) will highlight selected student research projects in progress. The SRP consists of a number of sixty-second presentations followed by a Poster Session, by graduate students from around the world, which have been selected on the basis of a short submission concerning their on-going research. Selection is based on the technical quality and innovation of the work. This year, the SRP will be presented in three theme sections.

The SRP will include an inspirational lecture. The SRP begins at 8:00 pm on Sunday, February 14th, and is open to all ISSCC registrants.

SRP Organizing Committee

Co-Chair:	**Rabia Tugce Yazicigil,** *Boston University, Boston, MA*
Co-Chair:	**Mondira (Mandy) Pant**, *Intel, MA*
Advisor:	**Anantha Chandrakasan**, *Massachusetts Institute of Technology, MA*
Advisor:	**Jan Van der Spiegel**, *University of Pennsylvania, Philadelphia, PA*
Media/Publications:	**Laura Fujino**, *University of Toronto, Toronto, Canada*
A/V:	**Trudy Stetzler**, *Halliburton, Houston, TX*

Committee Members

Utsav Banerjee
IISC, India

Woo-Seok Choi
Seoul National University, Korea

Zeynep Deniz
IBM, NY

Sijun Du
Delft University of Technology, The Netherlands

Philex Fan
National Cheng Kung University, Taiwan

Yingying Fan
Washington University in St. Louis, MO

Pasqualina Fragneto
ST Microelectronics, Italy

Antoine Frappe
University of Lille, France

Preet Garcha
Texas Instruments, TX

Ulkuhan Guler
Worcester Polytechnic Institute, MA

Mohamed Ibrahim
Cornell University, NY

Yaoyao Jia
The University of Texas at Austin, TX

Kyuho Jason Lee
Yonsei University, Korea

Jiamin Li
Southern University of Science and Technology, China

Xilin Liu
University of Toronto

Zeynep Lulec
Marvell Technology, Toronto

Saurav Maji
Nvidia, CA

Nandish Mehta
Nvidia, CA

Noriyuki Miura
Osaka University, Japan

Mondira Pant
Intel, MA

Angelo Parisi
imec, Belgium

Pei-Yun Tsai
National Taiwan University, Taiwan

Rabia Tugce Yazicigil
Boston University, MA

Plenary Session — Invited Papers

Chair: **Thomas Burd**, *Advanced Micro Devices, Santa Clara, CA*
ISSCC Conference Chair

Associate Chair: **Marian Verhelst,** *KU Leuven, Heverlee, Belgium*
ISSCC International Technical Program Chair

8:30 AM
FORMAL OPENING OF THE CONFERENCE

8:50 AM
1.1 Holistic Semiconductor Lithography for the Age of AI

Marco Pieters, *Executive Vice President and Chief Technology Officer*
ASML, Veldhoven, The Netherlands

Artificial intelligence (AI) is generating strong demand for semiconductor chips, especially at the leading edge. This dynamic is fueling innovation in the semiconductor industry to continue with geometrical scaling, with the accompanying benefits of reduced power consumption and increased operating speed, and to speed up the development of device and circuit stacking in the third dimension to further increase density and improve connectivity. In this presentation, we will present ASML's holistic lithography technology roadmap designed to meet the needs of the AI revolution. Our roadmap brings together EUV lithography (both 0.33 NA and high NA), DUV lithography (including 193-nm immersion), computational lithography, wafer inspection and metrology, and increasingly sophisticated control loops to improve resolution, overlay accuracy (including post-bonding overlay), process control, productivity, and to reduce the cost of technology. We will highlight the role of high-NA EUV lithography in reducing process complexity and cost by eliminating multi-patterning and, for logic integrated circuits, re-enabling 2D design and routing. We will discuss ASML's expanding role in advanced packaging and 3D integration to enable further density increase and connectivity speedup. We will demonstrate that, while AI drives demand for more powerful semiconductor chips, it is also part of holistic semiconductor lithography, enhancing modelling, simulation, metrology, and control loops to improve lithography performance and process control. Finally, advancing technology in the AI era is a shared challenge of the entire semiconductor ecosystem, requiring continued innovation and collaboration across research partners, equipment, material, and EDA suppliers, and chipmakers.

9:20 AM
1.2 The Next Leap in Image Sensors: Pixels and Beyond in the AI Era

Yusuke Oike, *CTO / Senior Vice President, R&D*
Sony Semiconductor Solutions, Atsugi, Japan

Relentless advances in pixel technology have transformed image sensors, delivering unprecedented imaging performance. Looking ahead, the next leap goes beyond pixels to reshape camera systems in response to rapid AI advancement. This talk highlights advances pushing pixel limits for faithful imaging, AI-leveraged imaging that enriches the photographic experience, and reliable multimodal sensing that provides low-latency observations physical AI needs to see and act in the real world.

9:50 AM
ISSCC, SSCS, IEEE AWARD PRESENTATIONS

10:15 AM
BREAK

10:45 AM

1.3 At the End of the Copper Tunnel, There Is Light

Matt Murphy, *Chairman and Chief Executive Officer, Marvell, Santa Clara, CA*

For over half a century, semiconductor progress was defined by transistor density. But with the dawn of AI, the bottleneck has shifted from how fast a chip can think to how fast the collective can share its thoughts. Whether connecting chiplets inside a package, AI servers within a rack, rows of servers across a datacenter, or bridging remote datacenters into a single cluster — connectivity is the key to AI efficiency.

Copper interconnects are the backbone of computing today, and pushing their limits of speed, reach, and power is an art that very few possess. But as AI pushes boundaries, copper hits a wall. Behind that wall is the light of optical links that will shape the AI datacenter. The move from copper to optics represents a structural rearchitecting of AI infrastructure, and one of the most consequential opportunities for semiconductor innovation today.

We'll discuss what drives this shift, how different optical technologies serve each layer of the AI datacenter, and what enables silicon photonics, optical DSPs, and co-packaged optics to make this transition economically viable at volume — allowing AI scale to continue and greater intelligence to be realized.

11:15 AM

1.4 From Silicon to Deployed Infrastructure: Redefining the Semiconductor Design Challenge at Hyperscale

Rani Borkar, *President, Azure Hardware Systems and Infrastructure Microsoft, Redmond, WA*

The demands of hyperscale AI infrastructure are redefining the semiconductor design challenge, because the distance between great silicon and great deployed infrastructure is wider and more consequential than ever. The optimization aperture continues to expand, with networking and memory architecture playing an increasingly first-order role in shaping design decisions across the stack, from die and package through rack, cluster, datacenter, and even regional infrastructure. At the same time, the center of gravity is shifting away from any single accelerator and toward composing the right system from purpose-built CPUs, high-performance storage, and heterogeneous, disaggregated AI accelerators. At production scale, reliability, manageability, and the ability to rapidly bring new hardware generations into production also become central to translating design advantage into deployed value. This plenary explores how those demands are reshaping hardware tradeoffs and linking silicon choices to the economics of delivering AI at global scale.

11:45 AM

PRESENTATION TO PLENARY SPEAKERS

11:50 AM

CONCLUSION

Digital Circuits for Clocking, Power Management and Adaptive Techniques

Session Chair:

Sylvain Clerc, *CEA-LIST DSCIN/LFIM, Grenoble, France*

Session Co-Chair:

Ping-Hsuan Hsieh, *National Tsing Hua University, Hsinchu, Taiwan*

1:30 PM

2.1 A 2nm GAA 4.7GHz Tri-Gear Armv9.4-A CPU Subsystem with Intra-Gear DVFS for Flagship Mobile SoCs

J. Lerdworatawee[1], H. Chen[2], S. Gururajarao[2], J. Xiong[2], E. Ho[2], G. Gammie[2], T. Chen[2], A. Varma[2], D. Mikan[2], H-H. Yu[3], J-H. Yang[3], Q. Sun[2], I. Lin[2], T-A. Yeh[3], Y-R. Tsai[3], Y-W. Chien[3], Y-C. Chiu[3], B. Huang[2], C-H. Chiang[3], A. Rajagopalan[2], A. Thippana[2], E. Wang[3], S. Hwang[3], K. Jou[3]

[1]MediaTek, San Diego, CA
[2]MediaTek, Austin, TX
[3]MediaTek, hsinchu, Taiwan

1:55 PM

2.2 A 2.1GHz Fully Resonant Clocked, Static Latch-Based Generalized Matrix Multiplier with Inductor-Over-Logic Integration in 16nm CMOS

E. Basaran, J. Park, Z. Yin, J. A. Arenas, V. Sathe

Georgia Institute of Technology, Atlanta, GA

2:20 PM

2.3 A Data Feed-Forward Digital LDO for an Adaptively Clocked 8×8 Systolic-Array GEMM Accelerator in 65nm CMOS

J. Arenas, Z. Yin, C-H. Huang, K. Hau, H. S. Ozturk, V. Sathe

Georgia Institute of Technology, Atlanta, GA

2:45 PM

2.4 A 12nm 256TOPS CIM-Centric SoC with Model-Scale-Aware Scheduling, IR-Drop Mitigation and CIM BIST/Repair for CV-to-LLM Inference

A. Guo[1], G. Chen[1], Y. Zhao[2], W. Gao[1], X. Liu[3], D. Yang[3], Z. Wang[2], G. Sun[4], Q. Wu[3], X. Si[5]

[1]HOUMO, Shanghai, China
[2]HOUMO, Beijing, China
[3]HOUMO, Nanjing, China
[4]Peking University, Beijing, China
[5]Southeast University, Nanjing, China

Break 3:10 PM

3:35 PM

2.5 6.7GHz Dual-Edge Clocked Compiled Memories in 2nm

P. Salz[1], W. Penth[1], M. Lee[2], S. Penth[1], B. Huott[3], P. Beck[1], P. Toth[1], H. Wetter[1], M. Kugel[1], A. Cook[1], U. Srinivasan[3], K. Kalafala[3], M. Verma[4], X. Zhao[3]

[1]IBM, Ehningen, Germany
[2]IBM, Austin, TX
[3]IBM, Poughkeepsie, NY
[4]IBM, Bangalore, India

4:00 PM

2.6 A 16-Element mm-Wave Digital Beamformer with Adaptive-Rate Joint Beam Tracking/Nulling and Dynamic Power Management

J-J. Park, H. S. Ozturk, J. Shin, S. T. King, M. M. Bolding, R. S. Westafer, V. Sathe

Georgia Institute of Technology, Atlanta, GA

4:25 PM

2.7 A 65nm 33.34mW 8-Element Adaptive Baseband Beamformer with Per-Element 2D Complex-Weighting SAR ADCs and a Reconfigurable GSC

G. Joung[1], S. Konno[2], A. Assoa Sangbone[3], A. Bhat[3], S. Spetalnick[3], Y-J. Kim[1], C. S. Cho[1], A. Raychowdhury[3], S. Ryu[1]

[1]Korea Aerospace University, Goyang, Korea
[2]Asahi Kasei Microdevices, Yokohama, Japan
[3]Georgia Institute of Technology, Atlanta, GA

4:50 PM

2.8 Cobalt 200: Microsoft Azure's Cloud-Native CPU Leveraging Per-Core Power Management for Power-Constrained Performance

A. Deval[1], C. Schaef[2], D. Bachand[3], B. Sutton[4], R. Hoffman[3], A. Cefal[5], A. Venkataraman[6], N. Khoury[5], R. Rivera[1], P. Dave[1], T. Mapes[1], P. Misra[1], A. Azam[5], M. Subhadra[5], J. Franke[5], S. Badran-Louca[3], D. Estrada[5], A. Chandran[5]

[1]Microsoft, Redmond, WA
[2]Microsoft, San Diego, CA
[3]Microsoft, Morrisville, NC
[4]Microsoft, Westfield, IN
[5]Microsoft, Hillsboro, OR
[6]Microsoft, Mountain View, CA

Conclusion 5:15 PM

Sensor Interfaces

Session Chair: ***Chinwuba Ezekwe,*** *Robert Bosch, Sunnyvale, CA*

Session Co-Chair: ***Inhee Lee,*** *University of Pittsburgh, Pittsburgh, PA*

1:30 PM

3.1 A PCB Shunt-Pair-Based Current Sensor with 0.017% Peak Self-Heating-Induced Error for a 35A Current Step

P. Park[1,2], W. B. Kim[1], S. Cho[1]

[1]KAIST, Daejeon, Korea

[2]*now at Massachusetts Institute of Technology, Cambridge, MA

1:55 PM

3.2 A 122dB-DR Hybrid Magnetic Sensor with ±145mT Input Range and ±0.34% Sensitivity Variation from –40°C to 120°C

J. Liu[1], T. Qu[1], L. Xiang[1], J. Zhu[2], X. Shen[2], Z. Hong[1], J. Xu[1]

[1]Fudan University, Shanghai, China

[2]Novosense Microelectronics, Shanghai, China

2:20 PM

3.3 A BMIC for Module- and System-Level EIS Featuring 2.1μV/√Hz Input-Referred Noise at 1Hz and 2.3μs Inter-IC Synchronization

K. Matsukawa[1], K. Honda[1], K. Sakata[1], T. Ito[1], T. Kitamura[1], M. Tsukahara[1], A. Ogawa[1], T. Takaue[1], I. Ishibe[1], K. Nakamura[2], Y. Furuta[2], T. Nezuka[2]

[1]DENSO, Aichi, Japan

[2]MIRISE Technologies, Aichi, Japan

2:45 PM

3.4 A 4.1/6.9fJ/Conversion-Step Pipelined-SAR Capacitance-to-Digital Converter with Merging-First Switching, Ratio-Scaled Detect-and-Skip Technique, and Load-Aware Reference Buffer

X. Huang, J. Gao*, Z. Wu, L. Shen*

Peking University, Beijing, China

*Equally Credited Authors (ECAs)

Break 3:10 PM

3:35 PM

3.5 A Fractional-N-PLL-ΔΣM-Hybrid Time-Domain Capacitance-to-Digital Converter with 187.4dB FoM_S and 374pF Input Range

M. Jiang, Y. Cheng, H. Wang, P. Yao, D. Wu, J. Tang, B. Gao, H. Qian, S. Pan, H. Wu

Tsinghua University, Beijing, China

4:00 PM

3.6 A 21.8μg/√Hz Noise Floor, 0.375mg/g² VRC, MEMS Capacitive Accelerometer Using a Multiplexed CVC Technique

C. Wenfei[1], Z. Longjie[1], M. Zhixing[1], W. Ling[1], Z. Zhangming[2,3]

[1]Xidian University, Xi'an, China
[2]Hangzhou Institute of Technology, Hangzhou, China
[3]Xidian University, Hangzhou, China

4:25 PM

3.7 A 99.3dB SNR 60fps Zoom-PFM-Based Readout IC for Large-Scale Resistive Tactile Sensor Array

R. Duan, J. Xu, Z. Chen, Q. Xia, F. Zhou, Y. Zhuo, Y. Zhang, Z. Chen, W. Lu

Peking University, Beijing, China

4:50 PM

3.8 A 34.5μΩ-Resolution 10.5μs-Conversion-Time Resistance Sensor for Online Discrete SiC Power Device Junction-Temperature Monitoring

W. Xu, Y. Liu, M. Zhang, Q. Fan

Delft University of Technology, Delft, The Netherlands

5:05 PM

3.9 A 6.3μs 2.7nJ/conversion Bipolar-Free Temperature Sensor with Distributed Remote Sensing and Single-Point Calibration in 2nm GAA Technology

L. Fassio[1], B. Grave[1], F. S. Sinisi[1], K. Sadeghipour[1], P. Metku[2], B. Pang[3], P. Hesamaddin[4], L. Lu[3], M. Roham[3], D. Alladi[3], K. A. O'Donoghue[1]

[1]Qualcomm, Cork, Ireland
[2]Qualcomm, Austin, TX
[3]Qualcomm, San Diego, CA
[4]Qualcomm, Irvine, CA

Conclusion 5:20 PM

mm-Wave Transceiver Building Blocks

Session Chair: ***Wooyeol Choi,*** *Seoul National University, Seoul, Korea*
Session Co-Chair: ***Taiyun Chi,*** *Rice University, Houston, TX*

1:30 PM

4.1 A 20-to-30GHz 0.13mm² Voltage-Mode Doherty Power Amplifier with >24% PAE_{6dB} and 3:1 VSWR Load Tolerance Supporting 6Gb/s 64QAM for 5G NR and K/Ka NTN/SATCOM Phased Arrays

F. Svelto, B. A. Abdelmagid, A. Wang, H. Wang
ETH Zürich, Zurich, Switzerland

1:55 PM

4.2 A 60GHz Double-Sequential Load-Modulated Balanced Amplifier with Reverse Adaptive Bias for Wideband Deep-Back-Off Efficiency Enhancement

G. Venturini, P. Reynaert
KU Leuven - MICAS, Leuven, Belgium

2:20 PM

4.3 A CMOS 63-to-81GHz VSWR-Resilient Load-Modulated Balanced Power Amplifier Co-Designed with Double-Quadrature Upconverter

S-H. Fu[1], Y. Zhang[1], Q. Liang[1], Z. Zhang[1], H-Y. Lai[2], P. Heydari[1]
[1]University of California, Irvine, CA
[2]University of California, Davis, CA

2:45 PM

4.4 A 45nm SOI-CMOS F-Band PA with Complementary Harmonic Cancellation Achieving 18.3dBm and 3.9W/mm²]

K. Q. Liang[1], S. Lepkowski[2], J. Moody[3]
[1]University of Maryland, Silver Spring, MD
[2]Sandia National Laboratories, Albuquerque, NM
[3]University of Maryland, College Park, MD

3:00 PM

4.5 A 13.7dBm OP1dB Four-Way Differential Combined D-Band Power Amplifier in 7nm FinFET

P-A. Fernandez, G. Venturini, P. Reynaert
KU Leuven ESAT-MICAS, Leuven, Belgium

Break 3:15 PM

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4.6 Diamond Signal Mapping for Improved Linearity and Reduced Complexity in Digital mm-Wave Transmitters

M. Mortazavi[1,2], M. Spirito[1], M. Babaie[1]
[1]Delft University of Technology, Delft, The Netherlands
[2]imec-Netherlands, Eindhoven, The Netherlands

4:00 PM

4.7 A 0.3-to-32GHz 4096-QAM RFDAC Supporting Two-Decade-Wide Software-Defined Radio

K. Zhao, J. Chen*, Y. Lu*, T. Liu, S. Chen, G. Liu, G. Wu, L. Huang, C. Shi, R. Zhang*
East China Normal University, Shanghai, China
*Equally Credited Authors (ECAs)

4:25 PM

4.8 An 89-to-156GHz 0.9-to-1.2V Phase Shifter Using Distributed Gain-State Interleaved Densification and Step-AM/Step-PM-Distortion-Minimized True-impedance-Invariant VGAs.

Z. Guo, W. Deng, H. Jia, B. Chi
Tsinghua University, Beijing, China

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4.9 A 6.8-to-39.4GHz Distributed Low-Noise Amplifier Using Multi-Branch Noise Cancellation and Inductor Folding

Z. Jiang, Z. Zhang*, Z. Wang*, Y. Qian, L. Huang, C. Shi, R. Zhang*
East China Normal University, Shanghai, China
*Equally Credited Authors (ECAs)

5:15 PM

4.10 A Quasi-Lossless E-M-Coupled Mode-Switching 24/38GHz Dual-Band LNA Achieving 47/65dBc Image Rejection and 3.3dB Noise Figure

J. Zhang[1,2], Q. Wang*[1,2], L. Wang[1,2], Q. Wu[1,2], Z. Yang[1,2], Y. Huang[1], Z. Chen[3], J. Zhang[1], X. Shan[1], K. Cheng[1], H. Ren[1], X. Guo[1,2], B. Li[1,2]*
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[2]University of Chinese Academy of Sciences, Beijing, China
[3]South China University of Technology, Guangzhou, China
*Equally Credited Authors (ECAs)

Conclusion 5:30 PM

Image Sensors and Ranging

Session Chair:

Sanshiro Shishido, *Panasonic Holdings Corporation, Osaka, Japan*

Session Co-Chair:

Min-Woong Seo, *Samsung Electronics, Hwaseong, Korea*

1:30 PM

5.1 A 3.2Mpixel Digital-Pixel Sensor with 1.62µm 3-layer Pixels for Pseudo-Global-Shutter Operation

J. Wu[1], R. Capoccia*[2], S. Chen[1], H. Manjunath[3], C. Zhai[4], W. Guo[4], A. Pujar[4], C. Desai[4], J. Schauer[4], S. Sharma[4], K. How[4], R. Wiser[4], R. Chilukuri[4], J. Ren[4], C. Liu[1], R. Ikeno[5], H. Abe[5], C-C. Wang[6], C-H. Lin[6]*

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[2]Meta, Zurich, Switzerland
[3]Meta, Burlingame, CA
[4]Meta, Sunnyvale, CA
[5]Brillnics, Tokyo, Japan
[6]Brillnics, Hsinchu, Taiwan
*Equally Credited Authors (ECAs)

1:55 PM

5.2 A 2-Stacked Synchronous EVS+Edge Hybrid CMOS Image Sensor with 3.85µm-Pitch Digital Pixels for DCG-HDR Imaging, Intra-Frame Event Sensing, and Edge Detection

Y. Luo[1], J. Li[2], S. Mirabbasi[2]

[1]vivo Mobile Communication, Shenzhen, China
[2]University of British Columbia, Vancouver, Canada

2:20 PM

5.3 A 320×256 131.2dB-DR Vertically Stacked Dual-QWIP LWIR-FPA with 8b Pixelwise DAC for In-Sensor Background Suppression HDR Imaging

H. Lu[1], Y. Zhuo[1], B. Yu[1], X. Du[1], X. Li[2], Y. Niu[3], X. Zhang[1], Y. Zhang[1], Z. Cheng[1], Y. Cai[1], W. Lu[2], W. Lu[1]

[1]Peking University, Beijing, China
[2]Shanghai Institute of Technical Physics Chinese Academy of Sciences, Shanghai, China
[3]Lingfeng Vision Chip Beijing Technology, Beijing, China

2:45 PM

5.4 Action-Recognition Vision System with Multi-Level Sparsity Solely Powered by a mm-Scale Solar Cell

Y. Zhao, A. Gupta, K. A. Ahmed, H. Okuhara, M. Alioto

National University of Singapore, Singapore, Singapore

Break 3:10 PM

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5.5 A 13.66pJ/(pixel·frame) 320×240 Processing-in-Sensor Pupil-Tracking Imager with Adaptive Binarization and Binary/ROI Readout

W-C. Chang, J. C. J. S. Marquez, G-C. Chen, R-S. Liu, M-F. Chang, K-T. Tang, C-C. Hsieh

National Tsing Hua University, Hsinchu, Taiwan

4:00 PM

5.6 A 16-Channel Attack-Adaptive dToF LiDAR SoC with a 3.1mW/ch Event-Driven AFE and Time/Amplitude Dual-Domain Fingerprinting

R. Nonaka[1], R. Matsuno*[1], S. Nagai*[1], S. Miyagi*[1], Y. Hayakawa[1], R. Suzuki[1], M. Murakami[1], S. Ando[1], W. Zhang[1], T. Kado[2], K. Yoshioka[1]*

[1]Keio University, Yokohama, Japan
[2]Sony Semiconductor Solutions, Atsugi, Japan
*Equally Credited Authors (ECAs)

4:25 PM

5.7 A Hierarchical Memory-Efficient Peak-Tracing SPAD Flash LiDAR Sensor with In-Pixel ROI-Histogram Encoding and Streamed Incremental Depth Decoding

S. Lin, Y. Wang, C. Zou, L. Liu, T. Zhao, R. P. Martins, M. Zhang

University of Macau, Macau, China

4:50 PM

5.8 A SPAD Image Sensor with Photon Arrival Time Encoding Achieving Dip-Free 54.4dB Peak SNR and 125dB Dynamic Range

D. Cho[1,2], H-S. Choi[1], S. Choi[1], Y. Na[1], S. Yang[1], M. Yang[1], Y. Youn[1], I. Park[3], J. Cheon[3,4], M-J. Lee[1], Y. Chae[1,3]

[1]Yonsei University, Seoul, Korea
[2]Samsung Semiconductor, Hwasung, Korea
[3]XO Semiconductor, Seoul, Korea
[4]Kumoh National Institute of Technology, Gumi, Korea

Conclusion 5:15 PM

Next-Generation Electrical and Optical Transceivers

Session Chair:
Tamer Ali, *Mediatek, Irvine, CA*

Session Co-Chair:
Peter Ossieur, *Imec, University of Ghent, Brugge, Belgium*

1:30 PM

6.1 A 318.75Gb/s-PAM8/212.5Gb/s-PAM4 DSP-Based Transceiver with 42.8dB/59.4dB Reach in 3nm FinFET

M. Abdullatif[1], H. Park*[2], A. Elshater*[2], S-H. Huang[3], A. Khashaba[2], A. Metawea[1], A. Atharav[2], M. Gohar[1], K. Salem[1], Q. Nehal[2], S. Kwon[2], A. Wanas[1], M. Deghadi[1], P. Yan[2], P. Khanna[2], V. Jolly[2], C-E. Liu[3], Y. Salah[1], S. Amer[1], M. Ramadan[1], H-T. Chien[3], Y-H. Chen[3], M. Kamal[1], E. Rafaat[1], A. Khaled[1], H. Ehab[1], M. Saad[1], M. Magdy[1], K. Tyagi[2], S. Abdelatif[1], N. Mohamed[1], A. Khaled[1], Y. Chun[2], M. Megahed[2], M. Fouad[1], J. Chen[2], J. Lee[2], E-H. Chen[3], M. Gandara[2], A. Essam[1], J-T. Chen[3], A. Salah[1], P-C. Liu[3], T. Ali[2]*

[1]MediaTek, Cairo, Egypt
[2]MediaTek, Irvine, CA
[3]MediaTek, Hsinchu, Taiwan
*Equally Credited Authors (ECAs)

1:55 PM

6.2 A 212.5-Gb/s Simultaneous Bidirectional DSP-Based PAM-4 Transceiver with 36-dB Self-interference Cancellation

Z. Xu[1], Y. Zhang*[1], J. Zhou[1], X. Chen[2], H. Chen[2], X. Hu[2], B. Duan[2], H. Guo[1], X. Lu[2], B. Luo[2], C. Chen[2], Z. Yang[2], Y. Chen[2], H. Xu[2], G. Jin[2], H. Wang[2], L. Zeng[2], M. Cai[2], H. Wang[2], Y. Yao[2], S-C. Lee[2], X. Gao[1]*

[1]Zhejiang University, Hangzhou, China
[2]Shanghai Formula Microelectronics, Shanghai, China
*Equally Credited Authors (ECAs)

2:20 PM

6.3 A 212.5Gb/s 2.18pJ/b DSP-Based PAM-4 Transceiver with 58dB Loss Compensation for AI Scale-out Interconnects in 4nm FinFET

C. Feng[1], J. Xie*[1], Z. Li[1], W. Yuan[1], Z. Yao[2], Y. Shen[2], H. Sun[2], S. Yi[2], X. Ding[2], X. Lu[2], K. Ouyang[2], Z. Long[2], Q. Pan[1]*

[1]Southern University of Science and Technology, Shenzhen, China
[2]Sanechips Technology, Shenzhen, China
*Equally Credited Authors (ECAs)

2:45 PM

6.4 A 200Gb/s/wire 2.48pJ/b Single-Ended PAM-4 Receiver with 32dB Loss Compensation in 12nm CMOS

Z. Wang[1], M. Zhong[1], J. Yang[1], Z. Feng[1], B. Ye[2], W. Gai[1,3]

[1]Peking University, Beijing, China
[2]East China Normal University, Shanghai, China
[3]Beijing Advanced Innovation Center for Integrated Circuits, Beijing, China

Break 3:10 PM

3:35 PM

6.5 A 0.75pJ/b 200Gb/s XSR PAM-4 Receiver with CTLE-Merged A-Demux and Low-Power 8-Phase Clock Path in 28nm CMOS

P. Cai, X. Li, R. Zhang, H. Wu, Q. Pan
SUSTECH, Shenzhen, China

3:50 PM

6.6 A 128Gb/s 0.244pJ/b 6-Tap Reflective Receiver FFE with Zero-Additional-Power Half-Line-Length Post-Taps in 28nm CMOS

H. Chung[1], C. Moon[2], J. Lee[1], S. Kim[1], B. Kim[1]
[1]Pohang University of Science and Technology, Pohang, Korea
[2]University of California, Berkeley, CA

4:05 PM

6.7 A 1.6Tb/s Coherent Optical Transceiver with 300GS/s RX and 250GS/s TX Achieving 55-fs RJ and > 110-GHz BW in 2nm CMOS

T. Dusatko[1], R. Nguyen[2], D. Cartina[1], S. Dallaire[3], W. Elhalwagy[3], M. Essawy[2], A. Fernandez[4], M. Hassanpourghadi[2], S. Ho[1], M. Honarparvar[3], H. Huynh[5], M. N. Khiarak[3], P. Le[6], P. Le[6], A. Mellati[2], K. D. Nguyen[6], P. Paro[2], R. A. Rasul[5], B. Reyes[4], N. Sanchez[4], F. Solis[4], T. Q. Tran[6], K. Tyshchenko[7], T-F. Wu[2], G. Hatcher[2], S. Jantzi[2], K. Chang[5]
[1]Marvell, Vancouver, BC, Canada; [2]Marvell, Irvine, CA
[3]Marvell, Ottawa, Canada; [4]Marvell, Cordoba, Argentina
[5]Marvell, Santa Clara, CA; [6]Marvell, Ho Chi Minh, Vietnam
[7]Marvell, Toronto, Canada

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6.8 An 8 × 50Gbps/Fiber DWDM Optical Link in a 3D-Stacked 7nm CMOS EIC/65nm PIC Technology

M. Raj[1], Z. Wang[1], A. Bekele[1], A. Chou[1], C. F. Poon[1], W. Zhang[1], Y. Cao[1], J. Kim[1], A. Chou[1], M. Li[1], Z. Mohammed[1], G. Saha[1], C. Xie[1], S. Daudlin[1], W. Lin[1], W. Fang[1], X. Chen[2], L. Chen[2], N. Narang[2], S. W. Lim[2], K. H. Tan[2], S. Chen[1], J. Im[1], P. Upadhyaya[1], Y. Frans[1]
[1]AMD, San Jose, CA
[2]AMD, Singapore, Singapore

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6.9 A 2×800-Gb/s 0.97-pJ/b Monolithic Silicon-Photonic DWDM PAM-4 Transceiver Achieving 200 Gb/s/λ in 45-nm CMOS SOI

Z. Ye[1], J. Jin*[1], Y. Lin*[1], Z. Sun*[1], M. He[1], Z. Zhou[1], D. Xu[1], W. Su[1], A. Xu[1], H. Wan[1], B. Hong[1], Q. Hu[1], H. Hu[2], J. Liu[2], M. Zhang#[1], Q. Ding[2], X. Bi#[1]*
[1]Huazhong University of Science and Technology, Wuhan, China
[2]Jiufengshan Laboratory, Wuhan, China
*Equally Credited Authors (ECAs)

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6.10 A 50Gb/s Burst-Mode Optical Transmitter Based on Directly Modulated DFB Laser with Dynamic Biasing and Reflection Cancellation for PON in 28nm CMOS

J. Li, Z. Zhou*, H. Wu, W. Wu, Z. Li, P. Cai, X. Luo, D. Zhan, R. Zhang, X. Cheng, W. Luo, Q. Pan*
Southern University of Science and Technology, Shenzhen, China
*Equally Credited Authors (ECAs)

Conclusion 5:35 PM

Hybrid and Switched-Capacitor Power Converters

Session Chair: ***Hanh-Phuc Le,*** *UCSD, La Jolla, CA*

Session Co-Chair: ***Serhii Zhak,*** *Renesas, Chandler, AZ*

1:30 PM

7.1 A Mains-Connected Series-Capacitor 7-Level 1-to-6 Outputs AC-DC Converter Achieving 1150mW/cm³ at 91.1% Efficiency and 2.5W Output

J. Shi[1,2], X. Xu[1,2], Y. Jiang[1,2], R. Martins[1], P-I. Mak[1]

[1]University of Macau, Macau, China
[2]UM Hetao IC Research Institute, Shenzhen, China

1:55 PM

7.2 A 100V-Input Single-ZVT-Branch 3-Level DSD Buck Converter with Adaptive Multiplexed Control for Quad-Switch ZVS Achieving 87% Peak Efficiency

K. Yuan[1], C. Ding*[1], J. Jiang[2], Y. Wu[3], K. N. Leung[4], X. Liu[1]*

[1]Chinese University of Hong Kong, Shenzhen, China
[2]Southern University of Science and Technology, Shenzhen, China
[3]Shenzhen Pengshen Technology, Shenzhen, China
[4]Chinese University of Hong Kong, Hong Kong, China
*Equally Credited Authors (ECAs)

2:20 PM

7.3 A Direct-Drive D-GaN Driver with a Compact 3-Level Inverting Boost Converter and Dual-Channel Current Balancing

P. Chu[1], S. Hua[1], H. Xu[1], Z. Chen[2], X. Zhang[2], H. Yu[3], Y. Gao[1]

[1]Southern University of Science and Technology, Shenzhen, China
[2]GaN Engine Technology Incorporation, Shenzhen, China
[3]Shenzhen Polytechnic University, Shenzhen, China

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7.4 A 4N-Cell Scalable Li-Ion Battery Cell-Equalizer-Integrated Buck Converter with Modular Configuration

S-J. Lee, J-H. Kim, M-H. Kim, S-U. Shin

Pohang University of Science and Technology, Pohang, Korea

Break 3:10 PM

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7.5 A 92.4%-Peak-Efficiency 2.5V-to-12V Resonant Charge Pump with Coupled On-Chip Magnetic Inductors for Mobile UFS NAND Flash Memories Achieving 96.8mW/mm² Power Density

M. Jeong[1], T. Park[1], H. Kim[1], S. Seo[1], M. Hwang[2], D. Lee[2], C. Kim[1]

[1]Korea University, Seoul, Korea
[2]SK hynix, Icheon, Korea

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7.6 A Fully Integrated 2.8-to-5V-Input AC-Coupled Dual-Path CSCR Inverting Converter for Negative Gate Bias of GaN PAs Achieving 5.35mW/mm² Power Density and 83% Peak Efficiency

M. Liang, Y. Mao, H. Xu, J. Xu, Z. Hong

Fudan University, Shanghai, China

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7.7 A Fully Integrated Multiphase-Interleaving CSCR SC Converter with 92.8% Output Ripple Reduction and 89% Peak Efficiency

D. Zhou, J. Tao, G. Cai

Hong Kong University of Science and Technology (Guangzhou), Guangzhou, China

4:45 PM

7.8 A 1.8V-Input Quad-Output Continuously-Scalable-Conversion-Ratio Switched-Capacitor DC-DC Converter with Independent Regulation Achieving 82.4% Peak Efficiency

Y. Yang[1], M. Huang[2], S. Du[1]

[1]Delft University of Technology, Delft, The Netherlands
[2]University of Macau, Macau, China

5:10 PM

7.9 A Fully Integrated 2.5-to-4.2V-Input Dual-5-Level-SC-Assisted Reconfigurable CSCR Converter Achieving 4× VCF-Step Multiplication and 89.4% Peak Efficiency

K. Lee, J. Kim, W. Jegal, J. Park, D. Seo, W. Shin, C. Jeong, M. Kim, M. Cho, Y. Lee

Sungkyunkwan University, Suwon, Korea

Conclusion 5:25 PM

Demonstration Session 1

This year, the Demonstration Session extending in selected regular papers, both Academic and Industrial, will take place on Monday February 15th, and Tuesday February 16th, from 5 pm until 7 pm in the Golden Gate Hall. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2027, as noted by the symbol **DS1**

List of papers to come.

List of papers to come.

Domain-Specific Accelerators and Processors

Session Chair:
Andreas Burg, *EPFL & RAAAM Memory Technologies, Lausanne, Switzerland*

Session Co-Chair:
Francesco Conti, *University of Bologna & Chips-IT, Bologna, Italy*

8:00 AM

8.1 A 6nm Processing-Near-Memory Accelerator with 1.22TB/s Bandwidth by 3D Stacking for On-Device LLM Inference

H. Liu[1], J. Dong[1], K. Song[2], X. Jing[3], Z. Zhang[4], S. Cao[3], Z. Sun[1], H. Shen[1], S. Liu[1], J. Liu[2], Y. Gu[1], Y. Zhu[1], M. Jia[1], S. Duan[1], C. Lin[2], S. Yin[1], L. Wang[1]
[1]Xiaomi, Shanghai, China
[2]Xiaomi, Shenzhen, China
[3]Xiaomi, Beijing, China
[4]Xiaomi, Xi'An, China

8:25 AM

8.2 A 2.5ms/Action 3D Two-DRAM-on-One-Logic Processor for Vision-Language-Action Applications

H. Wang[1], X. Yang[1], J. Wei[1], Z. Yue[1], Y. Su[1], H. Cheng[1], B. Li[2], H. Han[1], J. Gu[1], Y. Hu[1], Y. Wang[1], S. Yin[1]
[1]Tsinghua University, Beijing, China
[2]Xi'an JiaoTong University, Xian, China

8:50 AM

8.3 A 28nm 228–365μJ/Token LLM Processor Enabling Parallel Inference and KV-to-Weight Distillation-Based Test-Time Training

R. Guo, K. Jiang, F. Zhang, C. Jia, Z. Yang, Z. Yue, H. Han, Y. Wang, Y. Hu, S. Yin
Tsinghua University, Beijing, China

9:15 AM

8.4 LiteSeeker: A 48.7FPS CNN-SSM Multi-Object Video Perception Accelerator with Redundancy/Sparsity-Aware Execution and Cross-Model Orchestration

H. Cho, H. Kim, Y. Kim, S. Yang, A. Putra, C. Duong Manh, J-Y. Kim
KAIST, Daejeon, Korea

Break 9:40 AM

10:05 AM

8.5 A Hybrid-Bonded LogicFolding Flagship Mobile SoC with Full-Chip Intra-Module Partitioning

Y. Huang[1], L. Chen[2], T. He[3], Y. Liu[2], W. Cao[2], Y. Li[1], H. Wang[1], Y. Li[4], L. Sun[2], J. Zhu[3], S. Pang[3], P. Zhao[1], L. Zhang[1], S. He[2], J. Zhang[1], Q. Liu[2], C. Wang[2], B. Huang[2], Z. Liu[3], X. Liang[2], Y. Dong[1]

[1]Huawei Technologies, Beijing, China
[2]Huawei Technologies, Shanghai, China
[3]Huawei Technologies, Shenzhen, China
[4]Huawei Technologies, Chengdu, China

10:30 AM

8.6 MALAKOFEC: A 127.65Gb/s 17.0pJ/b GRAND-Based oFEC Decoder Using Logistic-Weight Extrinsic Computation for Optical Communication

L. D. Blanc, Y. Shen, J. Tapparel, C. T. Müller, A. Burg, W. Song

Ecole Polytechnique Fédérale de Lausanne, Lausanne, Switzerland

10:55 AM

8.7 A 3.01mW Wi-Fi ISAC Processor for Concurrent CSI-Based Localization and 802.11n Channel Estimation/Equalization

S. Yun, C. Lee, S. Kwon, J. Ahn, Y. Lee

KAIST, Daejeon, Korea

11:20 AM

8.8 A 1.14TOPS/W INT16-Dominant Sliding Residual Refresh FDM Processor Achieving FP32-Level Accuracy for PDE Solving

Y. Zhu[1], B. Duan*[1], J. Ma[1], J. Yang[1], X. Li[1], S. Wu[1], J. Zhang[1], Y. Wang[2], B. Yang[1], J. Zhu[1], A. Zhang[1], L. Liu[1]*

[1]Tsinghua University, Beijing, China
[2]RoadRunner Semiconductor, Shanghai, China
*Equally Credited Authors (ECAs)

11:45 AM

8.9 A 28nm 6.23TOPS/W Large-Scale Digital Multigrid PDE Processor with Halo-Reuse Memory and Folded Multi-Operator PEs

B. Duan[1], Y. Zhu*[1], J. Yang[1], X. Li[1], X. Zheng[1], C. Chen[1], Z. Yang[1], B. Yang[1], J. Zhu[1], Y. Wang[2], S. Chen[1], J. He[1], H. Jiang[1], A. Zhang[1], L. Liu[1]*

[1]Tsinghua University, Beijing, China
[2]RoadRunner Semiconductor, Shanghai, China
*Equally Credited Authors (ECAs)

Conclusion 12:00 PM

Power Management for AI & High-Performance Computing

Session Chair: ***Rinkle Jain,*** *Nvidia, Hillsboro, OR*

Session Co-Chair: ***Chris Schaef,*** *Microsoft, San Diego, CA*

8:00 AM

9.1 A Monolithic GaN and Si pMOS 12V-Input 4MHz Nested Dual-Path Converter Achieving 92% Peak Efficiency and 1107A/cm³ Current Density

P-H. Chen[1], S. Jha[1], H. Vora[2], S. Bader[2], P. Koirala[2], A. Vyatskikh[2], P. Golani[2], A. Zubair[2], M. Beumer[2], H. W. Then[2], H. Krishnamurthy[3], J. Yu[3], K. Ravichandran[3], H-P. Le[1]

[1]University of California, San Diego, CA
[2]Intel Foundry Technology Research, Hillsboro, OR
[3]Intel, Hillsboro, OR

8:25 AM

9.2 A Direct 48V-to-1V GaN Half-Bridge Converter with Offset-Free Mirrored-COT Control and 20dB EMI Reduction

J-H. Kim[1], J-M. Cho[1], S. Chung[2], S-W. Hong[2]

[1]Sogang University, Seoul, Korea
[2]Seoul National University, Seoul, Korea

8:50 AM

9.3 A 48V to 0.6-to-1.8V 600A Hybrid Zero-Bias-TLVR Converter with Coordinated Transient Control Achieving 92.8% Peak Efficiency and 53mV Undershoot for a 150-to-500A Load Step at 6.3A/ns

Q. Zhou[1,2], Y. Jiang[1,2], R. Martins[1], P-I. Mak[1,2]

[1]University of Macau, Macau, China
[2]UM Hetao IC Research Institute, Shenzhen, China

9:15 AM

9.4 A 48V-to-1V Stackable Switched-Capacitor Buck Hybrid Converter with Flexible Independent/Paralleled Outputs and All-On/-Off Transients

W. Yang[1,2], Z. Tong[3], Z. Song[1], X. Mao[2,4], Y. Lu[1]

[1]Tsinghua University, Beijing, China
[2]VD Technology, Chengdu, China
[3]Beihang University, Beijing, China
[4]University of Electronic Science and Technology of China, Chengdu, China

9:30 AM

9.5 A 3612A/in³ 48V-to-PoL Multilevel Quad-Path FIVR Chiplet with State-Dependent Phase Reconfiguration for VPD

J. Xu[1], Y. Yang[1], T. Zhang[1], Z. Deng[1], R. Gong[1], S. Guan[1], H. Zhang[1], H. Wang[1], R. Chen[1], J. Wei[2], W. Zhang[3], K. J. Chen[3], Y. Wang[1], X. Liu[1]

[1]Tsinghua University, Beijing, China
[2]Peking University, Beijing, China
[3]Hong Kong University of Science and Technology, Hongkong, China

Break 9:45 AM

10:05 AM

9.6 A 12V-to-1V Scalable Capacitive Charge-Equalization Converter with Intrinsic Transient Assist and Time-Gated Balancing

Y-C. Lee[1], Y-J. Jeon[2], C-H. Lee[1], S-W. Hong[2]
[1]Sogang University, Seoul, Korea
[2]Seoul National University, Seoul, Korea

10:30 AM

9.7 A Reliability-Enhanced 33A 3D-Stacked IVR Enabling Kiloampere-Class Power Delivery and 59W System-Power Reduction for AI Processors

Y. Wang, T. Li, W. Liao, X. Yang, Z. Liu, W. Song, X. Tian, C. Heng, L. Jia, H. Cheng, Z. Wang, W. Song, D. Li
Huawei Technologies, Shenzhen, China

10:55 AM

9.8 A Phase-Scalable LEAP Hybrid Converter with Inherent Current Balance and All-Inductor Transient Energization





Y. Wang, W. Sun, Y. Ji, J. Yuan, L. Cheng
University of Science and Technology of China, Hefei, China

11:20 AM

9.9 A Dual-Path DCM IVR with Heterogeneous Chiplet Integration Enabling 350µm-Thick Substrate-Embedded Vertical Power Delivery

S. Jha[1], P-H. Chen[1], E. Lee[1], T. Wakaoka[2], C. W. LIM[2], S. M. CHO[2], T. Kushima[2], R. Morishita[2], S. Yamaguchi[2], D. M. Giuliano[3], H-P. Le[1]
[1]University of California, San Diego, CA
[2]Murata Manufacturing, Yasu, Japan
[3]pSemi Corporation, Burlington, MA

11:35 AM

9.10 A 5MHz 40A DrGaN Buck with Dual-Edge Predictive Dead-Time Control Achieving 0.47ns/0.1ns and Three-Cycle Fast Settling

Z-Y. Lin, X. Ming, Y. Lu, Z-H. Liu, C-W. Zhuang, B. Zhang
University of Electronic Science and Technology of China, Chengdu, China

11:50 AM

9.11 A High-Frequency Direct 3V-to-1V Oscillator-Rectifier-Based PoL Converter with Cycle-by-Cycle Regulation for Fast Transient Response

J. Yang, H. Song, Z. Liu, R. Martins, M. Huang
University of Macau, Macau, China

Conclusion 12:05 PM

High-Resolution Noise-Shaping ADCs

Session Chair:
Lucien Breems, *NXP Semiconductors, Eindhoven, The Netherlands*

Session Co-Chair:
Frank van der Goes, *Broadcom, Bunnik, The Netherlands*

8:00 AM

10.1 A Rail-to-Rail Buffer-Integrated Noise-Shaping Pipelined-SAR ADC Achieving 103.9dB SFDR with Floating-Supply Sampler

H. Wang, X. He, Y. He, Y. Gao, Y. Zhong, L. Jie, N. Sun

Tsinghua University, Beijing, China

8:25 AM

10.2 A 92dB-SNDR Buffer-Embedded Noise-Shaping Pipelined-SAR ADC with a Floating Folded-Cascode Dynamic Amplifier and Mixed-Mode MES

K. Li[1], Y-H. Shih[1], D. S. Kang[1], Y. Hao[2], A. J. Prakash[1], A. Li[1], X. Lin[1], O. C. Wu[1], X. Zhang[1], T-H. Wang[1], B. Liu[2], S. Li[1]

[1]Georgia Institute of Technology, Atlanta, GA
[2]University of Glasgow, Glasgow, United Kingdom

8:50 AM

10.3 A High-Pass-Filtering CT ΔΣM with 80.5dB Blocker-DR and 4.7nV/√Hz Noise over 100MHz Bandwidth for FMCW Radar

Z. Zhu[1,2], M. Ganzerli[2], S. Javvaji[2], R. Rutten[2], Q. Liu[2], B. Burdiek[2], S. Bajoria[2], G. Radulov[1], P. Harpe[1], L. Breems[2,3]

[1]Eindhoven University of Technology, Eindhoven, The Netherlands
[2]NXP Semiconductors, Eindhoven, The Netherlands
[3]Delft University of Technology, Delft, The Netherlands

9:15 AM

10.4 A 112.4dB-SFDR 32kHz-BW ΔΣM with a Mismatch-Free 6-bit Time-DAC

E. Miotello[1,2], A. Sukumaran[1], A. Fernandez Schrunder[1], Ö. Urhan[1,2], T. Jang[2], S. Emery[1]

[1]CSEM, Zürich, Switzerland
[2]ETH Zürich, Zürich, Switzerland

9:30 AM

10.5 A 99.2dB-SNDR 150kHz-BW single-bit Continuous-Time ΔΣ ADC with PVT-Robust Virtual-Ground Switched DAC and Input-Independent-Switched Capacitive DAC

V. Garg, A. Jain, L. Pandey, P. Garg

STMicroelectronics, Greater Noida, India

Break 9:45 AM

Integrated CMOS Transceivers and Arrays above 100GHz

Session Chair:
Akshay Visweswaran, *Nokia Bell Labs, Murry Hills, NJ*
Session Co-Chair:
Jose-Luis Gonzalez-Jimenez, *CEA-Leti, Grenoble, France*

10:05 AM

11.1 A 110-to-170GHz Fully Integrated CMOS VNA Extension Chip with ≥124dB System Dynamic Range

Y. Ding[1], Z. Lin*[2], Y. Shen[1], J. Gao[1], L. Wang[1], L. You[1], S. Hu[1]*
[1]Southeast University, Nanjing, China
[2]Purple Mountain Laboratories, Nanjing, China
*Equally Credited Authors (ECAs)

10:30 AM

11.2 A Scalable 512-Element 140GHz Phased-Array Transmitter in 45nm RF SOI Achieving 61dBm $EIRP_{SAT}$

A. Davidson, H. Krishnaswamy
Columbia University, New York, NY

10:55 AM

11.3 A 140GHz 32-Element Highly Scalable Spatially-Fed Active Transmitarray Achieving 32.6dBm EIRP in 28nm CMOS

H. Zhu, Y. Wang, X. Feng, N. Xu, C. Jiang
Fudan University, Shanghai, China

11:20 AM

11.4 A 1THz 4-Element Phased-Array Transmitter in 65nm CMOS

B. LIU, L. Gao*, W. Ma, Z. Qu, Z. Sun, Z. Zheng, R. Tao, H. Dong, Y. Chang, D. Tang, Q. Meng, J. Chen, W. Hong*
Southeast University, Nanjing, China

Conclusion 11:45 AM

Wearable and Portable Biosensing

Session Chair: ***Phillip Nadeau,*** *Analog Devices, Cambridge, MA*

Session Co-Chair: ***Kaiyuan Yang,*** *Rice University, Houston, TX*

8:00 AM

12.1 A Saliva-Based Chronic Disease Screening SoC with Biomarker Interface and Analog Multimodal Fusion Classifier

Y. Kim[1], M. Song*[1], Y. J. Pyeon*[1], T. Kim[1], S. Lee[1], S. Park[1], H. Kim[2], J. Choi[3], Y. J. Lee[3], J. J. Kim[1,4]*

[1]Ulsan National Institute of Science and Technology, Ulsan, Korea
[2]SK hynix, Icheon, Korea
[3]Korea Institute of Science and Technology, Seoul, Korea
[4]Anvix Lab, Ulsan, Korea
*Equally Credited Authors (ECAs)

8:25 AM

12.2 A Zoom-in Compression Photoacoustic Imaging Receiver with PWM-Based True Time Delay and Matrix-Vector Multiplication ΔΣ ADC

H-C. Liao, S. Zhang, Y. Chen, L. Li, K. Yang

Rice University, Houston, TX

8:50 AM

12.3 A 6.3μW BCC-Based Gesture–Recognition Chip Achieving 94.69% Accuracy for 16 Hand Gestures

H. Dai, C. Han*, J. Fu, B. Zhao*

Zhejiang University, Hangzhou, China
*Equally Credited Authors (ECAs)

9:15 AM

12.4 ANP-ET: A 3.1kHz 7.72μJ/Inference Event-Driven Eye-Tracking Processor with Spatio-Temporal Sparse Inference for Early Detection of Dementia

Z. Jian[1], Z. Fang[1], H. Wang[1], H. Ren[2], R. Yu[1], X. Cao[2], Y. Yang[2], Z. Cheng[1], Y. Hua[1], C. Dai[1], Z. Wang[1], J. Zhang[1], N. Qiao[3], H. Chen[1]

[1]Tsinghua University, Beijing, China
[2]Hebei Medical University Third Hospital, Shijiazhuang, China
[3]SynSense, Chengdu, China

9:30 AM

12.5 A Wearable Ultrasonic Doppler–ToF ASIC with FFT-Free and Matched-Filtering-Free Readout for cNIBP Monitoring

Y. Han[1], H. Lu[1], L. Zhao[2], P. Tan[1], J. Y. Adebiyi[1], H. Tanaka[1], N. Lu[1], Y. Jia[1]

[1]University of Texas, Austin, TX
[2]Massachusetts Institute of Technology, Cambridge, MA

Break 9:45 AM

10:05 AM

12.6 A 140.5μW 99.8%-Accuracy 96.1dB-SNR BioZ IC for Real-Time Cell Analysis with On-Demand Push-Pull Excitation and Continuous-Time ΔΣ T-D Readout

J. Li[1], J. Chen[1], X. Zhang[2], P. Li[1], L. Zhang[1], N. Nayak[3], Y. Zou[4], X. Liang[3], H. Zhao[3], R. Weerasekera[1], X. Liu[5], R. Haqshenas[3], D. Jiang[3], M. Cryan[1], S. Ha[6], A. Demosthenous[3], E. Charbon[4], D. Pamunuwa[1]

[1]University of Bristol, Bristol, United Kingdom
[2]Imperial College London, London, United Kingdom
[3]University College London, London, United Kingdom
[4]Ecole Polytechnique Fédérale de Lausanne, Neuchâtel, Switzerland
[5]Fudan University, Shanghai, China
[6]New York University Abu Dhabi, Abu Dhabi, United Arab Emirates

10:30 AM

12.7 A 7.1nJ/measurement Phase-Referenced Direct-Polar-Extraction Impedance Measurement IC with Harmonic-Nulling Sampling

G. Choi[1], J. Lee*[1,2], J-Y. Sim[1]*

[1]Pohang University of Science and Technology, Pohang, Korea
[2]Samsung Electronics, Hwaseong, Korea
*Equally Credited Authors (ECAs)

10:55 AM

12.8 CHARM: A Multi-Layer, Sleep-Stage Reconfigurable Charge-Domain SoC for Stage- and Event-Triggered Theranostic Stimulation

Y. J. Pyeon[1], Y. Kim*[1], S. Lee*[1], S. Lee[1], S. Cho[1], J. Hwang[1], D. S. Keum[2], Y. G. Kim[2], H. E. Jeong[1,2], J. J. Kim[1,2]*

[1]Ulsan National Institute of Science and Technology, Ulsan, Korea
[2]Anvix Lab, Ulsan, Korea
*Equally Credited Authors (ECAs)

11:20 AM

12.9 A 0.6μm N-Type-Only IGZO ECG/EMG Readout FlexIC Integrating a 44.7dB CCIA and a 9.24b ENOB 140kS/s Power-Gated Asynchronous SAR ADC

C. Wang[1,2], Q. Lin[1,3], A. Spagnolo[1], M. Dandekar[2], M. Velazquez Lopez[1,2], H. Çeliker[1], H. Li[1], J. Segers[1], J. Genoe[1,2], N. Papadopoulos[1], K. Myny[1,2]

[1]imec, Leuven, Belgium
[2]KU Leuven, Leuven, Belgium
[3]*now at Fudan University, Shanghai, China

11:35 AM

12.10 A 3.94μW 1kHz-BW NS-SAR ExG Front-End with Segmented Mismatch Compensation and Hybrid-Order Input-Impedance Boosting

J. Lee, N. Gill, J. Han, R. Kim, J. Seo, T-H. Kim, K-H. Baek

Chung-Ang University, Seoul, Korea

Conclusion 11:50 AM

High-Performance Die-to-Die and Clock Generation

Session Chair:
Zeynep Toprak Deniz, *IBM Research, Yorktown Heights, NY*

Session Co-Chair:
Weixin Gai, *Peking University, Beijing, China*

8:00 AM

13.1 A 35Tb/s/mm 0.29pJ/bit 64Gb/s/wire Simultaneous Bidirectional Die-to-Die Interface Transceiver Supporting Independent Reference Clock

J. Guo[1], J. Ma[1], J. Deng[1], J. Chen[2], J. Gu[1], X. Zhang[1], Y. Wang[1], W. Zheng[3], A. Chowdhury[1], T. Tang[2], J. Lai[1], J. Ding[1], X. Liu[2], K. Chen[3], J. Tang[3], Q. Chen[3], H. Gong[2], X. Xiang[1], K. Wang[3], D. Liang[1], V. Wang[2], X. Yang[2], J. Chung[2], K. Yang[2], Z. Shang[2], O. Zhou[2], J. Xu[2], S. Liang[1], K. Ganesan[1], A. Hsu[2], M. Kashani[2], X. Sha[1], F. Khan[1], M. He[1], Y. Dong[1], J. Li[1], M. Lin[1], N. Sarhangnejad[2], H. Cong[2], W. Ismail[2], A. Emara[2], H. Mostafa[2], N. Soltani[2], T. Sandhu[2], J. Musayev[2], D. Shin[2], Y. Dawji[2], J. Guthrie[2], J. Liu[2], Y. Feng[2], M. Ramezani[2], Z. Lulec[2], F. Sun[2], J. Su[1], A. Huang[1], S. Sun[2], J. Fry[4], K. Xu[4], M. Wielgos[4], J. You[4], C. Cui[4], R. Qiu[4], X. Shi[4], Z. Xu[4], L. Wu[1], D. Amor[2], G. Li[2], X. Han[1], D. Storaska[4], W. Wang[1], F. Lyu[5], J. Su[1], C. Li[2], A. Gharbiya[2], H. Fang[1], A. Mostafa[1], H. Wang[1], K. Chang[1]

[1]Marvell, Santa Clara, CA
[2]Marvell, Toronto, Canada
[3]Marvell, Singapore, Singapore
[4]Marvell, Fishkill, NY
[5]Marvell, Irvine, CA

8:25 AM

13.2 A 64Gb/s Low-Swing UCIe-Compliant Interface Featuring Complementary Zero-Crossing Sampling and Pulse-Width-Modulation-Based DFE in A16 with Super Power Rail

Y-J. Huang, M-S. Lin, W-C. Chen, C-C. Tsai, Y-C. Chen, W-H. Huang, H-H. Kuo, N-C. Cheng, S-T. Lai, C-H. Wen, H-T. Ke, W-S. Lin, S-C. Yang, K-T. Chou, P-C. Chiou, J-R. Huang, G. V. Yadav, C-Y. Li, S. Li, K-H. Hsieh
TSMC, Hsinchu, Taiwan

8:50 AM

13.3 A 0.291-pJ/bit 50.4-Gb/s/wire Inverter-Based Internally AC-Coupled Simultaneous Bidirectional Transceiver for Short-Reach Die-to-Die Interfaces in 7-nm CMOS

Y. Nishi[1], X. Chen[1], S. G. Tell[2], B. Zimmer[1], G. Kalogerakis[1], W. J. Turner[1], S. Song[1], A. Rekhi[1], L. Xu[1], J. W. Poulton[2], W. J. Dally[1], C. T. Gray[2]

[1]Nvidia, Santa Clara, CA
[2]Nvidia, Durham, NC

9:15 AM

13.4 A 168-Gb/s/wire PAM-3 SBD Transceiver with Reflection, Crosstalk and Leakage Optimized for Standard and Advanced Channels

Q. Liu, Y. Nong, Y. Hui, L. Du, Y. Du
Nanjing University, Nanjing, China

Break 9:40 AM

10:05 AM

13.5 A 32-to-128Gb/s/wire 0.51pJ/bit 43×62μm²/Lane Simultaneous Bi-Directional Transceiver With Inverter-Based DFE and Per-Lane Clock-Deskew-Merged 4-Phase PLL for Die-to-Die Interfaces in 28nm CMOS

Y. Xiang, Y. Xiao, H. Yan, J. Liu, N. Wu, Z. Zhang, L. Liu

Institute of Semiconductors of the Chinese Academy of Sciences, Beijing, China

10:30 AM

13.6 A 28.8Tb/s/mm 100.8Gb/s/pin Data-Pattern-Robust Capacitively Driven PAM4 Transceiver over a 6mm Channel with All-Level AC/DC Magnitude-Alignment and Transition-Balanced Encoding

J. Lee, Y. Shin*, G. Lee*, J. Choi*

Seoul National University, Seoul, Korea

*Equally Credited Authors (ECAs)

10:55 AM

13.7 A 0.591pJ/bit 36.8Gb/s/wire 15mm-Channel-Length Simultaneous Bidirectional Transceiver for Long-Reach Die-to-Die interfaces in 7nm CMOS

X. Chen[1], Y. Nishi[1], S. G. Tell[2], B. Zimmer[1], G. Kalogerakis[1], L. Xu[1], W. J. Turner[1], S. Song[1], A. Rekhi[1], J. W. Poulton[2], W. J. Dally[1], C. T. Gray[2]

[1]Nvidia, Santa Clara, CA

[2]Nvidia, Durham, NC

11:20 AM

13.8 A 71.3fs Fractional-N Ring-Based PLL for 3D-Friendly 212.5Gb/s Wireline

J. Lin, Q. Li, G. Chen, Y. Wang, S. Peng, Y. Le, Y. Zheng, D. Peng, S. Du, D. Li

Huawei Technologies, Shenzhen, China

11:45 AM

13.9 An 18.9fs-RMS Nyquist-Band-Jitter 4-to-16GHz 16-Phase Clock Generator Using Symmetric Injection Locking

H. Zhu, Z. Wu, Y. Zhu, R. P. Martins, C-H. Chan, M. Zhang

University of Macau, Macau, China

Conclusion 12:00 PM

High-Performance Multi-Band Wireless Transceivers and Receivers

Session Chair: ***Alyssa Apsel,*** *Cornell University, Ithaca, NY*

Session Co-Chair: ***Julian Tham,*** *Infineon, San Jose, CA*

8:00 AM

14.1 A 0.4-to-7GHz Reconfigurable Receiver with LO-Synchronous Switched-Capacitor IIR Filters

L. Kong, N. Yan

Fudan University, Shanghai, China

8:25 AM

14.2 A Compact Digital-Intensive 2x2 Dual-Band Dual-Concurrent WiFi8 Transceiver Achieving -55dB EVM Floor in 6nm CMOS

C-Y. Yu[1], N. Egan[2], J. X. Wu[2], T. Fisher-Jeffes[2], W. Lee[3], J. Ko[3], N. Ramachandra[2], H-H. Chen[3], N. Baskaran[3], M. Nasrollahpour[2], C. Lo[2], T. Liang[1], H. Li[3], J-C. Hsueh[3], S-C. Hung[3], C-C. Hsiao[2], C. Chien[1], Y-H. Chang[1], A. Shabra[2], S. Ho[2], O. Shanaa[1]

[1]MediaTek, San Jose, CA
[2]MediaTek, Woburn, MA
[3]MediaTek, Austin, TX

8:50 AM

14.3 A 5nm CMOS 16-to-20GS/s RF Sampling Data-Converters-Based 8-Channel Wireless Transceiver for TDD/FDD 5G and Beyond Base Stations

Y. Liu[1], F. Van der Goes[2], M. Mehrpoo[2], X. Yang[1], A. Garg[1], A. Elkholy[1], V. Milirud[1], J. Mulder[2], X. Yang[1], D. Kong[1], S. Wang[2], G. Li[1], J. Riley[2], W. Zhang[1], X. Meng[1], X. Li[1], H. Hatamkhani[1], D. Kim[1], J. Liu[1], K. Kankipati[3], H. Jiang[1], J. Westra[2], A. Momtaz[1], J. Cao[1]

[1]Broadcom, Irvine, CA
[2]Broadcom, Bunnik, The Netherlands
[3]Broadcom, San Jose, CA

9:15 AM

14.4 A Full-Duplex Receiver with Hilbert-Transform Equalization and Voltage-Domain Self-Interference Cancellation Achieving 32.4dB SIC Across 300MHz BW

B. Chen[1,2], Z. Zong[2]

[1]Hong Kong University of Science and Technology, Hong Kong, China
[2]Hong Kong University of Science and Technology (Guangzhou), Guangzhou, China

Break 9:40 AM

Compute-in-Memory

Session Chair: ***Hidehiro (Ricky) Fujiwara,*** *TSMC, Hsinchu, Taiwan*

Session Co-Chair: ***Xueqing Li,*** *Tsinghua University, Beijing, China*

10:05 AM

15.1 A 2nm 119 TOPS/W–35 TFLOPS/W, 172 TOPS/mm²–47 TFLOPS/mm² Integer and Floating-Point Digital-CIM Compiler with Signed-Magnitude Look-Up Table Multiplier

H. Mori[1], J-M. Hung[1], W-C. Zhao[1], B. Crafton[2], B. Zhang[2], C-K. Chuang[1], H. Ishii[3], V. Joshi[4], X. Peng[2], C-Y. Kao[1], Y-Y. Liu[1], T. Hashizume[5], Y-H. Hsu[1], W-S. Khwa[1], H. Fujiwara[1], Y-D. Chih[1], Y-H. Chen[1], H-J. Liao[1], K. Akarvardar[2], M-F. Chang[1], T-Y. J. Chang[1]

[1]TSMC, Hsinchu, Taiwan; [2]TSMC, San Jose, CA; [3]TSMC, Osaka, Japan
[4]TSMC, Ottawa, Canada; [5]TSMC, Yokohama, Japan

10:30 AM

15.2 A 2.4TOPS 614GB/s 16GB LPDDR5X-PIM DRAM Featuring Multi-Function ALU/FPU and High Fault-Coverage Testability

T. Jeong, W. Han*, Y. W. Kim*, S. Lee, Y. Kim, S. Ji, Y. Paik, S. Kim, B. Kim, H-S. Yu, W. Kang, G. Park, S-H. Kwon, S. Lee, K. Sohn, S-J. Bae, Y-S. Sohn*
Samsung Electronics, Hwaseong, Korea, *Equally Credited Authors (ECAs)

10:55 AM

15.3 A 28nm 12.8TFLOPS/mm² Asymmetric-Precision-Floating-Point Compute-in-Memory Macro with Basis-Compressed-Dynamic-LUT and Saliency-Aware-Streaming-Alignment

Y. Yang[1,2], Y. Zhou[1,2], Y. Li[1], Y. Sun[1], Y. Du[1], Z. Liu[1], Y. Zhang[1], X. Wang[1,2], J. Xia[1], J. Chen[1], T. Jiao[1], Y. Tang[1], H. Ye[1,3], A. Guo[1], J. Yang[1,2], X. Si[1]

[1]Southeast University, Nanjing, China
[2]National Center of Technology Innovation for EDA, Nanjing, China
[3]Wenzhou University, Wenzhou, China

11:20 AM

15.4 A 22nm 72Mb 59.24–101.41 TFLOPS/W ECC-Capable Non-Linear-MLC RRAM CIM Macro for Neuro-Symbolic Reasoning

Y-K. Yeh[1], D-Q. You[1], Y-T. Shao[1], Y-H. Lin[1], C-F. Chang[1], Y-C. Chen[1], H-C. Chang[1], Y-H. Wang[1], C-Y. Weng[1], H-H. Hsu[1], J-C. Tien[1,2], T-W. Meng[1], T-H. Wen[3], Y-W. Chen[2], L. Liu[2], R-S. Liu[1], C-C. Hsieh[1], K-T. Tang[1], M-F. Chang[1,2]

[1]National Tsing Hua University, Hsinchu, Taiwan
[2]TSMC Corporate Research, Hsinchu, Taiwan
[3]TSMC Corporate Research, San Jose, CA

11:45 AM

15.5 3D-NAND-CIM: A Hybrid-Bonded 3D-NAND-Flash-based Analog In-Memory-Compute macro offering 4.8M weights/mm²

P. Narayanan[1], A. Vasilopoulos[2], G. W. Burr[1], M. Le Gallo[2], B. Filipiak[3], H. Castro[4], J. Binfet[5], J. Hirst[4], H. Utomo[6], K. Parekh[5], B. Bhushan[5], R. Venigalla[5], K. Kirby[5], U. Egger[2], J. Luquin[1], V. P. Jonnalagadda[2], A. Siampakos[7], T. Antonakopoulos[7], K. Hosokawa[8], M. Ishii[8], Y. Kohda[8], S. Munetoh[8], A. Singh[2], A. Friz[1], J. Buchel[2], I. Chalas[2], C. Mackin[1], A. Malhotra[1], A. Goda[9], D. Mills[4], G. Atwood[10], M. Helm[10], J. Burns[6], V. Narayanan[6], H. Tsai[1], A. Sebastian[2]

[1]IBM Research, San Jose, CA; [2]IBM Research, Zurich, Switzerland
[3]Micron Technology, Novi, MI; [4]Micron Technology, Folsom, CA
[5]Micron Technology, Boise, ID; [6]IBM Research, Yorktown Heights, NY
[7]University of Patras, Patras, Greece; [8]IBM Research, Tokyo, Japan
[9]Micron Technology, Tokyo, Japan; [10]Micron Technology, San Jose, CA

Conclusion 12:00 PM

Highlighted Chip Releases

Session Chair: ***Sid Das,*** *AMD, Cambridge, United Kingdom*

Session Co-Chair: ***Mahmut Sinangil,*** *Nvidia, Los Altos, CA*

1:30 PM

16.1 LPU: Preemptive Voltage and Clock-Period Scheduling for Supply-Transient Mitigation of a Deterministic Processor that achieves a record 3,431 output tokens/s on 100k-token input Gemma 4 31B

I. A. US[1], S. Raghavan[2]

[1]Nvidia, Williston, VT
[2]Nvidia, Santa Clara, CA

1:55 PM

16.2 ARM AGI agentic CPU

Author list to come.
ARM, Cambridge, United Kingdom

2:20 PM

16.3 MX1P: A 4nm CXL 3.2 Computational-Memory SoC with 3,072 RISC-V Cores and SSD-Backed Memory

J. Lee, K. Lee, K. Shin, J. Choi, S. Han, Y. Jo, T. Yeo, J. Yang, Y. Hwang, D. Baek, W. Moon, J. Park, T. Jung, G. H. Kim, S. Kwon, K. Jeon, H. Kim, G. Lee, K-J. Roh, Y. Kim, J. Lee, H. Jeong, G. Lee, D. Kim, J. Kim

XCENA, Seongnam, Korea

2:45 PM

16.4 MTIA 400 & 450: Multi-Chiplet AI Accelerators for Training and Inference at Scale

O. Wu, A. Bansal, J. Singh, Y. Chen, A. Narasimha, R. Agarwal, D. Jayaraman, K. Gandhi, B. Jakka, H. Dixit, N. Jagannathan, H. Aepala, A. S. Poojary, S. Jha, H. Reddy, B. Balasubramanian

Meta, Sunnyvale, CA

Break 3:10 PM

Physical AI and Robotics

Session Chair:

Jun Zhou, *University of Electronic Science and Technology of China, Chengdu, China*

Session Co-Chair:

Nathaniel Pinckney, *Nvidia, Austin, TX*

3:35 PM

17.1 DexMPC: A 12nm 30.9kHz Model-Predictive-Control Processor for Dexterous Hand Manipulation with Incremental KKT Solving and Speculative Parallel Line Search

J. Lu[1], C. Du[1], Y. Ma[1], Y. Lin[1], L. Wu[1], Y. Zhang[1], Z. Huang[1], K. Zhang[1], Z. Chen[1], K. Zhang[2], C. Chen[1], Q. Liu[1], X. Zeng[1], H. Zhu[1]

[1]Fudan University, Shanghai, China

[2]Sharpa, Shanghai, China

4:00 PM

17.2 WPU: A 130mW 23.6ms Real-Time Adaptive World-Model Processing Unit with Selective Imaginative Planning and Prediction-Aware Environmental Adaptation for Physical AI

J. Lee[1], S. Ha[1], Y. Moon[1], J. Choi[1], S. Kim[2], Y. Jeong[1], S. Jung[1], H-J. Yoo[1]

[1]KAIST, Daejeon, Korea

[2]Gwangju Institute of Science and Technology, Gwangju, Korea

4:25 PM

17.3 A 28nm 14.56μJ/Task Joint-Space Motion Planning Processor for Robotic Manipulators with NNS-Free Tree Expansion and Scoreboard-Driven Dynamic μOP Injection

J. Oh, B. Yoo, S. Jeon, J. Park, D. Jeon

Seoul National University, Seoul, Korea

4:50 PM

17.4 FlashGroot: A 14.6mJ/Action End-to-End Energy-Efficient VLA System-on-Chip with Action-Aware Inference Architecture for Reactive Mobile Physical Agents

J. Park, Y. Moon, S. Lee, H. Joo, M. Kim, C. Jeong, Y. Choi, W. Park, S. Kim, S. Song, S. Kim, Y. Kabylkassymov, H-J. Yoo

KAIST, Deajeon, Korea

Conclusion 5:15 PM

Ubiquitous Power Management

Session Chair:
Shusuke Kawai, *Toshiba, Kawasaki, Japan*

Session Co-Chair:
Tom Van Breussegem, *ICsense - TDK, Leuven, Belgium*

1:30 PM

18.1 A 83W Monolithic GaN 120/230V Off-Line Boost PFC with Fully-Integrated Closed-Loop Control Achieving 94.4% Peak Efficiency

N. Deneke, F. Matalewski, S. Kale, B. Wicht

Leibniz University Hannover, Hannover, Germany

1:55 PM

18.2 A SIBO Converter with Built-in Charge Sampler Achieving Continuous VOP Current, Unity Inductor-to-Load Current Ratio and RHPZ Elimination for AMOLED Display

Z. Tang, R. P. Martins, M. Huang

University of Macau, Macau, China

2:20 PM

18.3 A Single-Stage Motor Driver Merging Step-Down Conversion in Dexterous Robotic Hands with Motor-Inductance Reuse for Switched-Capacitor Soft Charging

S. Zhang[1], C. Tong[1], W. Yang[1], Z. Tong[2], Y. Lu[1]

[1]Tsinghua University, Beijing, China
[2]Beihang University, Beijing, China

2:45 PM

18.4 A Single-Inductor 3-in-1 Optical Power Supply Modulator with Integrated Frequency-Sweep Linearization and Bidirectional Temperature Regulation for FMCW LiDAR

W. Zhu[1], X. Sun[1], J. Tang[1], C. Huang[1,2]

[1]Iowa State University, Ames, IA
[2]University of Macau, Macau, China

Break 3:10 PM

3:35 PM

18.5 A Fully Integrated, Optically Powered, Isolated Switched-Capacitor Gate Driver with Forward-Mode Optical Communication and over 80% Optical-to-Gate Power Efficiency

J. Li, M. Klymenko, Y. Li, X. Wang, W. J. Scheideler, J. Liu, J. T. Stauth
Dartmouth College, Hanover, NH

4:00 PM

18.6 A Full-Duplex Isolated DC-DC Converter for Gate Drivers with 500mW Power Transfer at 45.2% Peak Efficiency and 79/10Mb/s Communication over a 79MHz Carrier

J. Lu, Q. Zhuang, Q. Li, B. Li, X. Yan, Y. Shi, H. Qiu
Nanjing University, Nanjing, China

4:25 PM

18.7 A 2.5A Scalable Analog Distributed LDO with Full-Spectrum SoC-Noise-Tolerant Hybrid Signaling and Dynamic Feedforward Gain Boosting

Y. Lee[1], M. Kim[1], H. Park[1], W. Jung[2], S. Yoo[2], J-H. Yang[2], H-G. Rhew[2], H-M. Lee[1]
[1]Korea University, Seoul, Korea
[2]Samsung Electronics, Yongin, Korea

4:50 PM

18.8 A 2.5-to-4.3V-Input 1-to-12V-Output Cascaded SIDO-Sigma Supply Modulator for 5G Symbol-Power Tracking

M. Shang, C. Chen, C. Bo, J. Yuan, X. Huang, L. Cheng
University of Science and Technology of China, Hefei, China

5:05 PM

18.9 A 10/5MHz Time-Domain Hysteretic Buck Converter With Cycle-by-Cycle Phase Reset and Multiphase Push-Pull Phase Chasing Achieving 64mV Undershoot for a 3A/3ns Load Step

Z. Shen[1,2], X. Zhang[1], H. Li[1], Y. Jiang[1,2], F. Zhang[3], R. Martins[1], P-I. Mak[1,2]
[1]University of Macau, Macau, China
[2]UM Hetao IC Research Institute, Shenzhen, China
[3]Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China

Conclusion 5:20 PM

Advanced PLLs and VCOs

Session Chair:
Dmytro Cherniak, *Marvell Technology, Santa Clara, CA*

Session Co-Chair:
Keigo Bunsen, *Sony Semiconductor Solutions Corporation, Atsugi, Japan*

1:30 PM

19.1 A 105fs$_{rms}$-Jitter and –247.6dB-FoM$_J$, 11.9-to-13.1GHz Ring-Oscillator-Based Fractional-*N* Frequency Synthesizer Using Power-Gating Injection-Locked Clock Multiplier and Multi-Error Calibration Engine

M. Chae, S. Jang*, S. Lee, J. Choi*
Seoul National University, Seoul, Korea
*Equally Credited Authors (ECAs)

1:55 PM

19.2 A 4.8-to-5.28GHz Digital PLL with a 96MHz Unbalanced Pierce Crystal Oscillator and Correlated-Double-Sampling Phase-Detector Achieving 17.4fs Jitter at 38.2mW Power

R. Moleri, D. Fagotti*, P. Salvi, D. Lodi Rizzini, G. R. Trotta, F. Osio, S. Gallucci, M. Rossoni, A. L. Lacaita, S. Levantino, S. M. Dartizio*
Politecnico di Milano, Milano, Italy
*Equally Credited Authors (ECAs)

2:20 PM

19.3 A 0.65-to-1V-V$_{DD}$ Fractional-N Variable-Slope SPLL with Configurable Constant Gain Loop Bandwidth and Linear Switch-Capacitor Array Achieving Sub-50fs$_{rms}$ Jitter, <-65dBc Fractional Spur, and <–275dB FoM$_N$

Y. Li, J. Liu, N. Wu, Z. Zhang, L. Liu
Institute of Semiconductors of the Chinese Academy of Sciences, Beijing, China

2:45 PM

19.4 A 10.0-to-13.7GHz Single-Core Series-Resonance VCO with LC-Ladder Resonator and Split-Inverter Core Achieving 31.2% TR and 203dBc/Hz FoM$_T$

Y. Chen, H. Guo
University of Science and Technology of China, Hefei, China

3:00 PM

19.5 Efficient and Power-Scalable Series-Parallel-Tank CMOS Class-E VCO with Phase Noise Down to –136.3dBc/Hz at 1MHz from 9GHz and 196.4dBc/Hz peak FoM

L. Piotto[1], K. Vural[2], A. Bilato[1], G. De Filippi[1], A. Mazzanti[1,2]
[1]Fondazione Chips-IT, Pavia, Italy
[2]University of Pavia, Pavia, Italy

Break 3:15 PM

3:35 PM

19.6 A 12nm 10.8-to-18.4GHz Fractional-N Hybrid Sampling PLL with <-61dBc Fractional Spurs Using Spread-Spectrum Modulation

Z. Xu, S. van der Ven, J. van den Heuvel, R. Li, M. Hashemipour-Nazari, M. Wanten, A. Kumar, P. Mateman, E. Allebes

imec-Netherlands, Eindhoven, The Netherlands

4:00 PM

19.7 A 0.021mm² Ring CP-PLL with Phase-Domain Dynamic Feedback Achieving –243.0dB FoM

M. Oveisi[1], S. Chae[2], P. Heydari[1]

[1]University of California, Irvine, CA
[2]Georgia Institute of Technology, Atlanta, GA

4:25 PM

19.8 A 14.5fs$_{rms}$ Jitter Noise-Cancelling PLL Featuring an On-Chip XO Driver with -176dBc/Hz Noise Floor and 3GV/s Slew Rate

Y. Liu, L. Liu, Z. Jing, Y. Du, Y. Liu, K. Kang, J. Gong

University of Electronic Science and Technology of China, Chengdu, China

4:50 PM

19.9 A 15.3-to-16.4GHz Series-Parallel-Resonance VCO with Common-Source-Based Negative Resistance Achieving 203.1dBc/Hz Worst-Case FoM$_A$

S. Kong, Q. Lin, Z. Huang

Hong Kong University of Science and Technology (Guangzhou), Guangzhou, China

5:05 PM

19.10 A Fully Connected Dual-Harmonic-Synchronized Octa-Core Oscillator in 65nm CMOS Achieving –160.6dBc/Hz Phase Noise at 10MHz Offset from a 9.27GHz Carrier

B. Jafari[1], A. Ghafari[2], A. Ghorbani Nejad[1], F. Mahmoudi[3], S. Mirabbasi[1], S. Shekhar[1]

[1]University of British Columbia, Vancouver, Canada
[2]Silicon Integrated, Eindhoven, The Netherlands
[3]TSMC, Austin, TX

5:20 PM

19.11 A 23.1-to-25.7GHz Current-Waveform-Shaping Series-Resonance VCO with Inductor-Sharing Technique Achieving 198.2dBc/Hz FoM

L. Chen, D. Ye

Huazhong University of Science and Technology, Wuhan, China

Conclusion 5:35 PM

Advanced Beamforming Techniques for Phased Arrays and Reflectarrays

Session Chair:
Konstantinos Manetakis, *CSEM, Thalwil, Switzerland*
Session Co-Chair:
Atsushi Shirane, *Institute of Science Tokyo, Tokyo, Japan*

1:30 PM

20.1 A 240GHz 0.9°-Needle-Beam-Steering Reflectarray with Modularized Packaging and 400 CMOS Chiplets

X. Chen[1], G. C. Dogiamis[2,3], B. Huang[1], S. F. Nagle[1], E. Lee[1], K. Pochana[1], S. Chintapally[1], R. Han[1]

[1]Massachusetts Institute of Technology, Cambridge, MA
[2]Intel, Chandler, AZ
[3]Deca Technologies, Tempe, AZ

1:55 PM

20.2 Active RF Dichroic Mirror: A 7.75-to-16GHz Frequency-Selective Relay Array with Autonomous Beam Tracking

H. E. Ge, H. Jia, W. Deng, B. Chi

Tsinghua University, Beijing, China

2:20 PM

20.3 A 40nm 17-to-32GHz 4-Beam 8-Channel Bidirectional Beamformer Employing Reconfigurable Doherty PA and Wideband LNA

J. Gu[1], Z. Wang[1], J. Sun[1], K. Hu[1], Z. Luo[1], L. Kong[1], X. Qi[2], Z. Xu[2], H. Xu[1,3], N. Yan[1,3]

[1]Fudan University, Shanghai, China
[2]Zhejiang University, Hangzhou, China
[3]Jiashan-Fudan Joint Research Institute, Jiashan, China

2:45 PM

20.4 A 0.54mm²/Path W-Band 16-Element Phased-Array Transceiver with Bidirectional Frequency Conversion for a 2D-Scalable AiP

F. Zhang[1,2], S. Jiang[3], D. Wang[1], H. Wan[1,4], C. Xu[1], W. Gao[1,4], N. Jiang[1], P. Yu[1,4], K. Guo[1,4], X. You[1,2,4], D. Zhao[1,2,4]

[1]Southeast University, Nanjing, China
[2]Peng Cheng Laboratory, Shenzhen, China
[3]Chengdu Xphased Technology, Chengdu, China
[4]Purple Mountain Laboratories, Nanjing, China

Break 3:10 PM

Amplifiers

Session Chair:
Edoardo Bonizzoni, *University of Pavia, Pavia, Italy*

Session Co-Chair:
Chuan-Hung Hsiao, *MediaTek, Hsinchu, Taiwan*

3:35 PM

21.1 A Low-Noise Wideband Floating Common-Gate TIA Front-End with a 1.04mW 1GS/s 8-bit Preamp-Reused Pipelined SAR ADC

Z. Chen, J. Li, L. Shen
Peking University, Beijing, China

4:00 PM

21.2 An Automotive LED Driver Using Area-Efficient Segmented HV Rail-to-Rail Voltage Sensing Technique with ±2.4mV Regulation Inaccuracy, 85ns Min Off-Time

J-J. Kuang[1,2], X. Ming[1], Z-H. Liu[1], S-T. Hu[1], Q. Su[2], X. Geng[2], B. Zhang[1]
[1]University of Electronic Science and Technology of China, ChengDu, China
[2]SouthChip Semiconductor Technology, ChengDu, China

4:25 PM

21.3 A Sensor Front-End with a >170dBΩ TIA and a 63dB-Extended Piecewise-Logarithmic Range up to 200°C

H. Siemssen[1], T. Stuckenberg[2], H. Borchardt[2], H. Vorwerk[1], R. Nowosielski[2], S. Jung[2], B. Wicht[1]
[1]Leibniz University Hannover, Hannover, Germany
[2]Baker Hughes, Celle, Germany

4:50 PM

21.4 An 8-Pin Isolated Amplifier/Modulator IC with Sub-0.5µs Overcurrent Detection Using Fast-Response Encoding and Signal Superposition

S. Oshita[1], H. Ishihara[2], T. Arai[1], M. Arai[1], T. Ogawa[1], T. Murasaki[1], M. Yamada[1], Y. Fukawa[1], S. Ootaka[1], O. Watanabe[1]
[1]Toshiba Electronic Devices & Storage, Kawasaki, Japan
[2]Toshiba, Kawasaki, Japan

5:05 PM

21.5 A 42V/60W+ Wireless PTx AFE with Integrated Full-Bridge and Lifetime-Guaranteed ±0.12%/±0.3% V/I Sensing

M. Sautto[1], F. Neri[1], J. Hennessy[1], S. Ipek[1], D. Pizzato[1], G. Mehas[2], M. Augustyniak[1], F. Di Fazio[1], G. Figliozzi[1], C. Martelli[1], A. Perkins[1], O. Tlaskal[3], H. Paz[4], W. Clement[5]
[1]Renesas Electronics, Zürich, Switzerland
[2]Renesas Electronics, San Jose, CA
[3]Renesas Electronics, Prague, Czech Republic
[4]Renesas Electronics, Chandler, AZ
[5]Renesas Electronics, Edinburgh, United Kingdom

Conclusion 5:20 PM

SRAM, HBM and DRAM

Session Chair:
Gunther Lehmann, *Infineon Technologies AG, Neubiberg, Germany*

Session Co-Chair:
Zheng Guo, *Intel, Portland, OR*

1:30 PM

22.1 SRAM Design in A14 Nanosheet Technology with Dual-Side Negative Bit-Line and Read Tracking Schemes for High-Density and Energy-Efficient Compute

J. Chang, Y-H. Chen, C-H. Hsieh, G. Chan, K-C. Lin, K-F. Lin, P-S. Wang, Y. Lin, S. Chen, M-H. Chang, P. Lin, C-W. Wu, C-Y. Lin, Y-H. Nien, H. Fujiwara, A. Katoch, R. Lee, H-J. Liao, C-Y. Lin, J-J. Liaw, S-Y. Wu

TSMC, Hsinchu, Taiwan

1:55 PM

22.2 A 40.1Mbit/mm² SRAM with Sub-I/O and Cross-Bank Redundancy for Arm DSU in 2nm GAA Technology

R. Mathur, A. W. Chen, V. V. Thakre, S. Aggarwal, S. S. Zond, N. G. Yuva, S. Padmanabhan, B. Maiti, S. Thyagarajan, Y. Chong

ARM, Austin, TX

2:20 PM

22.3 A 0.0288 µm² Bitcell, 22.48 Mbit/mm² Energy and Area Efficient Logic-Based 1-Read and 1-Write 2-Port 7T SRAM in 2nm Nanosheet Technology

M. Hamada[1], Y-H. Nien[2], M. Yabuuchi[3], K. Mizutani[1], Y. Ishii[1], K. Nii[1], H. Fujiwara[2], S-H. Hsu[2], P-E. Lin[2], Y-H. Chen[2], H-J. Liao[2], Y. Wang[2], F-M. Chang[2], L-J. Hung[2], P-W. Wang[2], T-Y. J. Chang[2], G. Yeap[2]

[1]TSMC Design Technology Japan, Yokohama, Japan
[2]TSMC, Hsinchu, Taiwan
[3]TSMC Design Technology Japan, Yokohama, Taiwan

2:45 PM

22.4 An Asymmetric-Leakage 4T eDRAM with Block-Level Leakage Self-Compensation Hold and Preemptive-Regeneration Dual-SA Read Schemes

T. Huang, R. Run, Y. Hu, D. Wu, J. Xu, G. Li, L. Pan, X. Xie

Tsinghua University, Beijing, China

Break 3:10 PM

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22.5 A 48GB 17Gb/s/pin HBM4E with I/O Eye Monitor and Voltage Droop Detection for On-Wafer SI/PI Integrity DFT

J-H. Kang, J. Jung, K. Kim, H. S. Jeong, G. Kim, H. Shim, Y. Kim, J. Jang, S-Y. Kim, H. Lee, C. Bae, Y-C. Kwon, B. Min, S. Ahn, A. Choi, J. Hwang, J. Lee, S. Baek, Y. G. Song, J-S. Lee, D. Lim, K-S. Ha, Y-S. Sohn, S. Hwang

Samsung Electronics, Hwaseong, Korea

4:00 PM

22.6 A 64-Channel 4096-DQ Custom HBM with Memory Controllers and 5-Layer Wafer-on-Wafer Hybrid Bonding

W. Zhang, Z. Wang, T. Huang, R. Liu, S. Zhang, J. Xia, H. Liao

Huawei Technologies, Shenzhen, China

4:25 PM

22.7 A 4nm All-Digital 3D-DRAM PHY With Direct Core Die Access Enabling Custom HBM Platforms

K. Chae, G. Kim, N. Kim, S. Yi, D. Kim, B. Koo, B. Rhew

Samsung Electronics, Youngin, Korea

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22.8 A 32-Gb 9.2-Gb/s/pin DDR5 SDRAM Fabricated with Vertical-Surrounding-Gate-Transistor and Wafer-on-Wafer Hybrid Copper Bonding Technology

Y. Tang, K. Cao, Y. Gu, M. Huang, F. Deng, G. Du, H. Li, Y. Zhu

Changxin Memory Technologies, Hefei, China

5:15 PM

22.9 A 16Gb DDR5 DRAM with Vertical-Gate Cell Transistor and Peripheral-on-Cell Architecture Using Wafer-to-Wafer Fusion Bonding and Deep Silicon Via Technology

J. Cheon, D. Lee*, J. Lee, S. Kim, H. Lee, H. Em, J. Lee, C. Jeong, T. Kwon, S. Kang, T. Kim, M. Park, M. Hwang, J. Ahn, H. Yim, S. Jeong, H. Won, Y. Kim, C. Lee, J. Kim, S. Lim, J. Kim, W. Kim, J. Hwang, H. Kim, J. Kim*

SK hynix, Icheon, Korea

*Equally Credited Authors (ECAs)

Conclusion 5:30 PM

Optics at the Edge

Session Chair: ***Giorgio Ferrari,*** *Politecnico di Milano, Milano, Italy*

Session Co-Chair: ***Filip Tavernier,*** *KU Leuven, Leuven, Belgium*

1:30 PM

23.1 OP-CIM: A 28nm 55fJ/bit, 204Gbps, 20.5TOPS/W Optically Programmable Compute-in-Memory Macro with Fused Optical Reception, SRAM, and Computation

Y. He[1,1], S. Kim[2], D. Y. Lim[1], S. Park[1], X. Hu[1], B-S. Kim[2], H. Mun[1], K. Lee[2], J-S. Seo[1]

[1]Cornell University, New York, NY
[2]University of Virginia, Charlottesville, VA

1:55 PM

23.2 A Monolithic 105dB·Hz$^{2/3}$-SFDR 190mW mm-Wave Analog Radio-over-Fiber Silicon Photonics Uplink Transmitter with Optoelectronic Feedback Linearization

J. Ke[1], J. Fang[1], S. Aniruddhan[2], S. Shekhar[1]

[1]University of British Columbia, Vancouver, Canada
[2]Indian Institute of Technology Madras, Chennai, India

2:20 PM

23.3 A 90-to-180-GHz CMOS LNPA-TFLN Co-Packaged Front-End Achieving 200-Gb/s Sub-THz-to-Optical Conversion

D. Tang[1], Y. Zhang*[2], L. Yang*[2], Z. Wang*[1], Q. Meng[1], Y. Guo[2], T. Long[3], P. Zhou[1], H. Shu[2], B. Chen[3], Z. Chen[1], J. Chen[1], H. Gao[1], T. Siriburanon[4], R. B. Staszewski[4], X. Wang[2], W. Hong[1]*

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[2]Peking University, Beijing, China
[3]ShanghaiTech University, Shanghai, China
[4]University College Dublin, Dublin, Ireland
*Equally Credited Authors (ECAs)

2:45 PM

23.4 A CMOS Phasor-FLIM Readout with Harmonic Rejection and Photon-Rate Adaptive Integration

K. R. Dandavate, Y. Yin, J. Yang, J. E. Sorrells, Y. Fan

Washington University in St. Louis, St. Louis, MO

3:00 PM

23.5 A 1024-Element Monolithically Integrated 2D Optical Phased Array and Driver ASIC in 45nm CMOS

D. Kramnik, J. Matres, H. Gehring, S. Bilodeau, M. de Cea Falco, B. Zhang, O. Cierny, G. Allen, M. Caverley, J-L. Plateau, D. Brinkley, T. Barwicz

Taara Connect, Sunnyvale, CA

Break 3:15 PM

Low-Power Radio and Techniques

Session Chair: ***Kuo-Ken Huang,*** *Everactive, San Jose, CA*
Session Co-Chair: ***Zhiwei Xu,*** *Zhejiang University, Hangzhou, China*

3:35 PM

24.1 A 3.5Gb/s 65nm IR-UWB Transmitter with a Lock-Retentive Dual-Loop Burst-Mode PLL and Fast-Settling Switched-Resistor Damping

Y. Huang, Y. Cheng, M. Feng, X. Liu
University of Toronto, Toronto, Canada

4:00 PM

24.2 A 28.2%-Efficiency BLE Transmitter with a Sub-µs Frequency-Settling FLL and –49dBm-HD3 Harmonic-Shaping Class-D PA

J. Jung[1], S. Shin[1], B. Wang[1], E. Lee[1], M. Abdolrazzaghi[2], U. Guler[2], A. P. Chandrakasan[1]
[1]Massachusetts Institute of Technology, Cambridge, MA
[2]Worcester Polytechnic Institute, Worcester, MA

4:25 PM

24.3 A 37–to-42GHz 8-Path Mixer-First Receiver Using the 5th Clock Harmonic and 7.5% Duty-Cycle Clocks

S. Khademi Sharif Abad, M. S. Oude Alink, B. Nauta
University of Twente, Enschede, The Netherlands

4:50 PM

24.4 A 1-Port Transceiver Using a Switch-Type Bidirectional Amplifier for Deployable X-Band ISAC Reflectarray Antennas

S. Date, J. Sudo, Y. Takeda, Y. Narukiyo, S. Kato, M. Kikuchi, H. Hayashi, S. Yatabe, H. Sakamoto, T. Tomura, J. Mayeda, A. Shirane
Institute of Science Tokyo, Tokyo, Japan

5:15 PM

24.5 A 1.2km/1.2km Tag IC for 3GPP Rel-20 Ambient-IoT with 665µW Oversampling Phase-to-Digital-Converter-Based Receiver

Q. Sun[1], Y. Guo*[2], Y. Jiang[1], W. Wang[1], W. Rhee[3], H. Jiang[1]*
[1]Tsinghua University, Beijing, China
[2]Shanghai Jiao Tong University, Shanghai, China
[3]Sungkyunkwan University, Seoul, Korea
*Equally Credited Authors (ECAs)

Conclusion 5:30 PM

Demonstration Session 2

This year, the Demonstration Session extending in selected regular papers, both Academic and Industrial, will take place on Monday February 15th, and Tuesday February 16th, from 5 pm until 7 pm in the Golden Gate Hall. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2027, as noted by the symbol **DS2**

List of papers to come.

List of papers to come.

List of papers to come.

EE3:
ISSCC Ping-Pong Challenge 2027

Location

Salon 9 (Yerba Buena Ballroom), B2 Level, Marriott Marquis

Take a break from circuits, papers, and specifications, and join fellow ISSCC attendees for the inaugural **ISSCC Ping-Pong Challenge**. Whether you are a seasoned player or simply looking for a fun way to connect with colleagues from around the world, this friendly competition promises an evening of networking, camaraderie, and healthy rivalry.

The event is open to all conference attendees. Matches will be played in doubles, with randomly paired teams. Each participant will have the opportunity to play two matches. Players of all skill levels are welcome. The evening will include networking, refreshments, and informal play throughout the event.

The top 25 scoring players will receive an exclusive **ISSCC-branded ping-pong paddle**, along with bragging rights for the remainder of the conference.

The world's premier integrated-circuits conference meets one of the world's most popular engineering pastime traditions. Grab a paddle, meet new colleagues, and join the first-ever ISSCC Ping-Pong Challenge.

Registration

Participation is limited to the first **288 registered players.** Additional registrants will be placed on a waitlist and may be assigned to replace no-shows. Registration opens on Monday, February 15th, at 12pm through the Mirasmart platform for registered ISSCC attendees only.

Players are required to download the Scoreholio app on their phones (Android or iOS) and create a free player account using the same email address used for conference registration. The app is required at the event to check-in players, send notifications, track scores and replace no-shows with waitlisted players.

Attendees who do not wish to compete do not need to register and are welcome to stop by, socialize, and cheer on participants throughout the evening.

Additional event details, including tournament operations and scoring procedures, will be provided through the Mirasmart platform after registration.

Schedule

Monday, February 15th

12:00 PM – Player registration opens

Tuesday, February 16th

12:00 PM – Player registration closes
7:45 PM - 8:00 PM – Player check-in
8:00 PM - 9:30 PM – Tournament play
9:30 PM - 10:00 PM – Awards and closing

Compute-In-Memory-Centric SoCs and Domain-Specific Accelerators

Session Chair:

Bo (Angela) Wang, *Singapore University of Technology and Design, Singapore, Singapore*

Session Co-Chair:

Win-San Khwa, *TSMC, Hsinchu, Taiwan*

8:00 AM

25.1 A 2nm 30.6TOPS/W RISC-V AI Accelerator with Integrated Digital Compute-in-Memory

B. Crafton[1], B. Zhang*[1], A. Lele*[1], W-S. Khwa*[2], H. Mori[3], J-M. Hung[3], W-C. Zhao[3], P-S. Wu[2], V. Joshi[4], N. Dipto[4], P. Noel[4], Y. Shin[4], M. Gershoig[4], C-K. Chuang[3], H. Ishii[5], T. Hashizume[6], X. Peng[1], K. Torigoe[5], Y-Y. Liu[3], Y-H. Hsu[3], H. Fujiwara[3], Y-D. Chih[3], Y-H. Chen[3], H-J. Liao[3], K. Akarvardar[1], M-F. Chang[2], T-Y. J. Chang[3]*

[1]TSMC Corporate Research, San Jose, CA
[2]TSMC Corporate Research, Hsinchu, Taiwan
[3]TSMC Design Technology, Hsinchu, Taiwan
[4]TSMC Design Technology, Ottawa, ON, Canada
[5]TSMC Design Technology Japan, Osaka, Japan
[6]TSMC Design Technology Japan, Yokohama, Japan
*Equally Credited Authors (ECAs)

8:25 AM

25.2 A 3.52mJ/Word 9T-TSPC-FF-Based Synthesizable-CIM Accelerator with Quantization Group Reordering and Speculative Speech Generation



Q. Zhi, Q. Cheng, K. Jiang, T. Jia
Peking University, Beijing, China

8:50 AM

25.3 ARTOO: A 6.24Tokens/s/mW Physical-AI SoC with Agentic Planning and Markov-World-Constrained Autoregressive Action Decoding

L. Zheng[1], C-Y. Chin[1], Z. Wang[1], A. M. Bavani[1], P-S. Wu[2], B. Crafton[3], B. Zhang[3], Y-D. Chih[4], M-F. Chang[2], H. Li[1]

[1]Purdue University, West Lafayette, IN
[2]TSMC Corporate Research, Hsinchu, Taiwan
[3]TSMC Corporate Research, San Jose, CA
[4]TSMC Design Technology, Hsinchu, Taiwan

9:15 AM

25.4 A 281–486TOPS/W 22nm Weight-Memory-Free Hardwired Projection Fabric for LLM with 87.8% MAC-Operation Reduction

M. Iwata[1], Y. Nagahara[1], A. Hori[2], Y. Inoue[2], H. Otsuka[1], Y. Yamakawa[1], Y. Okoshi[1], T. Ishibashi[1], D. Fujiki[1], T. Kaneko[1], K. Ando[2], M. Motomura*[1]*

[1]Institute of Science Tokyo, Yokohama, Japan
[2]Hokkaido University, Sapporo, Japan
*Equally Credited Authors (ECAs)

Break 9:40 AM

Late Breaking Industry Highlights

Session Chair: ***Sid Das,*** *AMD, Cambridge, United Kingdom*
Session Co-Chair: ***Mahmut Sinangil,*** *Nvidia, Los Altos, CA*

10:05 AM
List of papers to come.

Ultra-Broadband and High-Speed ADCs

Session Chair: ***Seung-Tak Ryu,*** *KAIST, Daejeon, Korea*

Session Co-Chair:

Il-Min Yi, *Gwangju Institute of Science and Technology, Gwangju, Korea*

8:00 AM

27.1 A 100GHz RF Direct-Sampling ADC with RF-Coupled Transformer-Bootstrapped Sampler and Single-Channel 10GS/s Current-Domain Intra-Stage Pipelining

J. Dai, Y. Zhong, H. Wu, Y. Tao, J. Zhang, A. Zhang, Y. Wang, W. Chen, L. Jie, N. Sun

Tsinghua University, Beijing, China

8:25 AM

27.2 A 12b 40GS/s TI Pipeline-SAR ADC Achieving –158dBFS/Hz NSD and 25GHz Bandwidth in 16nm FinFET

Y. Zhang, M. Zhang, Z. Wu, Y. Zhu, R. P. Martins, C-H. Chan

University of Macau, Macau, China

8:50 AM

27.3 A Skew-Calibration-Free 6GS/s 12b Pipelined ADC with Reservoir-Assisted Rapid-Startup Sampler and FVF-Biased Amplifier

Y. Wang, M. Zhang, Y. Zhu, R. P. Martins, C-H. Chan

University of Macau, Macau, China

9:15 AM

27.4 A Single-Channel 8GS/s Pipelined ADC with Speculative Quantization

J. Zhang, Y. Zhong, Y. Tao, J. Dai, M. Gu, A. Zhang, Y. Wang, Q. Yang, L. Jie, N. Sun

Tsinghua University, Beijing, China

Break 9:40 AM

10:05 AM

27.5 A 14b 200MS/s Bidirectional Zero-Crossing-Based Pipelined-SAR ADC with Joint Background Calibration and Floating Current Source

B. Li, J. Yang*, J. Wang, Z. Kong, J. Wang, Y. Wang, X. Tang*
Peking University, Beijing, China
*Equally Credited Authors (ECAs)

10:30 AM

27.6 A 300MHz-BW 15.7mW C/DT Hybrid Pipelined-SAR ADC with a Complex-Pole Switched-Capacitor Filter



S. Huang, X. He, Y. He, H. Zhao, Y. Zhong, L. Jie
Tsinghua University, Beijing, China

10:55 AM

27.7 A 4.2-to-373K 3GS/s 7b Time-Domain ADC with Gated-Ring-Oscillator-Based DEM

K. Yamashita[1,2], K. Yoshioka[1], V. Issakov[2], H. Ishikuro[1]
[1]Keio University, Yokohama, Japan
[2]Technische Universität Braunschweig, Braunschweig, Germany

11:20 AM

27.8 A 174GS/s 7b Time-Interleaved SAR ADC with 90GHz Bandwidth

H. Luo, Z. Long*, D. Wang*, S. Wu, Y. Huang, G. Li, J. Luan, T. Feng, H. Heng, J. Liu, W. Liu, S. Chen, K. Ouyang*
Sanechips Technology, Shenzhen, China
*Equally Credited Authors (ECAs)

Conclusion 11:45 AM

Advanced Digital and RF Techniques for cm-Wave

Session Chair:
Danilo Manstretta, *University of Pavia, Pavia, Italy*

Session Co-Chair:
Jianjun Zhou, *Shanghai Jiao Tong University, Shanghai, China*

8:00 AM

28.1 A Diamond-Quantized 1-Bit Digital Transmitter for Autonomous Spec-to-GDS Generation

D. Li, Y. Zhang*, Z. Zhang, Y. Huang, D. Zhang, Z. Liu, M. Tang, D. Xu, Y. Xiong, W. Wang, H. Tanaka, K. Kunihiro, H. Sakai, K. Okada*

Institute of Science Tokyo, Tokyo, Japan
*Equally Credited Authors (ECAs)

8:25 AM

28.2 A 2.4GHz Nonuniform-Timing Digital PA with Sampling-Replica Spreading and Seven PBO Efficiency Peaks

Y. Liu[1,1], Y. Hu[1], P. Zhang[1], Y. Chen[1], Y. Chen[1], H. Chen[1], C. Yang[2], C. Deng[1], M-W. Chen[3], A. Zhang[1]

[1]Tsinghua University, Beijing, China
[2]d-Matrix, Santa Clara, CA
[3]University of Southern California, Los Angeles, CA

8:50 AM

28.3 A 5-Mode Switching Digital Polar PA with 3-Entry AM and 4-Entry PM Predistortion and Multi-Peak PBO Efficiency

D. Li, Y. Zhang, Z. Zhang, Y. Huang, D. Zhang, M. Tang, D. Xu, H. Tanaka, Z. Ren, Z. Liu, Y. Xiong, W. Wang, Y. Liu, H. Gu, T. Hu, K. Kunihiro, H. Sakai, K. Okada

Institute of Science Tokyo, Tokyo, Japan

9:15 AM

28.4 A Low-Cost 4-to-8GHz Watt-Level Time-Interleaved Doherty Quadrature Digital Power Amplifier with Fully Synchronous Switching Logic in 28nm Bulk CMOS

F. Xie, G. Zhang, Z. Zhao, H. Xu, Y. Yin

Fudan University, Shanghai, China

9:30 AM

28.5 A 12b 8× Oversampling Power-DAC/DTX Using Encoder-Interleaving, Enabling Controlled Fundamental, Baseband, and Harmonic Content

T. Ibrahim[1], D. Mul[1], A. Li[1], R. Bootsman[1], M. R. Beikmirza[2], C. Gao[1], M. Alavi[1], L. de Vreede[1]

[1]Delft University of Technology, Delft, The Netherlands
[2]Nokia Bell Labs, Stuttgart, Germany

Break 9:45 AM

10:05 AM

28.6 A 4-to-8GHz InP–CMOS Hybrid Pulsed Cryogenic LNA with a 50mV-Dropout RAPID-LDO Achieving Sub-1ns Wake-Up and <1mV VDD Droop for Qubit Readout

Y. Miao, Y. Peng, C. Liu, Z. Qin, C. Deng, R. P. Martins, P. I. Mak

University of Macau, Macau, China

10:30 AM

28.7 A Sub-3dB-Insertion-Loss Simultaneous Dual-Band Electrical Balance Duplexer with Reconfigurable TX/RX Loss Allocation

K. Shi[1], H. Darabi[2], A. R. Behzad[1]

[1]Broadcom, San Jose, CA
[2]Broadcom, Irvine, CA

10:55 AM

28.8 A Watt-Level VSWR-Resilient 25%/50% Dual-Duty-Cycle Doherty Quadrature Digital Transmitter for Ku-Band 6G FR3

L. Cao[1], J. Li[1], F. Xie[1], Z. Zhao[1], Y. Wei[1], X. Zhang[2], H. Xu[1], Y. Yin[1]

[1]Fudan University, Shanghai, China
[2]South China University of Technology, Guangzhou, China

11:20 AM

28.9 An ISN-Less Compact FR3 Doherty PA Using Single Metal Layer for Enhanced Average PAE and AM-PM

H. Yu[1], L. Liu[1], A. Dissanayake[2], K. Muhammad[3], W. L. Lien[4], C-M. Huang[2], S. Li[1]

[1]University of Texas, Austin, TX
[2]MediaTek, West Lafayette, IN
[3]MediaTek, Plano, TX
[4]MediaTek, Singapore, Singapore

11:45 AM

28.10 A Device–Package–Circuit Co-Designed 5V GaN-on-Si Doherty-Like Power Amplifier Fully Covering n77 and n79 Bands

C. Han[1,2], M. Pan*[3], H. Tao[1,2], F. You[3], M. Ma[1,2], X. Li[1], Y. Tang[1], X. Wang[3], R. Qin[3], C. Peng[1], H. Tang[1], X. Yu[1,2], Z. Xiao[3], Y. Fan[3]*

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[2]National Key Laboratory of Solid-State Microwave Devices and Circuits, Nanjing, China
[3]University of Electronic Science and Technology of China, Chengdu, China
*Equally Credited Authors (ECAs)

Conclusion 12:00 PM

SESSION 29

Advanced Systems for Neural Interfaces and Signal Processing

Session Chair: ***Xiaolin Yang,*** *imec, Leuven, Belgium*

Session Co-Chair: ***Hyung-Min Lee,*** *Korea University, Seoul, Korea*

8:00 AM

29.1 A 0.03mm² Chopping-Free PVT-Robust Oscillator-First ExG-to-Digital Frontend with Edge-Pursuit Operation Achieving 177.1dB-FoM$_S$, 10.8-NEF, and 0.9GΩ-Z$_{IN}$

X. Chen[1,2], A. D. Fernandez Schrunder[1], D. Keller[1,2], R. Ravanilla[1], V. Louzada Wisniewski[1], T. Jang[2], S. Emery[1], K. Badami[1]

[1]CSEM, Zürich, Switzerland

[2]ETH Zurich, Zurich, Switzerland

8:25 AM

29.2 A 16-Channel Stimulation-Artifact-Tolerant Neural-Recording IC with a 2.145V$_{pp}$ Input Range and 40ns Feedforward Latency for Closed-Loop Neuromodulation

Y. Zhu[1], Y. Dong[1], Z. Li[1], M. Yang[1], H. Liao[1], Z. Wang[1], L. Zhang[1], Y. Guo[2], Y. Chen[1], R. Wu[1], D. Ruan[1], L. Lin[1], J. Li[1]

[1]Southern University of Science and Technology, Shenzhen, China

[2]Xi'an University of Technology, Xi'an, China

8:50 AM

29.3 A Peripheral-Nerve Interface SoC with a 175× Power-Scalable Topology-Adaptive NS-SAR ADC for EIT-Guided Fascicle-Selective Interferential Stimulation

J. Ma[*1], H. You*[*1], M. Abdolrazzaghi*[*1], Y. Huang*[*1], J. Xu*[*1], M. Kanchwala[1], M. Ning[1], M. R. Horn[1,2], Y. Sun[1,2], N. Bruce[3], J. Olorocisimo[1], S. Wang[1], L. Bao[1], Y. Liu[1], L. Xu[1], S. Gong[1], E. Gu[1], W. C. Gani[1], M. Wagih[3], G. Eleftheriades[1], J. Zariffa[1,2], R. Genov[1]*

[1]University of Toronto, Toronto, Canada

[2]University Health Network, Toronto, Canada

[3]University of Glasgow, Glasgow, United Kingdom

*Equally Credited Authors (ECAs)

9:15 AM

29.4 An Online-Spike-Sorting Chip with Two-Stage Template-Matching and Drift Correction Achieving 0.00054mm²/Ch and 1.11μW/Ch

Y. Han, Y. Pan, M. Cui, P. Foster, S. Stathopoulos, T. Prodromakis, S. Wang

University of Edinburgh, Edinburgh, United Kingdom

Break 9:40 AM

10:05 AM

29.5 Forward-FLOW: A Forward-Only Label-Free Online-Learning Processor with Full-Weight Update for Multi-Application Long-Term Health Monitoring

J. Kim[1], H. Choee[1], V. Lukito[1], I-J. Chang[2], E. J. Choi[3], M. Je[1]

[1]KAIST, Daejeon, Korea
[2]Kyung Hee University, Yongin, Korea
[3]Ewha Womans University, Seoul, Korea

10:30 AM

29.6 A Miniaturized Ultrasound-Based Leadless Dual-Chamber Closed-Loop Pacing IC with 83.8% Peak Stimulation Efficiency and Bidirectional Communication

Y. Lan[*1], C. Gao*[*1], C. Zhang[2], Z. Wang[3], L. Zhang[1], Z. Wang[1], Y. Wu[3], Y. Li[1], L. Lin[1], Y. Lu[2], J. Li[1]*

[1]Southern University of Science and Technology, Shenzhen, China
[2]Peking University, Beijing, China
[3]Capital Medical University, Beijing, China
*Equally Credited Authors (ECAs)

10:55 AM

29.7 All-in-One Magnetoelectric Multimodal Wireless Power, Communication, and Localization System for a Network of Implants

N. Ahmed, H. Zhu, W. Kim, L. Ren, Y. Zou, Y. Chang, J. Robinson, K. Yang
Rice University, Houston, TX

11:20 AM

29.8 A 40.68MHz Single-Stage 10-Output Regulating Rectifier with Error-Based Control and a Phase-Adaptive Active Diode for DVS in Wirelessly Powered Retinal Stimulators

M-G. Jeong, J-H. Kim, S-J. Lee, Y-W. Jeong, M-J. Cho, M-H. Kim, G. Kim, D-C. Lee, I-H. Hur, E-J. Ko, M-S. Kim, S-U. Shin

Pohang University of Science and Technology, Pohang, Korea

11:35 AM

29.9 A 32-Channel 55μW Electrode-to-Stream EEG Recording IC Achieving 466mV$_{pp}$ Input Range and 84.2dB DR, with Array Crosstalk Undetected Down to –132.9dBc

S. Seo[1], S. Chon[1], T. Jeon[1], H. Han[1], Y. Gwon[2], S. Roh[2], C. K. Chung[2,3], J. Bae[4,5], Y. Chae[1,5]

[1]Yonsei University, Seoul, Korea
[2]Seoul National University, Seoul, Korea
[3]Korea Brain Research Institute, Daegu, Korea
[4]Kangwon National University, Chuncheon, Korea
[5]XO Semiconductor, Seoul, Korea

Conclusion 11:50 AM

3D NAND and RRAM Memories

Session Chair:

Vita Hu, *National Taiwan University, Taipei, Taiwan*

Session Co-Chair:

Luigi Pilolli, *Openchip & Software Technologies, Rome, Italy*

8:00 AM

30.1 A 375-Layer 1Tb 3b/Cell 3D-NAND Flash with 4.8 Gbps IO Speed and 60%-Improved-Energy-Efficiency

S. Choi, S. Chae, C. Jeong, B. Seo, D. Kim, J. W. Park, B-K. Kim, S. Han, H. Jeon, C. Park, M. Shin, H. Shin, Y. Noh, D. Kim, C. Park, I. Baek, J. Yoo, K. Jeong, K. Kim, C. Yang, S. Y. Choi, C. Koo, H. Lee, B. You, Y. Yoo, S. Lee, D. Choi, S. Yeo, S. Lee, J. Jang, J-Y. Lee, K. Ahn, S. An, C. Choi, J. Lee, S. Park, D. Youn, J. Lim, Y. Hong, S. Ok, W. Choi, H. Huh, B. Kim, S. Lee, K. Seol, W. Jeong, S. Y. Cha

SK hynix, Icheon, Korea

8:25 AM

30.2 A 128Gb SLC(1bit/cell) 3D Flash Memory with Selectable 8kB/4kB/1kB Page Sizes and 4.4M IOPS/W Energy Efficiency

T. Fujimoto[1], N. Abiko[1], Y. Harada[1], S. Kanazawa[1], Y. Koizumi[1], M. Dome[1], S. Nagasaka[1], H. Yoshihara[1], D. Nakamura[1], T. Midorikawa[1], M. Miakashi[1], S. Oketa[1], T. Suzuki[1], Y. Kajiyama[1], T. Fujimura[1], H. Takenaka[2], N. Kumazaki[1], M. Ito[1]

[1]KIOXIA, Tokyo, Japan
[2]KIOXIA Systems, Yokohama, Japan

8:50 AM

30.3 A 42Gb/mm2 5XX-Layer 1.5Tb 3b/Cell WF-Bonding 3D-NAND Flash with 290MB/s Write-Throughput and 6.8Gb/s/pin IOs

S. Park, M. Kim, N. Choi, J. Seo, S. Park, J. Kim, J-Y. Chun, C. Kim, Y. Cho, B. Cho, S. Choi, G. Kim, S. Ahn, C. Rho, J. Shin, M. Kim, S. Kim, J. Lee, S-H. Baek, K. Kang, J. Seo, S. Kim, K-H. Chung, J. Park, T-H. Kwon, S. Kim, M. Lee, M. Cho, M. Choi, Y. Jung, S. Lee, J-J. Park, D. Che, J. Park, C. Yoon, M. Kim, C. Lee, Y. Choi, J. Cho, I-H. Park, S. Lee, D. Kang, J. Lee

Samsung Electronics, Hwaseong, Korea

9:15 AM

30.4 A 2.5Tb 5b/Cell 240-Layer Floating-Gate 3D-NAND Flash Memory Featuring PLC-Enabled Layer-Count Efficiency and NAND–System Co-Design for a 31Gb/mm^2] Bit Density and Hyperscale SSD Deployment

S. Upadhyay, A. Rahman, A. Madraswala, B. Lokasani, B. Ngo, B. Cleereman, C. W. Ha, C. Sun, D. Ward, H. Tian, H. Chitturi, J. Shah, J. T. Park, K. Gaewsky, M. Lee, P. Zhang, R. Haque, R. Fastow, R. Ursua, R. Maguad, S. Uribe, S. Biyani, S. Park, Y. Wakchaure, J. Choi

Solidigm, Rancho Cordova, CA

9:30 AM

30.5 A 1Gb 15.5Mb/mm^2 1T4R RRAM in 28nm CMOS Technology with 15ns Read Speed, 10^6 Cycles Write Endurance and 10 Years Retention at 85°C

H. Yang[1], K. Zhou[*2], X. Tong[2], H. Jiang[2], Q. Zuo[3], X. Xu[4], J. Yang[1,2], Q. Liu[1], M. Liu[1]*

[1]Fudan University, Shanghai, China
[2]Zhangjiang Laboratory, Shanghai, China
[3]Bejing Memsilicon Technology, Shanghai, China
[4]Chinese Academy of Sciences, Beijing, China
*Equally Credited Authors (ECAs)

Break 9:45 AM

Hardware Security

Session Chair: ***Leibo Liu,*** *Tsinghua University, Beijing, China*

Session Co-Chair: ***Itamar Levi,*** *Bar-Ilan University, Lehavim, Israel*

10:05 AM

31.1 A 2.09GOPS/mm² 2-Logic + 4-DRAM Die 3D-Stacked Fully Homomorphic Encryption Processor for Database Private Information Retrieval

Z. Chen[1,2], Z. Li[2,3], Y. Lu[2,3], W. Zhang[2,3], Z. Zhang[1,2], Z. Li[2,3], Y. Wang[1,2], T. Guan[2,3], L. Huang[2,3], Y. Cai[2,3], Q. Zhang[2,3], Y. Gao[2,3], Z. Liu[2,3], H. Xu[1,2], B. Yang[2,3], D. Wu[1,2], T. Jiang[2,3], S. Liu[1,2], G. Dong[2,3], S. Zhang[2,3], B. Zhang[2,3], Y. Wu[1,2], S. Li[2,3], D. Niu[2,4], H. Zheng[2,3], J. Zhang[2,4]

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[2]Hupan Lab, Hangzhou, China
[3]DAMO Academy, Alibaba Group, Shanghai, China
[4]DAMO Academy, Alibaba Group, Hangzhou, China

10:30 AM

31.2 A 144.1kOPS Migration-Agile Classical/PQC Cryptographic-Processor with Multi-Algebraic Reconfiguration, Heterogeneous Operator Fabric and Inter-Packet Scheduling

Y. Zhu[1,2,3], W. Zhu[1,2,3], H. Hu[1,2,3], D. Han[1,2,3], X. Li[1,2,3], W. Yang[1,2,3], R. Wang[1,2,3], J. Yang[1,2,3], J. Sun[1], Y. Ouyang[1], C. Chen[1,2,3], J. Yang[4], B. Yang[1,2,3], H. Wang[1,2,3], M. Zhu[5], A. Zhang[1,2,3]

[1]School of Integrated Circuits, Tsinghua University, Beijing, China
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[3]BNRist, Tsinghua University, Beijing, China
[4]Wuxi Research Institute for Applied Technologies, Tsinghua University, Wuxi, China
[5]Wuxi Micro Innovation Integrated Circuit Design, Wuxi, China

10:55 AM

31.3 An All-Digital Multi-Modal Tamper Detector Exploiting Interconnect R-L-C and Cross-Die Response for Diverse Die-to-Die Links and Assemblies

S. Oruganti, C-P. Lo, A. A. Kedilaya, J. P. Kulkarni

University of Texas, Austin, TX

11:20 AM

31.4 A 1.012Gb/s Fully Synthesizable Jitter-Based TRNG with Time-Amplified Entropy Generation

Z. Ma[1,2], S. Wu[1,2], Y. Yang[1,2], B. Yang[1,2], L. Wang[1,2], M. Grujic[3], S. Su[3], Z. Yang[1,2], C. Deng[1,2], W. Zhu[1,2], H. Wang[1,2], J. Yang[4], M. Zhu[5], I. Verbauwhede[3], A. Zhang[1,2], L. Liu[1,2]

[1]Tsinghua University, Beijing, China

[2]Beijing National Research Center for Information Science and Technology (BNRist), State Key Laboratory of Cryptography and Digital Economy Security, Beijing, China

[3]KU Leuven, Leuven, Belgium

[4]Wuxi Research Institute for Applied Technologies, Tsinghua University, Wuxi, China

[5]Wuxi Micro Innovation Integrated Circuit Design, Wuxi, China

11:35 AM

31.5 A Fully Synthesizable Adjacent-Cycle Fault-Injection Attack Detector Using a Phase-Preserving Latch RO Without Runtime Boundary Retuning or Feedback Locking

J. Kim, D. Kim, Y. Lee

Sungkyunkwan University, Suwon, Korea

11:50 AM

31.6 LayoutSeal: Tamper-Evident Layout Filling to Thwart Malicious Modifications with <1% PPA Overhead

Y. Su, K. Yang

Rice University, Houston, TX

Conclusion 12:05 PM

Displays

Session Chair: ***Jong-Seok Kim,*** *Hanyang University, Ansan, Korea*

Session Co-Chair: ***Seunghoon Ko,*** *Kwangwoon University, Seoul, Korea*

8:00 AM

32.1 A Single-Chip Unified TSP/EMR Controller with Dual-Mode Metal-Mesh Electrodes for Digitizer-Less Stylus Sensing in AMOLED Displays

K. Park[*1], *M. Song*[*1], *H. Kim*[*1], *J. Kim*[2], *J. Kim*[1], *S. Lee*[1], *M. Jin*[1], *S. Jun*[1], *J. Park*[1], *J. Yoon*[1], *H. Lee*[1], *D. Kim*[1], *I. Kim*[1], *H. Woo*[1], *U. Kim*[1], *B. Kim*[1], *S. Kim*[1], *Y. Cho*[1], *S. Ko*[2]

[1]Hideep, Seongnam, Korea
[2]Kwangwoon University, Seoul, Korea
*Equally Credited Authors (ECAs)

8:25 AM

32.2 A 400ch 10b 1μs/line Self-Charging-Channel Source-Driver IC with Hot-Swap Auto-Zeroed Inter-Chip Gamma Referencing for 50μV (1σ) AVO in Multi-Chip Foldable Displays

Y. Park[1], *H-J. Kim*[1], *J-G. Lee*[1], *J. Kim*[2], *J-Y. Jeong*[2], *S. Yoo*[2], *H-S. Kim*[1]

[1]KAIST, Daejeon, Korea
[2]Samsung Electronics, Hwaseong, Korea

8:50 AM

32.3 A 12b Source-Driver IC with a Dual-DDA EMB-DAC Amplifier and Real-Time Offset and Linearity Calibration Achieving 1388μm²/Channel and 0.7mV DVO for High-Resolution OLED-on-Silicon Displays

D. Kim[1], *C. Bae*[1], *Y. Lee*[1], *S. Jeon*[1], *C. Kwon*[2], *D. Ha*[2], *J. Kim*[1]

[1]Hanyang University, Ansan, Korea
[2]Samsung Display, Yongin, Korea

9:15 AM

32.4 A 10b OLED Display Driver IC with Capacitance-Isolating, Difference-Extracting Relays (CIDERs) Achieving 12× Grayscale-Reference Power Reduction with 25% Shorter Worst-Case Input Delay

H-J. Kim[1], *Y. Park*[1], *S. Chae*[1], *J-G. Lee*[1], *B. Kim*[2], *S. Kuk*[2], *I. Kim*[2], *Y. Kim*[2], *S. Kim*[2], *H-S. Kim*[1]

[1]KAIST, Daejeon, Korea
[2]Samsung Electronics, Hwaseong, Korea

9:30 AM

32.5 A Per-Channel-Equalized Touch Readout IC Driving On-Cell 1000pF-Load OLED Panels at 909kHz with Baseline-Recovering Common-Current Subtraction Achieving 28.7dB SNR under 1-H Display Noise

J-Y. An[1], *J. Ahn*[1], *S. H. Choi*[1,2], *S-Y. Lee*[1], *Y-K. Choi*[3], *H-M. Lee*[1]

[1]Korea University, Seoul, Korea
[2]Samsung Electronics, Hwaseong, Korea
[3]SymbioDisplay Tech, Seoul, Korea

Break 9:45 AM

Optimization Accelerators

Session Chair:
Yoonmyung Lee, *Sungkyunkwan University, Suwon, Korea*

Session Co-Chair:
Jieun Park, *Samsung Electronics Foundry, Suwon, Korea*

10:05 AM

33.1 A 2-to-1024-State Fully Connected Potts Machine with Spin-Stationary KDF and State-Driven Active-Coefficient Access

X. Wang, Y. Lou, X. Chen, Y. Yang, Y. Su

Peking University, Shenzhen, China

10:30 AM

33.2 An 8K-Spin Ising Machine IC Supporting Native Interactions Up To Order 4096 with Limitless 4-Way Multi-Chip Scalability

J. Kim, J-Y. Sim

Pohang University of Science and Technology, Pohang, Korea

10:55 AM

33.3 LAGD: A 7nm 512MHz Dual-Core Ising SoC with Fully Connected Analog Feedback

J. Sun, T. Bettens*, S. De Weer, I. Ramirez-Lechuga, W. Vandesteene, T. Piessens, G. M. Sarda, W. Dehaene, M. Verhelst*

KU Leuven ESAT-MICAS, Leuven, Belgium

*Equally Credited Authors (ECAs)

11:20 AM

33.4 A 512-Spin GNN-Assisted Ising Machine with Unified Time-Domain RRAM-CIM and Arbitrary Graph Connectivity

J. Zhang, S. Wei, S. Pan, B. Cheng, Y. Su, X. Li, L. Pan, D. Wu, J. Tang, H. Qian, B. Gao, P. Yao, H. Wu

Tsinghua University, Beijing, China

11:45 AM

33.5 A Stochastic Analog 3-SAT Solver Using an Unsigned Crossbar and Push-Pull Clauses Achieving 21.26µs Mean Solution Time and 100% Solvability for 75-Variable Hard Problems in 12nm CMOS

M. Palaria[1], T-H. Hsu[1], T. T. Tanisha[1], H. Roy[1], Z. Ren[2], S. Su[2], W. Wu[1], M-W. Chen[1]*

[1]University of Southern California, Los Angeles, CA

[2]University of Waterloo, Waterloo, Canada

Conclusion 12:00 PM

Visual Computing Accelerators and Processors

Session Chair: ***Jun-Seok Park,*** *Seoul National University, Seoul, Korea*

Session Co-Chair: ***Tony Wu,*** *Google, San Jose, CA*

1:30 PM

34.1 A 1.44mm² 1.27mJ/Frame Display-Processing SoC with 240Hz High-Frame-Rate and Multi-Format HDR for Mobile Applications

T-M. Liu, K-M. Yang, D-J. Lin, C-W. Liang, J-Y. Yeh, P-H. Chiang, J-H. Chung, Y-C. Tseng, W-T. Huang, M-H. Wu, K-C. Huang, K-W. Chen, S-W. Hsieh, P-Y. Tsai, T-C. Chen, S-L. Wu, P-C. Yeh, C-J. Jan, C-I. Wu, H-J. Chu, X-L. Chen, N. Feng, Y-M. Yeh, M-E. D. Shih, H-J. Wei, Y-S. Liu, Y-C. Chang, C-C. Ju, Y-C. K. Jou

MediaTek, Hsinchu, Taiwan

1:55 PM

34.2 LYRA: A 3.5nJ/Point Streaming 4D Point-Cloud Transformer Processor with Spatial Registration and Incremental Inference

C. Zhou[1], Y. Ma*[1], W. Luo[1], X. Wang[1], Z. Li[2], Z. Guo[1], Y. Jiang[1], Z. Guo[2], Z. Gao[1], Y. Lin[1], H. He[1], A. Li[1], Y. Fu[1], S. Qiu[1], C. Zhang[1], Y. He[3], G. Li[1], Y. Yang[1,4], H. Jiao[1]*

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[2]Wuhan University, Wuhan, China
[3]Reconova Technologies, Xiamen, China
[4]Peking University, Beijing, China
*Equally Credited Authors (ECAs)

2:20 PM

34.3 A 7nm 285TOPS/W Universal Series-Based Point Cloud Processor for Cross-Scene 3D Perception

C-L. Chuang[1,2], Y-F. Shyu[1], C-H. Yang[1]

[1]National Taiwan University, Taipei, Taiwan
[2]MediaTek, Hsinchu, Taiwan

2:45 PM

34.4 A 2.48mJ/Frame Saliency-Aware Super-Resolution Processor Achieving 120FPS at 4K for Virtual-Reality Devices

X. Shi[1], J. Han[1], Z. Tang[1], Z. Yang[1], Y. Zhang[1], C. Fu[2], J. Han[1]

[1]Fudan University, Shanghai, China
[2]ShaoXin Laboratory, Shaoxing, China

Break 3:10 PM

3:35 PM

34.5 A 0.49mJ/Frame 4K-141fps Super-Resolution Accelerator with Content-Adaptive Residual Computing and Function-Reconfigurable Compute-in-Memory Architecture

T. Zheng, W-H. Yu, Y. Zhang, K-F. Un, J. Xu, R. P. Martins, P-I. Mak
University of Macau, Macau, China

3:50 PM

34.6 Fornax: A 16nm 16-Die Diffusion Processor with Fractal Recursion and Bit-Plane Folding for 8K Edge Image Generation

C. Zhou, Z. Guo, Z. Xu, E. Dai, Y. Zhong, G. Zhou, J. Zhang, J. Ku, H. Li, Y. Chen
Duke University, Durham, NC

4:15 PM

34.7 MAQAM: A 2nm 8.83mJ/Frame Mobile 512×512 Single-Step Diffusion Accelerator via K/V Bank Remapping for Conflict-Free Matmul and Adaptive Unified L1/L2 Memory

S-W. Hsieh, C-H. Yuan, Y-T. Liu, Y-T. Wu, P-Y. Tsai, M-H. Lin, C-Y. Cheng, L-F. Hsu, H-P. Chu, H-W. Chih, P-H. Chiang, C-M. Chang, M-T. Wu, Y-S. Chen, S-P. Kuo, C-K. Tseng, M-E. D. Shih, Y-C. Tseng, C-P. Chen, S. Chang, S. Huang, C-M. Wang, P-Y. Yeh, J. Liu, Y-C. Chang, C-C. Ju, Y. K. Jou
MediaTek, Hsinchu, Taiwan

4:40 PM

34.8 SUPRA: Attention-Guided Token-Skipping Diffusion LLM Accelerator with Mixed-Precision Parallel Self-Speculative Unmasking and Utilization-Aware Token Prefetching

Y. Tan[1,2], P. Dong[1,2], F. Tian[1,2], Y. Zhang[1,2], X. Liu[2], F. Li[2], P. Luo[2], L. Liang[2], K-T. Cheng[1,2]
[1]Hong Kong University of Science and Technology, Hong Kong, China
[2]AI Chip Center for Emerging Smart Systems, Hong Kong, China

5:05 PM

34.9 $Dollar: A Branch-Fused Diffusion Large Language Model Accelerator with Agent-Driven Psum-Aware Quantization and Multi-Precision Cache-PE

J. Zhou, Z. Zhu*, Z. Mu, L. Luo, T. Jia*
Peking University, Beijing, China
*Equally Credited Authors (ECAs)

5:20 PM

34.10 A 19.06TOPS/W 3D Structure-Driven Generation Accelerator with Geometry-Adaptive Computation and Adjacency-Inspired Reuse Dataflow

W. Yi[1], X. Feng[2], H. Ge[1], B. Pan[1], Y. Liu[2]*
[1]Beihang University, Beijing, China
[2]Tsinghua University, Beijing, China

Conclusion 5:35 PM

SESSION 35

Oscillators, Frequency and Voltage References

Session Chair:

Harijot Singh Bindra, *University of Twente, Enshcede, The Netherlands*

Session Co-Chair:

Yihan Zhang, *Hong Kong University of Science and Technology, Hong Kong, China*

1:30 PM

35.1 A 1.15mW 150MHz Inductor-Less Pulse-Injection 3rd-Overtone Crystal Oscillator Achieving 141µs Self-Startup Time and –262.9dB FOM$_J$ in 28nm CMOS

H. Li[1,2], Y. Wang[1], P-I. Mak[1], R. Martins[1], K-M. Lei[1]

[1]University of Macau, Macau, China
[2]UM Hetao IC Research Institute, Shenzhen, China

1:55 PM

35.2 A 26.3nW 32.768kHz TCXO Achieving ±4.4ppm Accuracy Using Injection-Based Frequency Correction and Digital Inhibition for Real-Time Clock Applications

P. Wang[*1], Y. Wang*[*1], H. Zhang[2], K. C. Li[1], L. Gu[1], Y. Cao[1], G. Dai[1], Y. Cheng[2], S. Pan[2], Y. Zhang[1]*

[1]Hong Kong University of Science and Technology, Hong Kong, China
[2]Tsinghua University, Beijing, China
*Equally Credited Authors (ECAs)

2:20 PM

35.3 A Temperature-Compensated Crystal Oscillator with Capacitance-Aware Varactor Control Achieving ±0.44ppm Inaccuracy and 45× Inaccuracy Improvement from -40°C to 85°C

Y. Cheng[1], H. Wang[1], X. Li[1], H. Zhang[1], P. Wang[2], Z. Li[1], X. Liu[1], M. Jiang[1], P. Yao[1], D. Wu[1], J. Tang[1], B. Gao[1], H. Qian[1], Y. Zhang[2], S. Pan[1], H. Wu[1]

[1]Tsinghua University, Beijing, China
[2]Hong Kong University of Science and Technology, Hong Kong, China

2:45 PM

35.4 A 200MHz 1.32mW Crystal Oscillator with Active Harmonic Canceler Achieving 27.6fs RMS Jitter and –153dBc/Hz Phase Noise at 10kHz Offset in 22nm CMOS

W. Chen[*1], J. Liu*[*1], R. B. Staszewski[2,3], Y. Hu[1]*

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[2]University College Dublin, Dublin, Ireland
[3]AGH University of Krakow, Kraków, Poland
*Equally Credited Authors (ECAs)

3:00 PM

35.5 An 8.65nW 32kHz TCXO with XO-Clock-Reused Temperature Sensing and Valley-Synchronized Load-Capacitance Switching

X. Wang[1], W. Huang[1], H. Li[1], Z. Yang[1], Z. Kong[1], J. Liu[1], X. Qian[1], X. Meng[2], J. Zhao[3], J. Li[1], L. Lin[1]

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[2]Hefei University of Technology, Hefei, China
[3]Shanghai Jiao Tong University, Shanghai, China

Break 3:15 PM

3:35 PM

35.6 A 395fJ/cycle 1b DFLL Employing Auto-Nulled Stochastic Chopping Achieving a <950ppb Allan Deviation

R. P. Burns, P. P. Mercier
University of California, San Diego, CA

4:00 PM

35.7 A 2.9ppm/°C 28MHz RC Frequency Reference from –40°C to 125°C with Gate-Leakage-Driven High-Order Temperature Compensation

W. Lv[1], P. Ren[1], D. Ye[1], K-M. Lei[2], L. Liao[1], Z. Chen[1]
[1]Hunan University, Changsha, China
[2]University of Macau, Macau, China

4:25 PM

35.8 A –40-to-165°C 0.6V 4nm 5T2R-Core VREF with 20.31ppm/°C TC and High-T Region Compensation

Y-T. Shih[1], L-J. Huang[1], K-H. Chen[1], Y-H. Lin[2], A-M. Lee[2], S-R. Lin[2]
[1]National Yang Ming Chiao Tung University, Hsinchu, Taiwan
[2]Realtek Semiconductor, Hsinchu, Taiwan

4:50 PM

35.9 A 0.9V 0.25pJ/Cycle 31.1ppm/°C Digital Frequency-Locked Loop Using Leakage-Free Time-Domain Resistive Trimming

D. S. Truesdell, A. Tanaka, Z. Gunn, J. Wang, B. H. Calhoun
University of Virginia, Charlottesville, VA

5:05 PM

35.10 A 690pW CMOS Cross-Biased Voltage Reference Achieving 15.2 ppm/°C from –50°C to 150°C and –88dB PSR at 10Hz

W-T. Chen[1], I-F. Lin[1], Y-H. Tung[1], W-W. Chen[2], T-H. Hung[2], Y-T. Liao[1]
[1]National Yang Ming Chiao Tung University, Hsinchu, Taiwan
[2]Novatek, Hsinchu, Taiwan

5:20 PM

35.11 A 2nm Dual-Loop Bandgap Reference with Decoupled BJT and Temperature-Compensated Current Paths

S. Wada[1], S. J. Huang[2], T. Matsuda[1], S-C. Tsao[2], Y-C. Peng[2], K-H. Hsieh[2]
[1]TSMC Design Technology Japan, Yokohama, Japan
[2]TSMC, Hsinchu, Taiwan

Conclusion 5:35 PM

Energy Harvesting, WPT and Piezo Actuators

Session Chair: ***Chen-Yen Ho,*** *MediaTek, Hsinchu, Taiwan*

Session Co-Chair: ***Hans Meyvaert,*** *Magics Technologies, Geel, Belgium*

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36.1 A One-Step 3.7-V_{DC} to 1k-V_{PP} Symmetric Bidirectional Pulser with Energy-Recovery and Multi-Parameter Tunability for Driving Microactuator Arrays

S. Han[1,2], Z. Tong[3], X. Wu[2], H. Jiang[2], T-L. Ren[2], C. Huang[1], Y. Lu[2]
[1]University of Macau, Macau, China
[2]Tsinghua University, Beijing, China
[3]Beihang University, Beijing, China

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36.2 A 200-10kHz 100V_{PP} Piezoelectric Micropump Driver Using Switched-Capacitor-Assisted Floating Linear Amplifier Achieving 83.4%-Peak-Efficiency and 0.24%-THD+N

T. Tang[1], Z. Tang[1], C. Hu[1], T-Y. Chen[2], X. Liu[3], J. Jiang[1]
[1]Southern University of Science and Technology, Shenzhen, China
[2]Erised Semiconductor, Shenzhen, China
[3]Chinese University of Hong Kong, Shenzhen, China

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36.3 A 92.21%-Peak-Efficiency Symmetric Step-Down Rectifier with Cycle-by-Cycle Reverse-Current Control Achieving Full-Load-Range Regulation for Wireless Power Transfer

Y. Lin, Y. Chen, J. Guo
Sun Yat-Sen University, Guangzhou, China

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36.4 A Fully Integrated Switched-Capacitor Energy Harvester with 12-V Storage and Self-Restoring Power-Path Feedback

B. Wang, J. Jung, E. Lee, M. Manohara, U. Guler, A. Chandrakasan
Massachusetts Institute of Technology, Cambridge, MA

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36.5 A Two-Perturbation Direct Impedance-Matching MPPT Technique with MPP Retention under Source-Voltage Variations for Thermoelectric Energy Harvesting

Z. Ye[1], C. Wang[2], R. Zhang[1], K. N. Leung[2], J. Guo[1]
[1]Sun Yat-Sen University, Guangzhou, China
[2]Chinese University of Hong Kong, Hong Kong, China

Break 3:15 PM

From Circuits to Waves: Signal Processing in Frequency, Time, and Space

Session Chair:
Alberto Valdes-Garcia, *IBM Research, Yorktown Heights, NY*
Session Co-Chair:
Davide Guermandi, *imec, Leuven, Belgium*

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37.1 Vector-Intelligent Synthetic Array (VISA): Efficient, Direct Data-to-Wireless Conversion at 140GHz
Y. Qin, Y. Feng, Z. Tang, Y. He, B. Zhang, C. Wang
University of Electronic Science and Technology of China, Chengdu, China

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37.2 A 4096-QAM Digital Transmitter with Reconfigurable Eight-Tap Free-Space FIR Filtering
Y. Liu, P. Zhang, Y. Chen, Y. Hu, Y. Chen, L. Wu, Y. Zhu, C. Deng, A. Zhang
Tsinghua University, Beijing, China

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37.3 A Scalable 4GS/s/chip Frequency-Channelized MP-DFT Radar-Correlation Front-End with 47.3 1b-TOPS Equivalent Throughput in 65nm CMOS
H. Jiang, J. Hu, X. Pu, Q. Wu, P. R. Kinget
Columbia University, New York, NY

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37.4 ISAAC: An Information-Shaping Array with Ambiguity Control Using Dynamic Spatial-Lattice Reconfiguration and Decoying for Point-to-Point Private Communication in Full-FoV
Z. Guo, H. Luo*, W. Deng, H. Ren, H. Jia, B. Chi*
Tsinghua University, Beijing, China
*Equally Credited Authors (ECAs)

Conclusion 5:15 PM

Circuits for Quantum and Other Unconventional Compute

Session Chair:
Joseph Bardin, *Google & UMass Amherst, Santa Barbara, CA*

Session Co-Chair:
Albert Wang, *Apple, Sunnyvale, CA*

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38.1 Cryo-CMOS Reconfigurable Array with Real-time Optical Downlink and Complex-Weighted FDM Readout

Z. Dai[1], R. Wu[2], D. Yan[1], Z. Xu[2], C. Liu[1], Y. Yang[2], Y. Fan[1], C. Wang[1]
[1]University of Electronic Science and Technology of China, Chengdu, China
[2]Chengdu Data Automation System Technologies, Chengdu, China

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38.2 CryoSieve: A 22nm-FDSOI Cryogenic Quantum Error Correction Syndrome Processor with 17× Cryo–RT Transmission Energy Reduction

G. Tao[1], A. Knapen[1], H. Wang[1], J. Luo[2], H. Wu[1], R. Qi[2], X. Wei[1], J. Mack[1], G. Ravi[1], D. Sylvester[1], M. Saligane[1,2], Q. Zhang[1]
[1]University of Michigan, Ann Arbor, MI
[2]Brown University, Providence, RI

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38.3 A 4K Cryo-CMOS Write/Read Control IC for Phononic Quantum-Memory Bit-cell

Y. Guo[1], Y. Liu*[2], H. Li*[3], S. Yin[1], Y. Li[1], Z. Chang[3], W. Wang[3], T. Tian[3], Q. Liu[2], G. Wang[1], T. Li[3], H. Jiang[3]*
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[2]Beijing Academy of Quantum Information Sciences, Beijing, China
[3]Tsinghua University, Beijing, China
*Equally Credited Authors (ECAs)

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38.4 A Sub-mW 4K Qubit-Drive Transmitter Using an Asynchronous DTC-Timed DAC with Adaptive Time-Grid Pulse Shaping Achieving >72dBc SFDR and 8GS/s Effective Sampling Rate in 28nm CMOS

F. Yuan[1], H. Su[1], Y. Miao[1], X. Zhang[1], Y. Wu[1], H. Wang[2], R. P. Martins[1], P. I. Mak[1], Y. Peng[1]
[1]University of Macau, Macau, China
[2]Beijing Academy of Quantum Information Sciences, Beijing, China

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38.5 FlexSoC: A 285.5k-TFT 2MHz Flexible 32-Bit System-on-Chip with 5-Metal Monolithic LTPS Integration and Drive-Extended Parasitic-Suppressed Standard Cells

J. Song, A. Yan, E. Zhang, Y. Yang, H. Liu, T-L. Ren

Tsinghua University, Beijing, China

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38.6 A 231.061GHz Chip-Scale Molecular Clock with Hershey-Kiss FM and Digital 1st-/5th-Order Locking Achieving <100ppt Allan Deviation From 1s to 10,000s

J. Jung, K. Pochana, J. Wang, T. Weigand, E. Lee, I. Choe, K. A. Nelson, R. Han

Massachusetts Institute of Technology, Cambridge, MA

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38.7 A 15-b Cryo-CMOS Z/Flux Driver with mHz-Range Bias-Noise Filtering for Flux-Tunable Superconducting Qubits

J. Lee[1,2], S. Bae*[2], J-Y. Sim[2]*

[1]Samsung Electronics, Hwaseong, Korea

[2]Pohang University of Science and Technology, Pohang, Korea

*Equally Credited Authors (ECAs)

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38.8 A 4–100 K k_BT/C Noise-based Cryo-CMOS Temperature Sensor with a Trimming-Free 0.9997-R^2 Linearity

J. Weng[1], Y. Sha*[1], P. Wang[2], Z. Huang[1], Q. Liu[1], M. Liu[1]*

[1]Fudan University, Shanghai, China

[2]Shanghai Institute of Technical Physics Chinese Academy of Sciences, Shanghai, China

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38.9 An 11.3ppm/K, 5-50K CMOS Current Reference for Cryo-CMOS Superconducting-qubit Controllers

S. Ray, D. Frank, J. Bulzacchelli, J. Timmerwilke, R. Robertazzi, B. Sadhu, D. Friedman

IBM Research, Yorktown Heights, NY

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38.10 A 0.9%FAR 0.91µW Attention-Based Flexible Attention-spans Keyword Spotting System with Fine-Grained AFE Gating

P. Huang[1], Z. Liu[1], W-H. Yu[1], K-F. Un[1], L. Zhao[2], R. P. Martins[1], P-I. Mak[1]

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[2]Zhejiang University, Hangzhou, China

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Memory Interfaces

Session Chair: ***Kyunghoon Kim,*** *SK hynix, Icheon, Korea*

Session Co-Chair: ***Thomas Hein,*** *Micron, Munich, Germany*

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39.1 A 17.6Gb/s/pin LPDDR6 Ultra SDRAM interface design with switch cross-coupled DFE CA IB, improved DCC WCK IB, hybrid 240 Ohm ZQ leg DQ TX and high-speed IO DFT schemes

X. Chen, W. Zhang, Z. Xue, W. Li, X. Tang, S. Ma, H. Tu, E. Gao, H. Li, K. Cao, Y. Zhu

Changxin Memory Technologies, Hefei, China

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39.2 A 25-Gb/s/pin 0.036-pJ/bit/dB LPDDR Transmitter with Consecutive-Identical-Digit-Length-Adaptive and Simultaneous-Switching-Noise-Mitigating Active-Inductive Below-V_{SS} Pull-Down Pre-Emphasis

G. Ha, J-H. Chae

Kwangwoon University, Seoul, Korea

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39.3 A 0.5-to-8GHz Self-Relative-Jitter-Cancellation Technique Co-Designed with a Quadrature-Error Corrector for Unmatched Memory Interfaces

J. Seo, H. Jeon, M. Jeon, J. Lee, J. Choi

Seoul National University, Seoul, Korea

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39.4 A 4×128-Gb/s Single-Ended PAM-4 Transceiver with Crosstalk-Canceling Transformer-Capacitance Network for Ultra-High-Density Memory Links

Q. Liu[1], Y. Hui[1], Y. Nong[1], T. Zhao[1], Z. Li[1], Y. Liu[1], J. Guo[1], D. Li[2], L. Du[1], Y. Du[1]

[1]Nanjing University, Nanjing, China
[2]Wuhan University of Technology, Wuhan, China

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39.5 A 30Gb/s/pin Single-Ended PAM4 Receiver with Reconfigurable 4-Tap Charge-Based DFE and Self-Calibration of Vref and DFE Coefficients

H. Seong[1], J. Park[1], J. Lee[1], J. Lee[1], Y. Choi[2], M. Kwak[2], J-Y. Sim[1], S-K. Lee[1]

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[2]Samsung Electronics, Hwaseong, Korea

Break 3:15 PM

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39.6 A 16.5Gb/s/pin Self-Calibrating 18-UI-Span Floating-Tap DFE Receiver for Multi-Drop Memory Interfaces

M. Kim[*1], *J-W. Moon*[*1], *B-C. Kim*[1], *J. Lee*[1], *H. Seong*[1], *J. Park*[2], *C. Yoon*[2], *J-Y. Sim*[1], *S-K. Lee*[1]

[1]Pohang University of Science and Technology, Pohang, Korea
[2]Samsung Electronics, Hwaseong, Korea
*Equally Credited Authors (ECAs)

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39.7 A 65.9Tb/s/mm 0.18pJ/b Crosstalk-Balanced EPAM4 Transceiver for High-Density Short-Reach Memory Interfaces in 28nm CMOS

G. Zhang[*1], *R. Kuai*[*1], *F. Lv*[1], *L. Xiao*[1], *M. Li*[1], *L. Yuan*[1], *B. Bai*[1], *K. Xin*[1], *C. Fan*[2], *G. Zhang*[2], *X. Zheng*[3], *H. Sun*[3], *M. Lai*[1]

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[2]Xi'an Jiaotong University, Xi'an, China
[3]Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China
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39.8 A 40Gb/s/pin Single-Ended PAM4 Transceiver with Three-Step Pattern-Based Switching-Jitter Compensation for Memory Interfaces

T. Kim[1], *H. Shin*[1], *C. Sim*[1], *S. Kim*[1], *J. So*[1], *H. Shin*[1], *S-B. Lee*[1], *H. Jung*[1], *C. Lee*[1], *K. Yoon*[1], *G. An*[2], *S-M. Lee*[3], *S-H. Kim*[3], *S. Yoo*[3], *J. Song*[2], *C. Kim*[1]

[1]Korea University, Seoul, Korea
[2]Incheon National University, Incheon, Korea
[3]Samsung Electronics, Hwaseong, Korea

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39.9 A 14-nm 2.7D Die-to-Die Interface with a 31-Gb/s 0.251-pJ/bit Equalizer-Free NRZ 3D IO and a 6.5-mm 0.135-pJ/bit On-Chip Interconnect

T. Kong[1], *S-J. Yun*[1], *S. Jung*[1], *E. Kim*[1], *H. Choi*[1], *H-J. Kim-Lee*[1], *S-E. Jo*[1], *S. Lee*[1], *S. J. Kim*[1], *J. Kim*[2], *W-S. Choi*[3], *J. Han*[4], *S. Lee*[2], *H-S. Choi*[3], *Y. Shin*[3], *Y. Kwon*[4]

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[2]Konkuk University, Seoul, Korea
[3]Seoul National University, Seoul, Korea
[4]Hanyang University, Seoul, Korea

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High-Frequency Synthesizers and LO Generation

Session Chair: ***Ping Lu,*** *NVIDIA, Santa Clara, CA*

Session Co-Chair: ***Simone Dartizio,*** *Politecnico di Milano, Milan, Italy*

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40.1 A 158GHz Current-Mode Sub-Sampling PLL with 44fs$_{rms}$ Integrated Jitter and 9mW Power Consumption

S. Sabbaghi, Z. Mohseni, Q. J. Gu

Georgia Institute of Technology, Atlanta, GA

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40.2 A 0.60-to-16.05GHz Ultra-Wide Quadrature-LO Generator Using a 16-Phase RTWO Fractional-*N* PLL and Fractional-Resolution Quadrature Frequency Divider Achieving 64.2fs$_{rms}$ Jitter and –249.1dB FoM$_J$

J. Lee, H. Lee*, J. Lee*, J. Kim, J. Choi*

Seoul National University, Seoul, Korea

*Equally Credited Authors (ECAs)

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40.3 A 10GHz FMCW Synthesizer with a Phase-Aligned Frequency Interpolator Achieving 2812.8MHz/µs Chirp Slope and 0.0297% rms Frequency Error with a 50MHz Reference

D. Zhang, Y. Zhang, Z. Liu, Y. Xiong, Z. Zhang, T. Hu, W. Wang, D. Li, M. Tang, D. Xu, Y. Liu, D. Xu, K. Kunihiro, H. Sakai, K. Okada

Institute of Science Tokyo, Tokyo, Japan

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40.4 A 16-to-19GHz Fractional-N Sampling PLL with DTC Nonlinearity Cancellation and Range Reduction Achieving -251.6dB FoM Using 100MHz FREF

R. Yang[1], Y. Kang*[1], B. Chen[1,2], Z. Zong[1]*

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[2]Hong Kong University of Science and Technology, Hong Kong, China

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40.5 A 51.1-to-57.2GHz Bufferless Class-F_2 Self-Mixing VCO Achieving 193.1dBc/Hz FoM

C. Song, Y. Wang*, L. Wu*
The Chinese University of Hong Kong (Shenzhen), Shenzhen, China
*Equally Credited Authors (ECAs)

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40.6 A 24.0-to-27.3GHz Differential Ping-Pong Gain-Boosting Charge-Sharing Locking PLL with Offset-Precharge Spur Cancellation Achieving 55fs Jitter and -74.4dBc Spur

C. Khongprasongsiri[1], P. Sawakewang[1], C. Liu[1], P. Kaczmarczyk[1,2], F. Hong[1], R. B. Staszewski[1,2], T. Siriburanon[1]
[1]University College Dublin, Dublin, Ireland
[2]AGH University of Krakow, Krakow, Poland

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40.7 A 25.8-to-60.6GHz LO Generator with a Single-Mode VCO, Fundamental-Cancelling 3rd-Harmonic Extractor and Intrinsic Differential 2nd-Harmonic Generator Achieving $FoM_{T@10MHz}$ of 210.9dBc/Hz in 65nm CMOS

T. Ou[1], X. Du[1], J. He[1], Z. Chen[1], Y. Peng[1], H. Xu[2], N. Yan[2], J. Yin[1], R. P. Martins[1], M-K. Law[1]
[1]University of Macau, Macao, China
[2]Fudan University, Shanghai, China

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40.8 A 0.042mm² 92-to-112GHz Fundamental Bandpass Distributed VCO with Second-Harmonic Enhancement Achieving 197.1dBc/Hz FoM_T

Y. Fang[1], Z. Fu[1], H. Guo[2], T. Chi[2], S. Li[1]
[1]University of Texas, Austin, TX
[2]Rice University, Houston, TX

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40.9 Quad-Core Series-Resonance 20GHz SiGe BiCMOS VCO with –129dBc/Hz Phase Noise at 1MHz Offset, 190dBc/Hz FoM, and 60GHz Tripled Output

K. Vural[1], A. Bilato[2], G. De Filippi[2], J. Jamal[1], L. Piotto[2], A. Mazzanti[1,2]
[1]University of Pavia, Pavia, Italy
[2]Fondazione Chips-IT, Pavia, Italy

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40.10 A 20-to-35GHz CMOS Frequency Doubler with Fourth-Harmonic-Assisted Drain-Voltage Shaping and Coupled-Line Output Matching Achieving 30.2% Total Efficiency at 11.4dBm Output Power

C. Rong, W. Li, H. Guo
University of Science and Technology of China, Hefei, China

Conclusion 5:35 PM

Emerging Electrical and Optical Connectivity: From System Architecture to Circuits

Organizers: **Ahmed Mostafa,** *Marvell, Santa Clara, CA*
Ariel Cohen, *Technion, Israel Institute of Technology, Haifa, Israel*

Co-Organizer: **Jay Im,** *AMD, San Jose, CA*

Zeynep Toprak Deniz, *IBM Research, Yorktown Heights, NY*

Champions: **Giuseppe Gramegna,** *imec, Leuven, Belgium*
Jae-sun Seo, *Cornell University, Ithaca, NY*

This forum brings together system architects, circuit designers, optical-link experts and researchers to explore advances in achieving high-bandwidth density through electrical and optical interconnects. As data-center networks evolve, connectivity is increasingly classified into scale-up, scale-out, and scale-across domains, each presenting distinct performance, power, and integration challenges. The requirement for high-bandwidth connectivity is driving the emergence of dense optical interconnects to achieve better compute efficiency.

The scaling path toward 400Gb/s and beyond exposes fundamental limits in signal integrity, power delivery, and packaging. In addition, the rapid growth of AI clusters is further intensifying I/O bandwidth and power constraints. Together, these pressures are accelerating a shift beyond traditional electrical interconnects toward heterogeneous and optical-centric architectures.

This forum will examine how next-generation network architectures leverage novel electrical and optical connectivity to optimize compute efficiency and energy consumption. It will highlight state-of-the-art circuit techniques and performance advances critical to realizing high-performance electrical and optical transceivers. Key circuit and technology limitations, along with innovations enabling 400+-Gb/s operation, will be discussed.

By highlighting emerging connectivity paradigms and practical implementation strategies, this forum aims to provide insights into scalable, manufacturable, reliable, and interoperable systems for next-generation computing infrastructure.

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Introduction** **Ahmed Mostafa,** *Marvell, Santa Clara, CA*
8:25 AM	**Breaking the AI Interconnect Wall: From Scale-In to Scale-Across, Architecture to Circuits** **Lenin Patra,** *Marvell, Santa Clara, CA*
9:10 AM	**Scaling Optical Interconnects for AI Data Centers: Up, Across, and Out** **Clint Schow,** *UC Santa Barbara, Santa Barbara, CA*
9:55 AM	Break
10:10 AM	**High-Speed Electrical and Optical Transceiver DACs: Architecture, Circuit Design, and Test Challenges and Solutions** **Ajay Balankutty,** *AMD, Santa Clara, CA*
10:55 AM	**High-Speed Receiver Design Techniques for Electrical-Optical Interconnects** **Sam Palermo,** *Texas A&M University, College Station, TX*
11:40 AM	**Power/Performance Challenges for Next-Generation High Baud-Rate Optical Links** **Arash Farhoodfar,** *Google, Mountain View, CA*
12:25 PM	Lunch
1:40 PM	**Transceiver Link Budget: Accounting for and Implications of Noise, Nonlinearity, ISI and Reflection in Modern 200 & 400 Gb/s Serial Links** **Itamar Levin,** *Altera, Jerusalem, Israel*
2:25 PM	**Clocking Solutions for DACs and ADCs in DSP-based Wireline Receivers** **Wei-Zen Chen,** *National Yang Ming Chiao Tung University, Hsinchu, Taiwan*
3:10 PM	Break
3:25 PM	**High-Density Die-to-Die Chiplet Interconnects** **Gerald Pasdast,** *Intel, Santa Clara, CA*
4:10 PM	**Beyond Traditional Copper: RF-over-Waveguide as a High-Bandwidth, Low-Power Bridge to Next-Gen AI Fabrics** **Hyeonmin Bae,** *KAIST, Seoul, Korea*
4:55 PM	Closing Remarks

AI Optimized Sensing: Approaching Physical World Through Co-Designed Sensors and AI

Organizers: **Atsumi Niwa,** *Sony Semiconductor Solutions Corporation, Atsugi, Japan*
Mei-Chen Chuang, *TSMC, Hsinchu, Taiwan*

Co-Organizers: **Leonardo Gasparini,** *Fondazione Bruno Kessler, Trento, Italy*
Sam Sheng, *Google, Stanford University, Mountain View, CA*
Bo (Angela) Wang, *Singapore University of Technology and Design, Singapore, Singapore*
Augusto Ximenes, *CogniSea, Seattle, WA*

Champions: **Makoto Ikeda,** *University of Tokyo, Tokyo, Japan*
Qinwen Fan, *Delft University of Technology, Delft, The Netherlands*

With the rapid advancement of AI technology and Physical AI, there is growing interest in sensing technologies that enable direct interaction with the real world. While sensor and AI processing technologies have developed independently based on their own performance metrics, their integrated approach has become a critical technical consideration. This forum will conduct an in-depth examination of the current state and future technological possibilities of sensing technologies that consider AI processing, taking into account these technological trends. Specifically, we will discuss circuit technology approaches in the collaborative design of sensors and AI processing, organize the technical and implementation challenges for realizing AI-integrated systems that exceed conventional single-sensor performance, and clarify the path to practical implementation from the perspective of circuit designers.

Through such discussions, we aim to provide insights that will enable semiconductor circuit technology experts to understand the technological direction of next-generation sensing systems and apply this knowledge to actual design and development work.

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Introduction** **Atsumi Niwa,** *Sony Semiconductor Solutions Corporation, Atsugi, Japan*
8:25 AM	**The Grand Vision: How AI-Integrated Sensors will Transform Our World** **Brian Chen,** *Google, Mountain View, CA*
9:15 AM	**Event-Based Vision: Co-Designing Sensing and Intelligence for the Dynamic World** **Guillermo Gallego,** *Technische Universität, Berlin, Germany*
10:05 AM	Break
10:20 AM	**Multimodal Sensor Fusion on the Edge** **Chiao Liu,** *Meta, Redmond, WA*
11:10 AM	**What Sensors Miss, Inference Recovers: From Compressive Sampling to Generative Imaging** **Ralph Etienne-Cummings,** *Johns Hopkins University, Baltimore, MD*
12:00 PM	Lunch
1:20 PM	**Intelligent Sensor Readout: Adaptive Sensing and Feature Extraction at the Analog-Digital Boundary** **Chih-Cheng Hsieh,** *National Tsing-Hua University, Hsinchu, Taiwan*
2:10 PM	**Low-Power Analog Front-Ends for Always-On AI Sensing** **Gerard Mora-Puchalt,** *Analog Devices, Valencia, Spain*
3:00 PM	Break
3:15 PM	**Co-Design of Machine Learning, Edge Computing and Imaging Applications** **Yoshitaka Miyatani,** *Sony Semiconductor Solutions, Tokyo, Japan*
4:05 PM	**In-Sensor Analog Computing: The Path to Extreme Energy Efficiency** **Ghazi Syed Sarwat,** *IBM, Zurich, Switzerland*
4:55 PM	Closing Remarks

Towards 6G: Circuits and Systems for Joint Communication, Sensing, and Edge AI

Organizers: **Konstantinos Manetakis,** *Cisco Systems, Thalwil, Switzerland*
Julian Tham, *Infineon, San Jose, CA*

Co-Organizers: **Alberto Valdes Garcia,** *IBM Research, Yorktown Heights, NY*
Ewout Martens, *imec, Leuven, Belgium*
Minyoung Song, *DGIST, Daegu, Korea*
Omeed Momeni, *UC Davis, Davis, CA*

Champions: **Kostas Doris,** *NXP, Eindhoven, The Netherlands*
Chris Rudell, *University of Washington, Seattle, WA*

As we move toward 6G and edge AI, wireless hardware must support more than traditional communication. Future systems must combine high-capacity links, accurate sensing, low-latency local intelligence, and resilient security, all under strict power and thermal limits. These demands push RF front-ends, data converters, frequency generation, and 2.5D/3D packaging to operate at higher frequencies, scale to larger phased arrays, and bring lightweight real-time AI closer to the RF front-end for inference and hardware augmentation. Enabling these capabilities requires advances in wideband high-frequency RFIC architectures, tighter RFIC-antenna co-design, improved thermal management in heterogeneous integration, high-speed low-power converters, low-jitter frequency synthesis, and compute architectures for AI-enhanced beamforming and sensing. This forum brings together experts from industry and academia to discuss these advances across RF-AI platforms.

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Introduction** **Konstantinos Manetakis,** *Cisco Systems, Thalwil, Switzerland*
8:25 AM	**6G's Sixth Sense: Making the Network a Sensor** **Harish Viswanathan,** *Nokia Bell Labs, Murray Hill, NJ*
9:15 AM	**System-Level Challenges in Joint Communication, Sensing, and Edge ML** **Bo Tan,** *University College London, London, United Kingdom*
10:05 AM	Break
10:20 AM	**AI-Based ISAC with Phased Arrays: System Design, Algorithms, and Edge Deployment** **Arun Paidimarri,** *IBM Research, Yorktown Heights, NY*
11:10 AM	**Prior Knowledge-Guided Deep-Learning-Enabled Generative Synthesis for 6G EM Devices** **Zhi Ning Chen,** *National University of Singapore, Singapore*
12:00 PM	Lunch
1:20 PM	**Bridging the LiDAR Gap: LO Synchronization and Array Architectures for mm-Wave Radars** **Jingzhi Zhang,** *University of Electronic Science and Technology of China, Chengdu, China*
2:10 PM	**Trends and Opportunities of Data Conversion for MIMO and Beamforming** **Shuo-Wei (Mike) Chen,** *University of Southern California, Los Angeles, CA*
3:00 PM	Break
3:15 PM	**Compute Architectures for RF-Aware Edge AI and Low-Latency Near-Sensor Processing** **Luca Benini,** *ETH Zurich, Zurich, Switzerland*
4:05 PM	**Enabling Next-Generation RF-AI Systems through 2.5D/3D Heterogeneous Integration** **Xiao Sun,** *imec, Leuven, Belgium*
4:55 PM	Closing Remarks

Enabling the Quantum Revolution: Silicon Systems for High-Precision Quantum Sensing and Computing

Organizers: **Anh Tuan Do,** *A STAR, Singapore, Singapore*
Ka-Meng Lei, *University of Macau, Taipa, Macau, China*

Co-Organizers: **Filip Tavernier,** *KU Leuven, Leuven, Belgium*
Chris Rudell, *University of Washington, Seattle, WA*
Alyosha Molnar, *Cornell University, Ithaca, NY*

Champions: **Mingoo Seok,** *Columbia University, New York, NY*
Carolina Mora Lopez, *imec, Leuven, Belgium*

The central objective of this forum is to explore the frontiers of silicon-based quantum hardware. As the industry targets the '10,000-qubit' milestone and the deployment of field-ready quantum sensors, traditional modular electronics have reached a physical and thermal bottleneck. This forum examines how silicon-based systems serve as the essential catalyst for this revolution. By bringing together industry architects and academic pioneers, the session will address the critical engineering trade-offs for energy-efficient cryogenic transceivers, autonomous qubit state controllers, and integrated readout for single-photon and NV-diamond sensing. Participants will gain actionable insights into the industrial state of the art—including temperature-aware design in the cryogenic regime—and identify the remaining challenge that the solid-state circuits community is uniquely positioned to solve.

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Introduction** **Anh Tuan Do,** *A STAR, Singapore, Singapore*
8:25 AM	**Integrated Single-Photon Sensing/Imaging** **Edoardo Charbon,** *EPFL, Lausanne, Switzerland*
9:15 AM	**Challenges in Engineering Quantum Computers** **Juhwan Yoo,** *Google Quantum AI, Goleta, CA*
10:05 AM	Break
10:20 AM	**Cryo-CMOS Designs for Superconducting Qubit-Based Quantum Computers: Challenges, Approaches, and Demonstrations** **Daniel Friedman,** *IBM, Yorktown Heights, NY*
11:10 AM	**NV Diamond Quantum Magnetometer with CMOS IC** **Jens Anders,** *University of Stuttgart, Stuttgart, Germany*
12:00 PM	Lunch
1:20 PM	**Scalable Solution for Quantum Sensing and Computing** **Elena Blokhina,** *Equal1, Dublin, Ireland*
2:10 PM	**Temperature Sensing in Cryogenic Regime** **Yatao Peng,** *University of Macau, Taipa, Macau, China*
3:00 PM	Break
3:15 PM	**Heterogeneous Integration of Spin–Photon Interfaces** **Mohamed I. Ibrahim,** *Cornell University, Ithaca, NY*
4:05 PM	**High-Fidelity Cryogenic Quantum Controller IC** **Jae-Yoon Sim,** *Pohang University of Science and Technology, Pohang, Korea*
4:55 PM	Closing Remarks

Hardware Security, from Fundamentals to Implementations

Agenda

Time:	Topic:
8:00 AM	Breakfast
8:25 AM	**Introduction by Chair** ***Yvain Thonnart,*** *CEA-List, Grenoble, France*
8:30 AM	**Introduction to Hardware Security** ***Todd M. Austin,*** *University of Michigan, Ann Arbor, MI*
10:00 AM	Break
10:30 AM	**Secure and Efficient Hardware Architectures for Cryptography** ***Patrick R. Schaumont,*** *Worcester Polytechnic Institute, Worcester, MA*
12:15 PM	Lunch
1:20 PM	**Hardware Attacks and Chip-Level Countermeasures** ***Makoto Nagata,*** *Kobe University, Kobe, Japan*
2:50 PM	Break
3:20 PM	**Circuits for Hardware Roots of Trust** ***Ingrid Verbauwhede,*** *KU Leuven, Leuven, Belgium*
4:50 PM	Conclusion

Introduction

Hardware security is taking on growing importance, going beyond traditional roles in protecting systems and data toward ever-expanding use cases in AI, datacenters, and emerging applications. Architectural and circuit-level techniques supporting secure designs are critical enablers of this growth. Progress in this area is even more critical given the increasing sophistication of threats and the growing demand for robust security in high-volume products. This short course is designed to explore these foundational and more advanced concepts. The first lecture provides an introduction to hardware security and its criticality in the age of AI, with a general overview of threats and defense. The second lecture focuses on digital architectures for cryptography, reviewing secure algorithms, crypto-accelerators, and their secured implementations. The third lecture addresses the basics of physical-level attacks and associated countermeasures by circuits as well as packaging structures for security. Finally, the last lecture introduces circuits for hardware roots of trust, covering true random number generators, physically unclonable functions, and their evaluation against security standards.

A Certificate of Completion will be issued for each of the four Short-Course lectures to in-person attendees who complete a short questionnaire at the end of each lecture.

8:30 AM

SC1: Introduction to Hardware Security

Todd M. Austin, *University of Michigan, Ann Arbor, MI*

What happens when the software protecting our systems can no longer be trusted? Hardware offers a foundation for security that holds even after software is compromised. This lecture introduces the fundamentals: security goals, encryption, authentication, roots of trust, secure boot, and trusted execution, plus threats from hardware Trojans to side channels and fault injection. As AI accelerates the discovery of software exploits, trust in future systems will increasingly rest on hardware.

Todd Austin is a Professor of Computer Science at the University of Michigan. His research spans computer architecture, hardware security, dependable systems, and AI hardware. His contributions include the SimpleScalar simulator, Razor circuits, and the Morpheus secure processor.

10:30 AM

SC2: Secure and Efficient Hardware Architectures for Cryptography

Patrick R. Schaumont, *Worcester Polytechnic Institute, Worcester, MA*

Hardware architectures for cryptography achieve efficiency and performance by specializing to the common primitives of cryptography. However, the very security objectives that justify the use of hardware also apply to the cryptographic realization itself, confronting the designer with an additional challenge: maintaining security in the hardware design. This lecture demonstrates the need for cryptographic hardware acceleration, and reviews common implementation techniques for recent public-key cryptography as well as architectural techniques to ensure implementation security.

Patrick Schaumont is a Dean's Excellence Professor and Joseph Samuel Satin Distinguished Fellow in Electrical and Computer Engineering at Worcester Polytechnic Institute. He received a PhD from UCLA in 2004. His research focuses on secure, efficient, and real-time embedded computing systems, and on associated design methods to optimize and test secure hardware design. Schaumont has served as co-chair in leading conferences in cryptographic and secure engineering, including CRYPTO, CHES, HOST, and FDTC. He serves as the Editor-in-Chief for IEEE Transactions on Emerging Topics in Computing. He is a Fellow of the IEEE.

1:20 PM

SC3: Hardware Attacks and Chip-Level Countermeasures

Makoto Nagata, *Kobe University, Kobe, Japan*

IC chips are threatened by physical-level attacks on security functionality. This lecture covers the basics of physical interaction on IC chips, the roots of vulnerability in secure IC systems and the countermeasures by circuits as well as packaging structures. Physical medias include voltage pulses, electromagnetic (EM) waves as well as photons and laser beams and also appear in emission and by irradiation. Circuit techniques and simulation methodologies are highlighted for security by design.

Makoto Nagata received the B.S. and M.S. degrees in physics from Gakushuin University in 1991 and 1993, respectively, and the Ph.D. degree in electronics engineering from Hiroshima University in 2001. He is a full professor at Kobe University since 2009. His interests include analog techniques for digital security as well as for system safety. He chaired the technology directions subcommittee for ISSCC (2018-2022) and served as an executive committee member of the conference (2023-2025). He was the technical program chair (2010–2011), the symposium chair (2012–2013), and an executive committee member (2014–2015) for the symposium on VLSI circuits. He was SSCS AdCom member (2020-2022) and appointed as SSCS distinguished lecturer (2020-2021 and 2024-2025).

3:20 PM

SC4: Circuits for Hardware Roots of Trust

Ingrid Verbauwhede, *KU Leuven, Leuven, Belgium*

This lecture will cover first the definition of a root of trust. Next, it will introduce the role of circuits as a foundation for a root of trust. It will cover circuits to protect against attacks and to enable cryptographic and security protocols. It will further go into details on secure circuit styles, physical sources of entropy for true-random-number generators and physically unclonable functions. Post-processing is required to make these sources suitable in cryptographic protocols.

Ingrid Verbauwhede is a professor at COSIC KULeuven, and a co-founder & scientific advisor to Belfort. She works on post-quantum crypto, computing on encrypted data, circuits for security and trusted computing. She is a fellow of IEEE and IACR, received the 2023 IEEE Don Pederson and 2025 FWO excellence awards.

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HOW TO REGISTER FOR ISSCC

Online: This is the only way to register and will give you immediate email confirmation of your events. Go to the ISSCC website at www.isscc.org and select the link to the Registration website.
Payment Options: Immediate payment can be made online via credit card. **Registrations received without full payment will not be processed until payment is received at YesEvents.** Please read the instructions on the Registration website.

COVID 19 PROTOCOLS

The health and safety of our conference attendees is our top priority. The ISSCC 2027 conference Organizing Committee remains vigilant in monitoring the COVID-19 pandemic. The conference will follow CDC and State of California guidelines. ISSCC is planned as an in-person event but it also has an online offering. We look forward to you joining us in San Francisco, CA. If you don't feel comfortable participating in large gatherings, or if your organization has travel restrictions, we encourage you to join us online.

MASKS, VACCINATION, SANITIZERS

Masks help slow the spread of the virus. They help to protect the medically vulnerable and those unable to get vaccinated. In San Francisco there are no longer masking requirements for most people. People may choose to wear masks, even when they are not required. Respect the choices others make for their health.

Currently, proof of vaccination is no longer required in meetings in San Francisco. We will be monitoring that regulation and the ISSCC website will be updated as regulations change.

Hand sanitizing lotion will be available throughout the hotel and at the Registration desk.

REGISTRATION DESK HOURS:

Saturday, February 13:	**4:00 pm to 7:00 pm**
Sunday, February 14:	**7:00 am to 8:30 pm**
Monday, February 15:	**6:30 am to 4:00 pm**
Tuesday, February 16:	**8:00 am to 4:00 pm**
Wednesday, February 17:	**8:00 am to 4:00 pm**
Thursday, February 18:	**7:00 am to 2:00 pm**

Students must present their Student ID
at the Registration Desk to receive the student rates.

Those registering at the IEEE Member rate
must login to their IEEE membership during registration.

Deadlines: The deadline for registering at the Early Registration rates is 12:00 Midnight EST **Sunday January 10, 2027.** After January 10th, and before 12:00 Midnight EST **Monday January 25th, 2027,** registrations will be processed **at the Late Registration rates. After January 25th, you must register at the on-site rates.** You are urged to register early to obtain the lowest rates and ensure your participation in all aspects of ISSCC.

Cancellations/Adjustments: Prior to 12:00 Midnight EST **Monday January 25, 2027,** conference registration can be cancelled. Fees paid will be refunded (less a processing fee of $75). Send an email to the registration contractor at ISSCCinfo@yesevents.com to cancel or make other adjustments.

No refunds will be made after 12:00 Midnight EST January 25th, 2027. Paid registrants who do not attend the conference will have access to the on-demand material.

IEEE MEMBERSHIP SAVES ON ISSCC REGISTRATION

Take advantage of significantly reduced ISSCC fees by using your IEEE membership number. Additional savings are available for members of the IEEE Solid-State Circuits Society. If you're an IEEE member and have forgotten your member number, simply phone IEEE at 1(800) 678-4333 (US and Canada) or +1 732-562-6785 (all other regions) and ask. IEEE membership staff will take about two minutes to look up your number for you. If you come to register on site without your membership card, you can phone IEEE then, too. Or you can request a membership number look-up online at https://supportcenter.ieee.org. If you're not an IEEE member, consider joining before you register to save on your fees. Join online at www.ieee.org/join any time and you'll receive your member number by email. When joining IEEE you can also select a Solid-State Circuits Society (SSCS) membership, which more than pays for itself by giving you an additional $30 off the registration fee among other benefits.

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We invite you to join or renew today to participate in exclusive educational events, access to leading research and best practice literature, and start your own career legacy by mentoring students and young professionals entering our field. It all starts with becoming a member of the Solid-State Circuits Society where you can:

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-Access exclusive SSCS Conference Digests for ISSCC, CICC, A-SSCC, ESSERC, and the Symposium on VLSI Technology and Circuits.

-Access publications - In addition to JSSC and the SSCS magazine, your SSCS membership gives you free access to IEEE Solid-State Circuits Letters, IEEE Sensors Magazine, IEEE Transactions on Circuits and Systems for Artificial Intelligence, and IEEE Transactions on AgriFood Electronics, plus discounted subscription rates to several other publications.

SSCS MEMBERSHIP SAVES EVEN MORE ON ISSCC REGISTRATION

This year, SSCS members will again receive an exclusive benefit of a $30 discount on the registration fee for ISSCC in addition to the IEEE discount. Also, the SSCS will again reward our members with a $10 Starbucks gift card when they attend the Conference as an SSCS member in good standing.

Join or renew your membership with IEEE’s Solid-State Circuits Society today at sscs.ieee.org - you will not want to miss out on the opportunities and benefits your membership will provide now and throughout your career.

ITEMS INCLUDED IN REGISTRATION

Technical Sessions & more: In person registration includes admission to all technical and evening sessions starting Sunday evening and continuing throughout Monday, Tuesday and Wednesday. Access to author interviews, social hours, to the Student Research Preview, to the Demo Sessions, to the open Women in Circuits Programs and to the Exhibition are also included. ISSCC does not offer partial conference registrations.

Technical Book Display: Several technical publishers will have collections of professional books and textbooks for sale during the Conference. The Book Display will be open on Monday from 3:00 pm to 8:00 pm; on Tuesday from 9:30 am to 1:30 pm; and on Tuesday from 3:00 pm to 8:00 pm.

Exhibition: For the third year, ISSCC is planning to organize an Exhibition open to Companies and non-academic Research Institutions. The main aim of the Exhibition is to showcase the participating Corporations/Institutions, their products and their applications. The Exhibition will be open on Monday from 3:00 pm to 8:00 pm; on Tuesday from 9:30 am to 1:30 pm; and on Tuesday from 3:00 pm to 8:00 pm.

Demonstration Sessions: Hardware demonstrations will support selected papers on Monday and Tuesday evenings.

Author Interviews: Author Interviews will be held Monday, Tuesday and Wednesday evenings. Authors from each day's papers will be available to discuss their work.

Monday and Tuesday Social Hours: Refreshments will be available starting at 5:30 pm.

University Events: Several universities are planning social events during the Conference. Check the University Events display at the conference for the list of universities, locations and times of these events.

Publications: All ISSCC registrants will be able to access the online Digital Digest:

-Visuals: A PDF of the visuals from all papers presented will be available for download.

-Demonstration Session Guidebook: A descriptive guide to the Demonstration Sessions will be available for download.

-Note: Instructions will be provided for all downloads. Downloads will be available during both the Conference and for a limited time afterwards.

OPTIONAL EVENTS

Educational Events: Many educational events are available at ISSCC for an additional fee. There are ten 90-minute Tutorials and two all-day Forums on Sunday. There are four additional all-day Forums on Thursday as well as an all-day Short Course. The Forums and Short Course include breakfast pastries and coffee, lunch and break refreshments. The Tutorials include break refreshments. See the schedule for details of the topics and times.

OPTIONAL PUBLICATIONS

ISSCC 2027 Publications: The following ISSCC 2027 digital publications can be purchased in advance or on site:

2027 ISSCC Download USB: All of the downloads included in conference registration, (regular papers and presentations) (mailed in March)

2027 Tutorials USB: All of the 90-minute Tutorials (mailed in June).

2027 Short Course USB: (mailed in June).

The Short Course and Tutorial USBs contain the audio and written English transcripts synchronized with the presentation visuals. In addition, the USBs contain a pdf file of the presentations and pdf files of key reference material.

Earlier ISSCC Publications: Selected publications from earlier conferences can be purchased. There are several ways to purchase this material:

-Items listed on the registration website can be purchased with registration and picked up at the conference.

-Visit the ISSCC Publications Desk. This desk is located in the registration area and has the same hours as conference registration. With payment by cash, check or credit card, you can purchase materials at this desk.

See the posted list at the Conference for titles and prices.

-Visit the ISSCC website at www.isscc.org and click on the link "SHOP/Shop ISSCC/Shop Now" where you can order online or download an order form to mail, email or fax. For a small shipping fee, this material will be sent to you immediately and you will not have to wait until you attend the Conference to get it.

HOW TO MAKE HOTEL RESERVATIONS

Online: ISSCC participants are urged to make their hotel reservations at the San Francisco Marriott Marquis online. Go to the conference website and click on the Hotel Reservation link. ***Conference room rates are $297 for a single/double*** *(per night plus tax),* ***Student Room Rate is $228 for a single/double*** *(per night plus tax).* You will need to show your student ID when checking in at the student rate. If you do not have a student ID your room will be at the Conference Room Rate. In addition, ISSCC attendees who are Bonvoy Members booked in the ISSCC group receive **in-room Internet access. Non-members of Bonvoy may sign up at check in, there is no charge for participation.**

All online reservations require the use of a credit card. Online reservations are confirmed immediately. You should print the page containing your confirmation number and reservation details and bring it with you when you travel to ISSCC. **Telephone:** Call 877- 622-3056 (US) or 415-896-1600 and ask for "Reservations." When making your reservation, identify the group as ISSCC 2027 to get the group rate.

Hotel Deadline: Reservations must be received at the San Francisco Marriott Marquis no later than 5 pm Pacific Time January 25th, 2027 to obtain the special ISSCC rates. A limited number of rooms are available at these rates. **Once this limit is reached or after January 25th, the group rates may no longer be available, and reservations will be filled at the best available rate.** Changes: Before the hotel deadline, your reservation can be changed by calling the telephone numbers above. After the hotel deadline, call the Marriott Marquis at 415-896-1600 (ask for "Reservations"). Have your hotel confirmation number ready.

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TAKING PICTURES, VIDEOS OR AUDIO RECORDINGS DURING ANY OF THE SESSIONS IS NOT PERMITTED

REFERENCE INFORMATION

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ISSCC Email:	ISSCC@ieee.org
Registration questions:	ISSCCinfo@yesevents.com
Hotel Information:	San Francisco Marriott Marquis Phone: 415-896-1600 780 Mission Street San Francisco, CA 94103
Press Information:	Laura C. Fujino Phone: 416-418-3034 University of Toronto Email: lcfujino@aol.com
Registration:	YesEvents Phone: 800-937-8728 Email: issccinfo@yesevents.com

Hotel Transportation

Visit the ISSCC website "Registration/Transportation from Airport" page for helpful travel information and links.
You can get a map and driving directions from the hotel website at:
www.marriott.com/hotels/travel/sfodt-san-francisco-marriott-marquis/

Next ISSCC Dates and Location:
ISSCC 2028 will be held on February 20-24, 2028
at the San Francisco Marriott Marquis Hotel.

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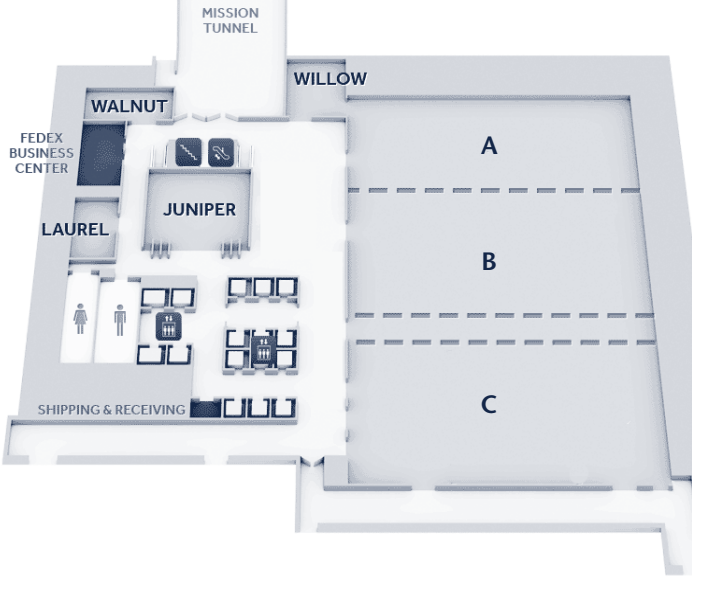

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